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Design Of Low Power Baugh-Wooley Multiplier

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Abstract: In VLSI design the performance of any system is determined by the performance of the elements of the system. Multiplier is the slow element in the system. The multiplier speed is depends on multiplication technique and type of adder. This paper proposes the type of architecture of 32 bit Baugh-Wooley multiplier. The code is implemented in XILINX ISE 14.5 software. The delay and power of 32 bit Baugh-Wooley multiplier obtained after synthesis and is compared with existing multiplier and found that the proposed Baugh-Wooley multiplier circuits seems to have better performance in terms of delay and power.

Keywords: VLSI, system, Baugh-Wooley Multiplier, XILINX, etc.

I. INTRODUCTION

Day by day a faster design with smaller area and lower power consumption is essential for the modern electronic designs . In microelectronics design multiplier is a fundamental unit and widely used in circuits, for which the multiplication process should be optimized properly. Multipliers generally have extended latency, huge area and consume substantial amount of power. Hence designing of low-power multiplier has become an important part in VLSI system design.

Multiplication involves two basic operations- the generation of the partial product and their accumulation. Therefore, there are possible ways to speed up the multiplication that reduces the complexity, and as a result reduces the time needed to accumulate the partial products. Both solutions can be applied simultaneously.

A. Baugh-Wooley Two's Complement Signed Multiplier

Two's Compliments is the most popular method in representing signed integers in Computer Sciences. It is also an operation of negation (Converting positive to negative numbers or vice -versa) in computers which represent negative numbers using two's complements. Its use is so wide today because it does not require the addition and subtraction circuitry to examine the signs of the operands to determine whether to add or subtract.

+N	Positive Integers	-N	Negative Integers		
			Sign & Magnitude	2's Complement	1's Complement
+0	0000	-0	1000	----	1111
+1	0001	-1	1001	1111	1110
+2	0010	-2	1010	1110	1101
+3	0011	-3	1011	1101	1100
+4	0100	-4	1100	1100	1011
+5	0101	-5	1101	1011	1010
+6	0110	-6	1110	1010	1001
+7	0111	-7	1111	1001	1000
+8	----	-8	----	1000	----

Fig. 1 a: - Two's complement and One's complement representation

Two's complement and one's complement representations are commonly used since arithmetic units are simpler to design. Fig.1 shows Two's & One's complement representation.

B. Baugh-Wooley Two'complement Signed numbers

Baugh-Wooley Two's complement Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits. Baugh-Wooley technique was developed to design direct multipliers for Two's complement numbers. When multiplying Two's complement numbers directly, each of the partial products to be added is a signed number. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree. According to Baugh-Wooley approach, an efficient method of adding extra entries to the bit matrix suggested to avoid having deal with the negatively weighted bits in the partial product matrix. In fig 1 (b) & (c) partial product arrays of 5*5 bits Unsigned and Signed bits are shown.

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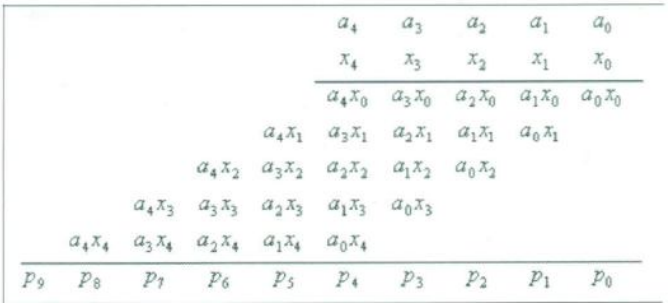

Fig. 1 b: - 55 Unsigned multiplication

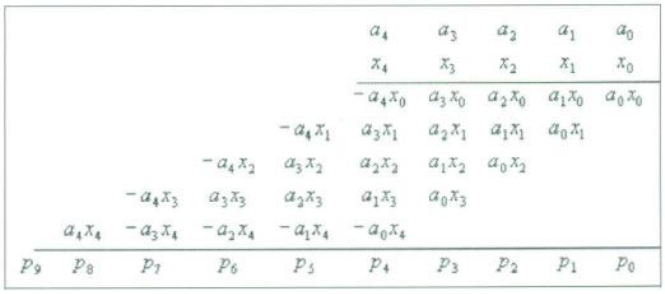

Fig. 1 c: - Signed multiplication

Figure 1 (c) shows how this algorithm works in the case of a 5x5 multiplication. The first three rows are referred to as PM (partial products with magnitude part) and generated by one NAND and three AND operations. The fourth row is called as PS (partial products with sign bit) and generated by one AND and three NAND operations with a sign (with magnitude part) and generated by one NAND and three AND operations. Consider the partial products of PM. Suppose b2= b0 in figure1 (c). Then the third row can be obtained by shifting the first row by 2 bits. Likewise, shift operation can be used to obtain a partial product of different bit level as in sign magnitude multiplication. Baugh-Wooley schemes become an area consuming when operands are greater than or equal to 32 bits. The rest of the paper is organised as follows. The Baugh-Wooley architecture is explained in section 2. Implementation results in terms of power, area, and speed 4 bit multipliers and comparison are presented.

C. Baugh-Wooley Architecture

Hardware architecture for Baugh-Wooley multiplier is shown in fig 2. It follows left shift algorithm. Through MUX (multiplexer) we can select which bit will multiply. Suppose we are adding +5 and -5 in decimal we get '0'. Now, represent these numbers in 2's complement form, and then we get +5 as 0101 and -5 as 1011. On adding these two numbers we get 10000. Discard carry, then the number is represented as '0'.

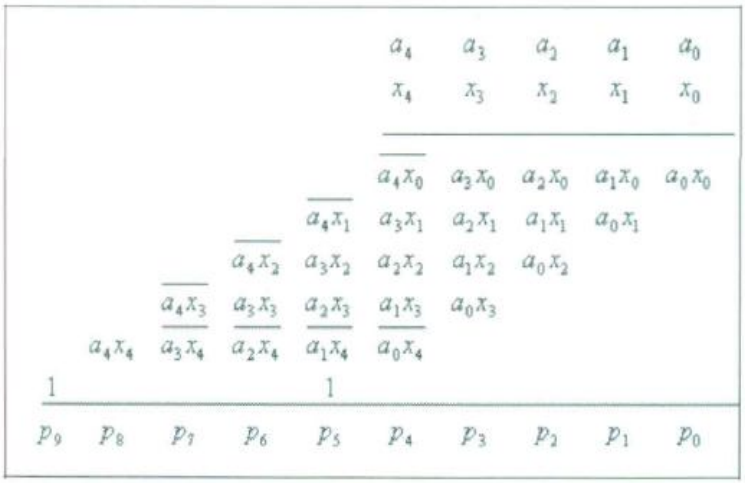

Fig. 1 d :- 5*5 Multiplication example of Baugh-Wooley architecture

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D. Baugh-Wooley Multiplier

Baugh- Wooley Multiplier is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complemented form. Partial Products are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh- Wooley Multiplier operates on signed operands with 2's complement representation to make sure that the signs of all partial products are positive. Here are using fewer steps and also lesser adders. Here a0, al, a2, a3& b0, b1, b2, b3 are the inputs. The outputs are p0, p1....p7. Pipelining resister used in this architecture, so it will take less time to multiply large number of 2 's complement but less than 32 bit. Above 32 bit Modified Baugh-Wooley Multipliers used.

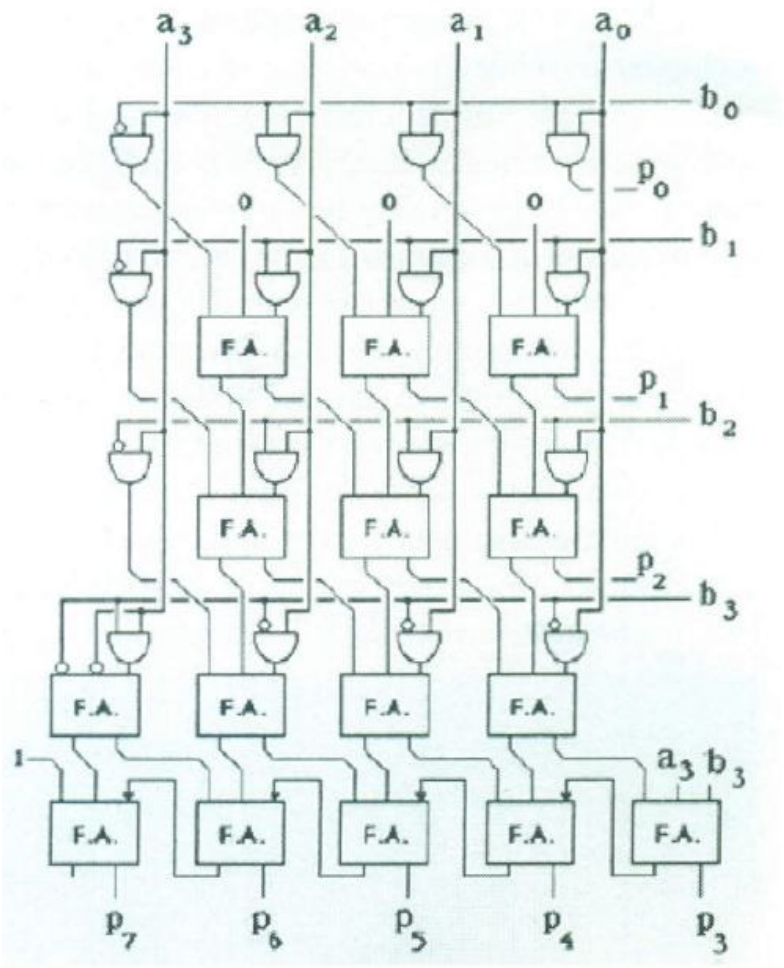

Fig. 2:- Block diagram of 4*4 Baugh-Wooley multiplier

II. IMPLEMENTATION ON XILINX SOFTWARE

Now we are moving towards main programming parts. Using the Baugh-Wooley multiplier we have to develop a program. In this paper the 32 bit multiplier is designed in VHDL (very high speed integrated circuits hardware description language). Synthesis and simulation was done in XILINX ISE 14.5. project navigator and simulator integrated in the XILINX package. XILINX is software which is purely based on the VHDL language. VHDL is Very Large Scale Integrated Circuit Hardware Description Language. We have performed our programming using the Vertex6XC6VCX75T FF84-2. Integrated Software Environment is a software tool produced by Xilinx for synthesis and analysis of HDL design, enabling the developer to synthesize their design, perform time analysis, examine RTL diagrams, simulate a design reaction to different stimuli, and configure the target device with the programmer. It includes ISE simulator which we can use for functionality verification of program.

III. EXPERIMENTAL RESULT

The result of the 32 bit Baugh-Wooley multiplier is given in the figures below in which 32-bit number is in binary form. Also the RTL schematic of Baugh-Wooley multiplier is given

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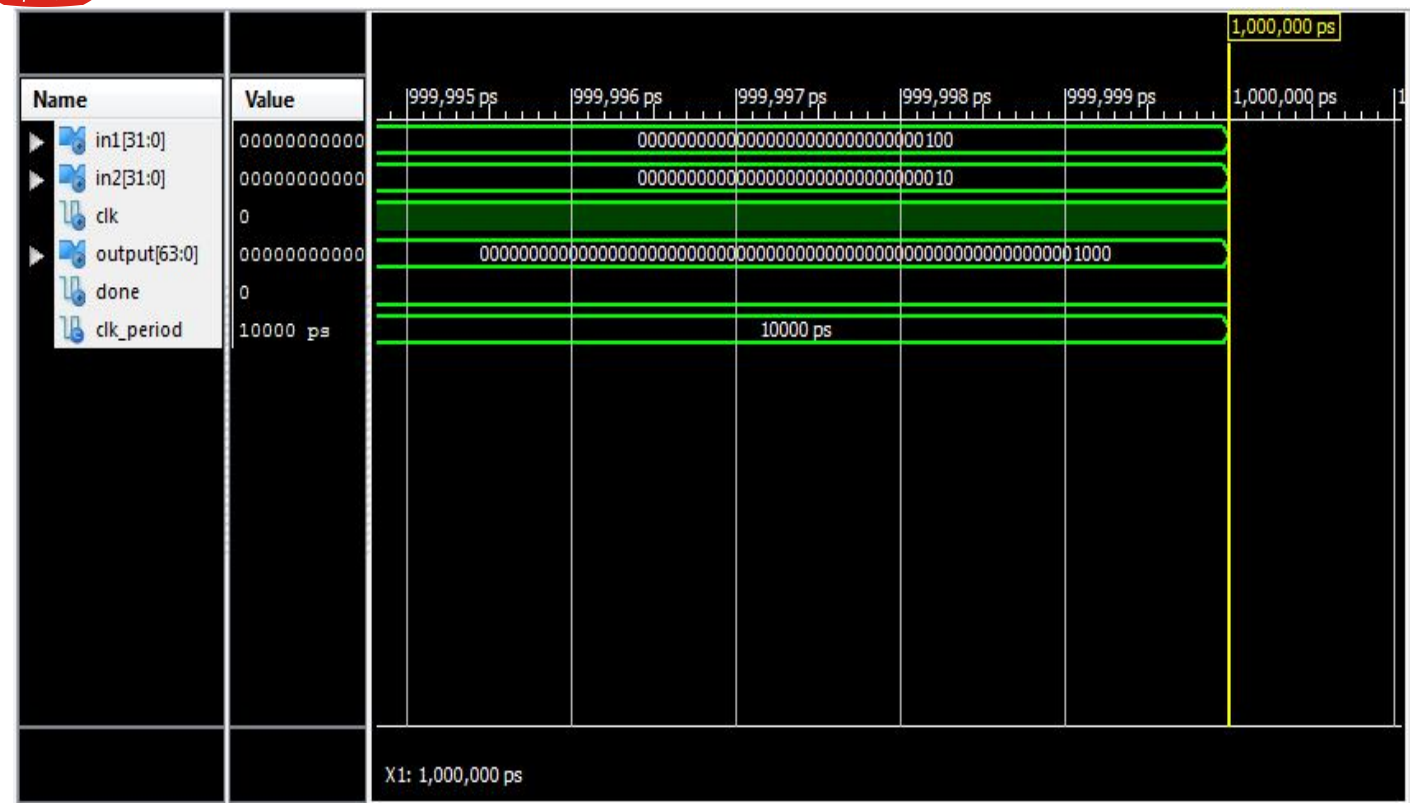

Fig. 3 – Simulation result of Baugh-Wooley Multiplier

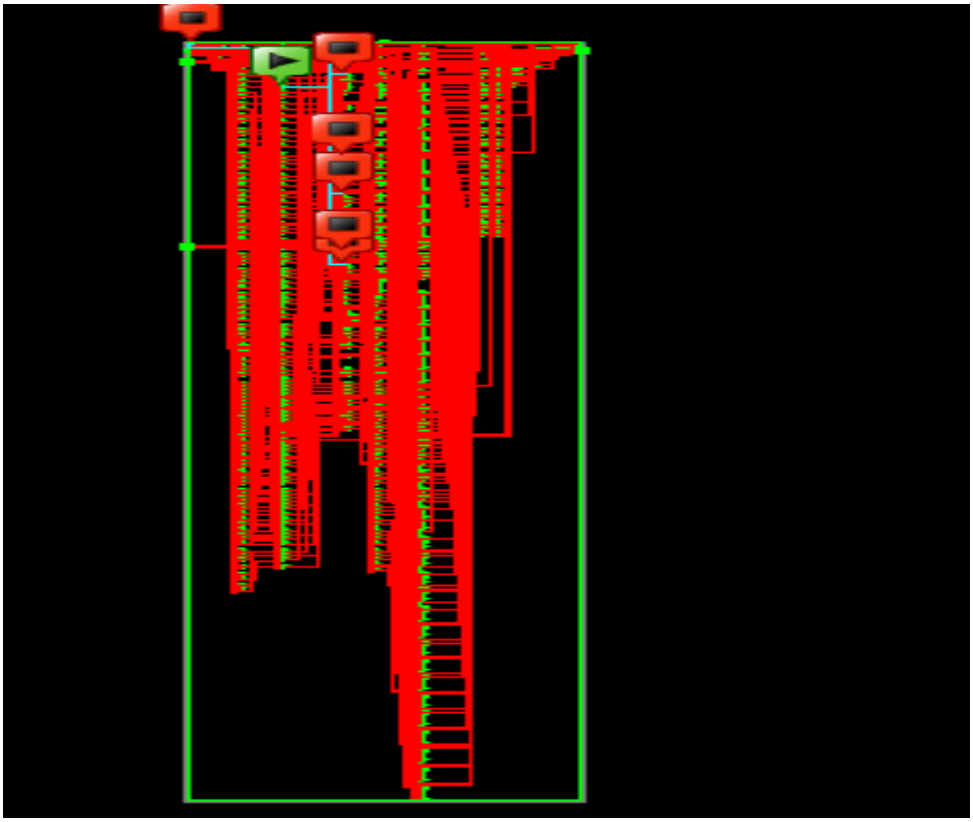

Fig. 4- RTL view of Baugh-Wooley Multiplier

Table 1 –Result of device utilization of Baugh-Wooley Multiplier

REF PAPER	NAME OF MULTIPLIER	DELAY(ns)	POWER(mW)	NO. OF SLICE LUT'S	DEVICE /FAMILY
Proposed Design	Baugh-Wooley	3.584	0.0012	738	Virtex 6 XC6VCX75T FF84-2

Table 2- comparison of existing method with proposed method

REF PAPER	NAME OF MULTIPLIER	DELAY(ns)	POWER(mW)	DEVICE /FAMILY
[12]	Baugh-Wooley	6.496	-	-
[5]	Booth	3.68	9.74	-
Proposed Design	Baugh-Wooley	3.584	0.0012	Virtex 6 XC6VCX75T FF84-2

From this table we conclude that power required for Baugh-Wooley multiplier is less than other existing multiplier.

IV. ACKNOWLEDGMENT

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V. CONCLUSION

The proposed Baugh-Wooley multiplier is simulated using XILINX ISE 14.5. The comparison between proposed and existing multiplier is shown in table 2. From that table we conclude that Baugh-Wooley multiplier have less power than existing multiplier.

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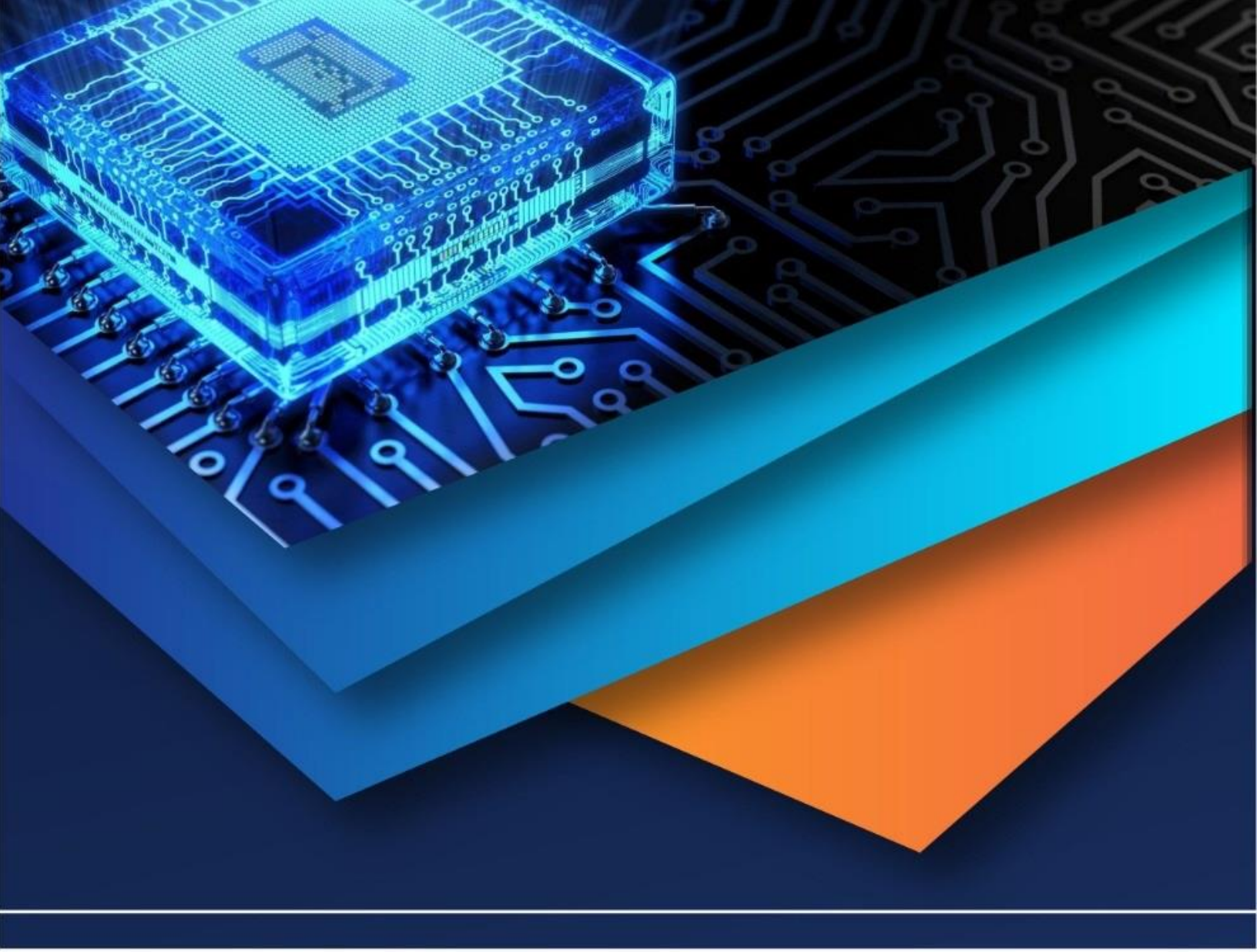

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