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FPGA Implementation of Variable Size 2D DCT

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Abstract: ***The discrete cosine transform (DCT) is basically known as compressing mpeg and jpeg images. The basic reason why it is widely used all over is because of its simplicity and easily computed for faster execution. A lot of research is in progress for faster execution of DCT mean while many of algorithms are also developed for compression of video and images. The ancient technique which is being used for limited sizes of images whether it is Chen's technique or Row column decomposition technique. Hardware implementations are difficult and complicated using these codes, have to go through a lengthy and time taking coding scheme. In this work a new and efficient method is proposed using Simulink system generator due to which codes are automatically generated and hardware implementation has become easy. This architecture is also useful for different size of images. It supports variable size image. The performance analysis of hardware utilization is effectively carried out. The generated codes are generated in Verilog and hardware utilization is carried out by FPGA Virtex 5 xc5vlx110t.***

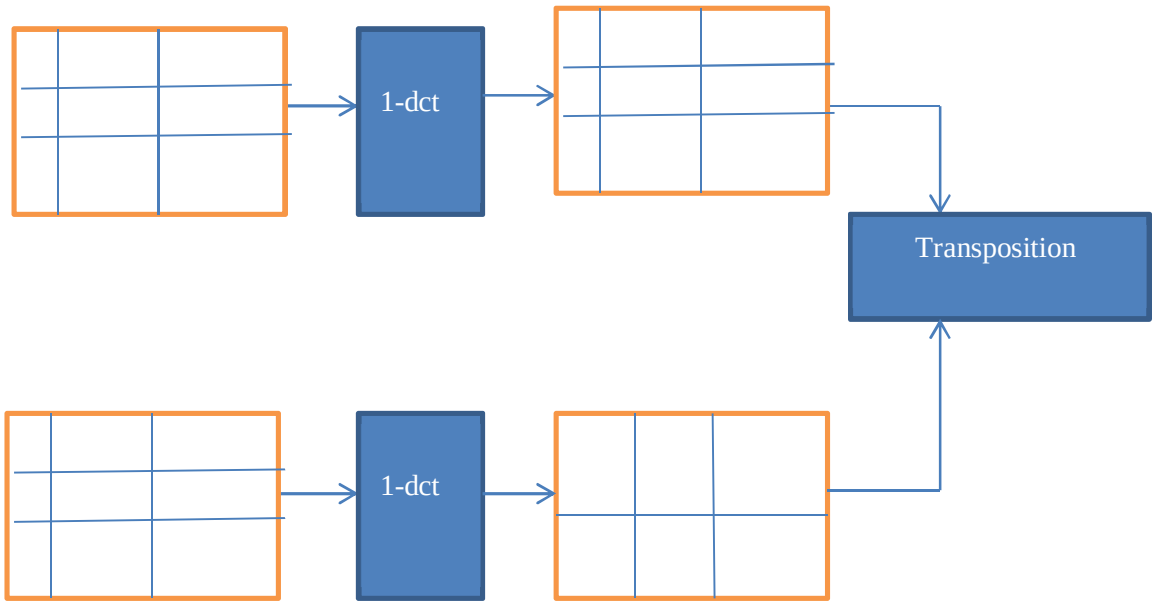
Keywords: DCT, Simulink System Generator, FPGA, Verilog.

I. INTRODUCTION

The discrete cosine transform (DCT) introduced in 1974 by Ahmed *et al.* It has become an intensively useful concept for image, audio filters and video signal processing due to its uses and being adopted in standards like Moving Picture Experts Group (MPEG), Joint Photographic Experts Group (JPEG) [21]. DCT is also playing an important role in digital watermarking [3]. In addition to transforms, the working of the DCT is exactly same to the optimal Karhunen–Loeve Transform (KLT) [11].For the real-time audio, image and video processing requirement, DCT and inverse DCT (IDCT) are needed [6]. Different algorithms are developed for computation of Discrete cosine Transforms [8]-[9]. The 2D DCT is used for achieving high speed, high throughput and very less latency computing architectures [18].

An effective number of compression methods are present, that are being took to a many applications, as: videophones, compact disc and videoconference, multimedia systems. Such applications calculate the bandwidth of transmission line through the compression applied on such application for use [10].DCT and IDCT combines a particular sort of attribute that allows essential image compression. Compression for video audio, pictures are applied in both hardware and software utilizations [2].In any case, the equipment executions are particularly significant for the finish of enormously calculations and may gain a dreadful parcel preferable throughput over programming. Digitalizing the world, a lot of research is going to advance as well save the memory. Image compression has played an important role in commercial photography, industrial imaging & video processing. Image can contain a large data which can further cause complexity in various applications in image processing. Image compression allows mapping of data from a high space to low space. The objective of image compression is to represent an image with few numbers of bits without losing of any bits containing useful information .Image compression transforms the image from time domain into frequency domain which further helps in saving the memory. The most common technique used for transforming is DCT (discrete cosine transforms). It is a kind of lossy transform where transform is done losing of some extravagant information which has no use & occupying large area of memory. As DCT only contains real part where imaginary part is ignored. This dissertation unfolds an efficient way of 2D-DCT with FPGA implementation.

Image block



Transferred image blockFig-1 2D DCT

$$A(u)=\sqrt{2}/nc(u)\sum_{x=0}^{n-1}A(x)\cos\frac{(2x+1)u\pi}{2n} \qquad u=0,\ldots\ldots,n$$

Where $c(u)=2^{-\frac{1}{2}}$ for u=0

=1 otherwise

Equation-1(1D DCT)[3]

For calculating 2-DCT

$$A(u,v)=\frac{\sqrt{2}}{n}*\sqrt{2}/m\sum_{i=0}^{n-1}a(i)\sum_{i=0}^{m-1}a(j).cos\frac{(2x+1)u\pi}{2n}.cos\frac{(2x+1)v\pi}{2m} \text{ for } 0<n<N-1$$

=0, otherwise

Equation-2(2D DCT)[4]

A. Hardware Design

1) Xilinx System Generator: Xilinx System Generator (XSG) is an Integrated Design Environment (IDE) for FPGAs within the ISE design suite, which enables using SIMULINK, for a model based design. In real time implementation 2D DCT image processing algorithm can be carried with FPGA boards. Here implementation of 2D DCT is done with Virtex 5 xc5vlx110t device and least resources are used. Once the design is modeled in XSG, Verilog or VHDL code can be generated automatically.

2) *Core Gnerator:* For hardware simulation the architecture has to be converted to synthesizable code. The entire model is converted to HDL code and then bit file is generated from it. .For this model had to be converted to JTAG hardware and software co- simulation. The block shown below in Fig shows the parameters for target device and generate (*.bit) file is generated.

3) *Design flow for 2D DCT*

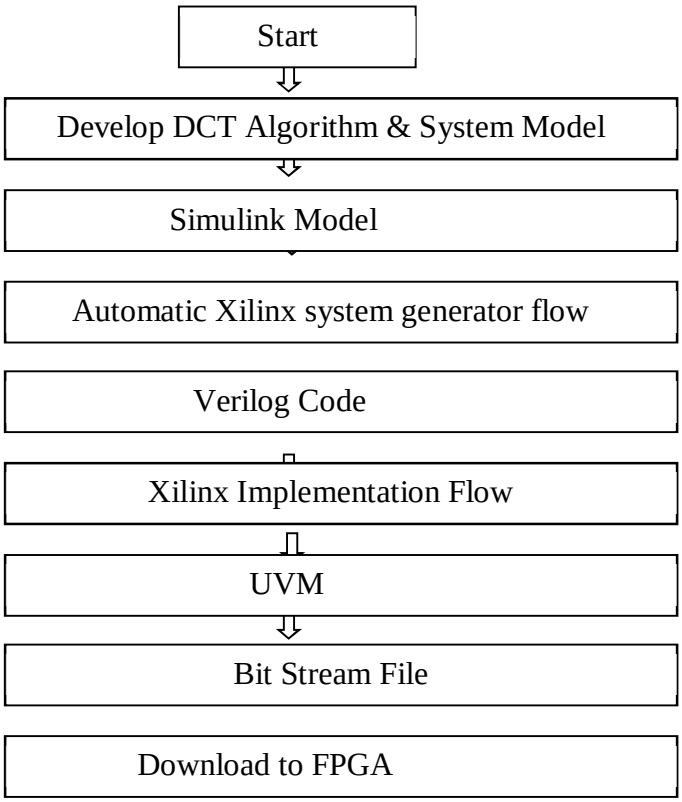


Fig-4 Flow chart for co-simulation

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II. IMAGE PROCESSING ALGORITHM FOR COMPRESSION

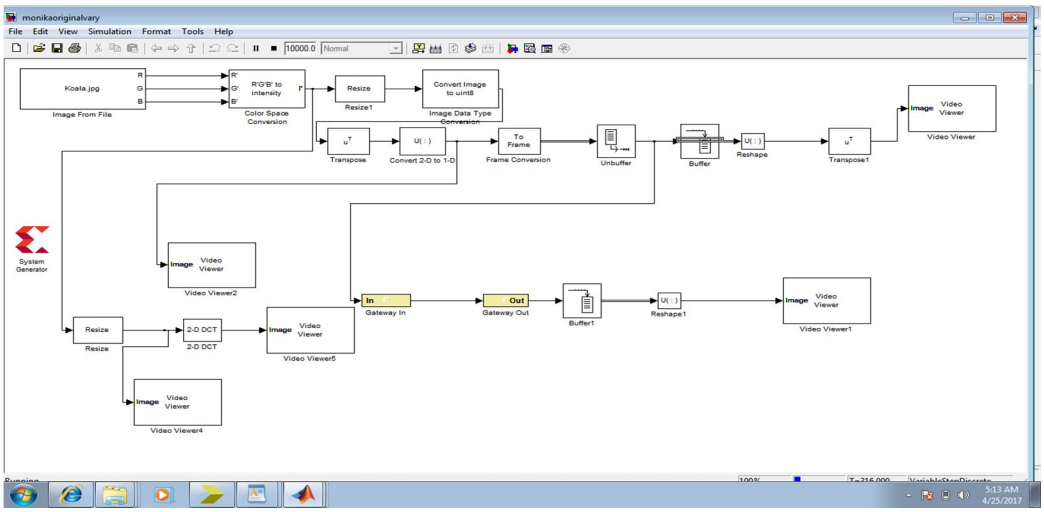


Fig-5 Simulink model for image compression

III. RESULT

Image-1

Image-2

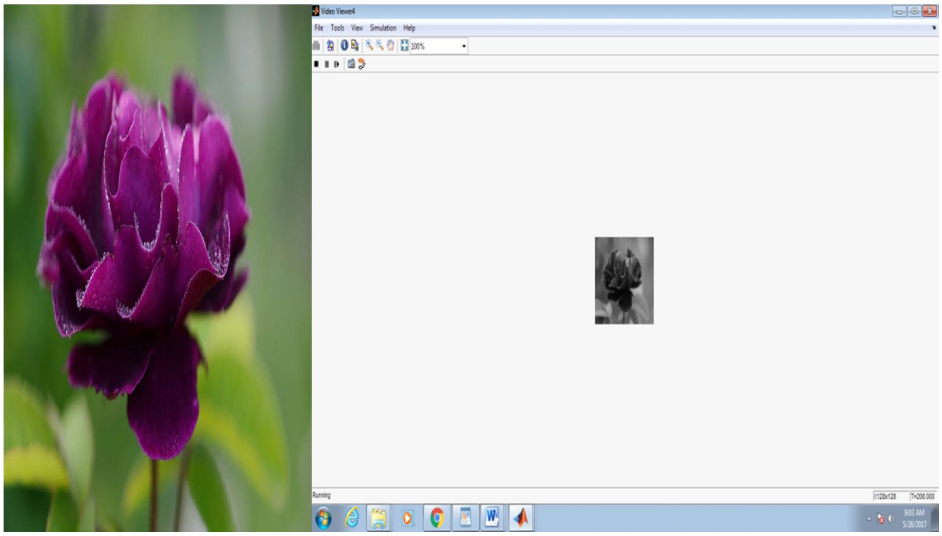
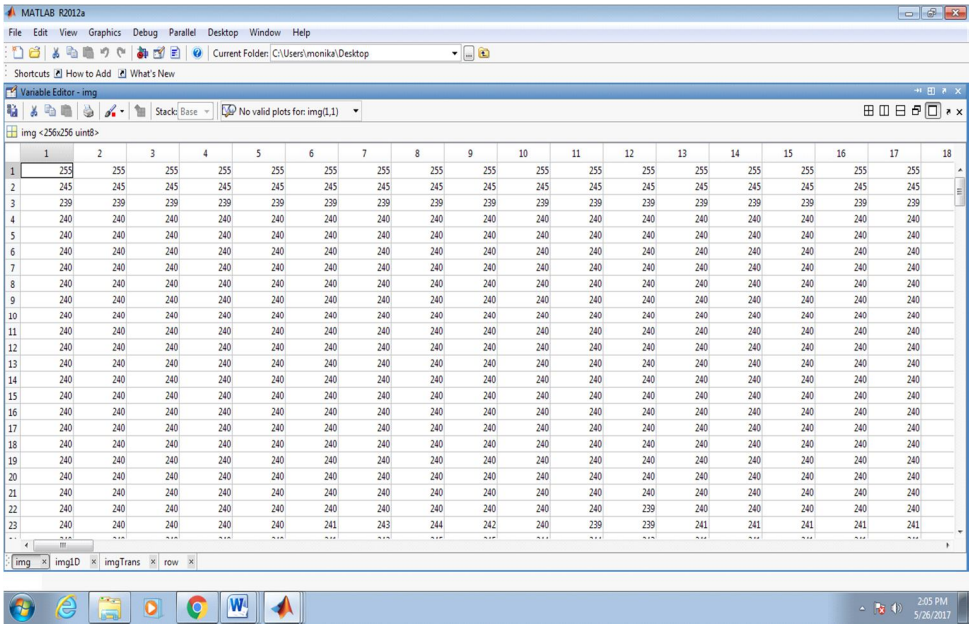


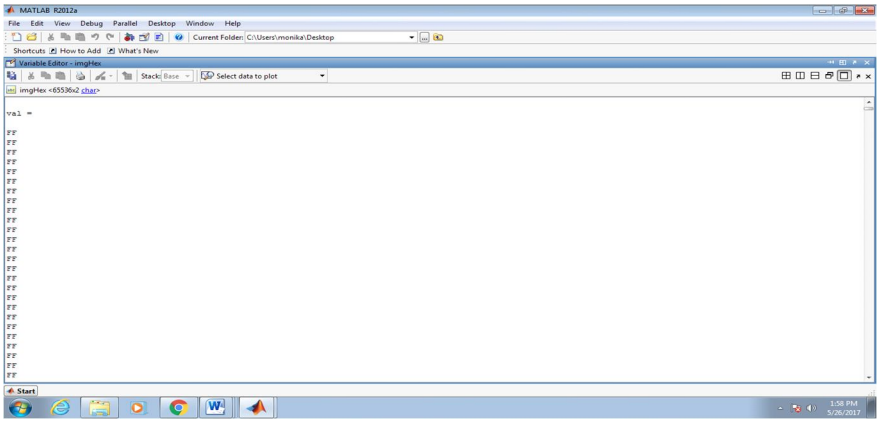
Image-3

IV. DISPLAYING THE IMAGE

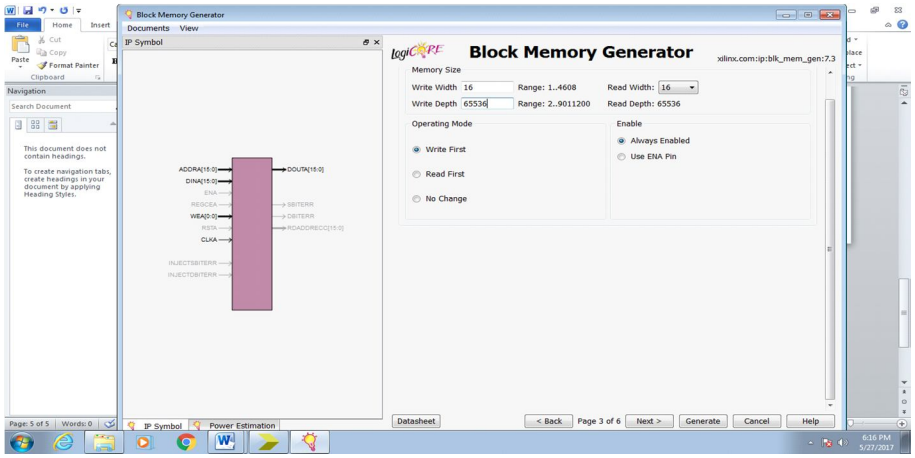


Original image pixel

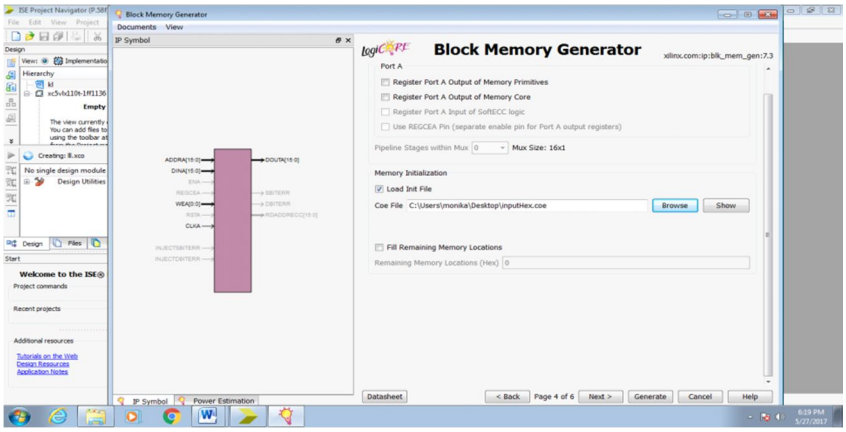
A. Convert the Pixel Into Hex File



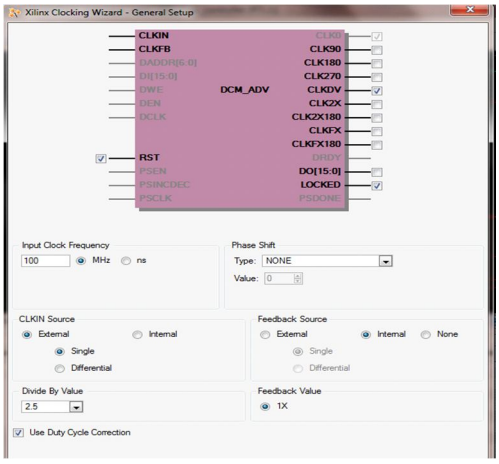
Hex file with extension coeRead the coe file by setting the write depth.



Width and Depth specification



Then click on generate. Xcw and .v file are created, synthesizing .v file we've ngc file. Copy these file to the main module. Generate DCM clock.



B. DCM Clock

The DCM block (Digital clock manager) can be made using IP core and the clocking frequency can also be setup.

The other ports can be easily be enabled by just checking it. As shown above the DCM block is designed at 100/2.5 MHz. The phase shift value is given none and clkdv is selected in the block.

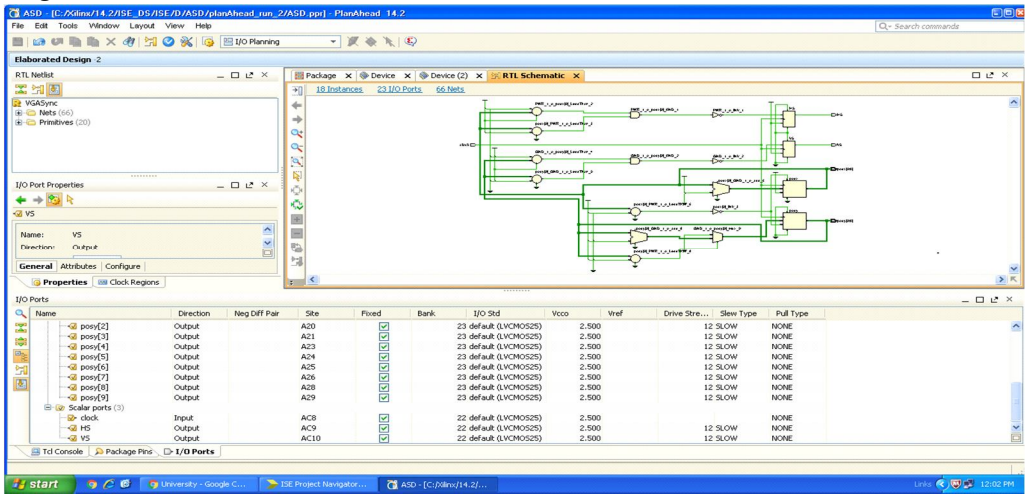


Fig-6. RTL Schematic

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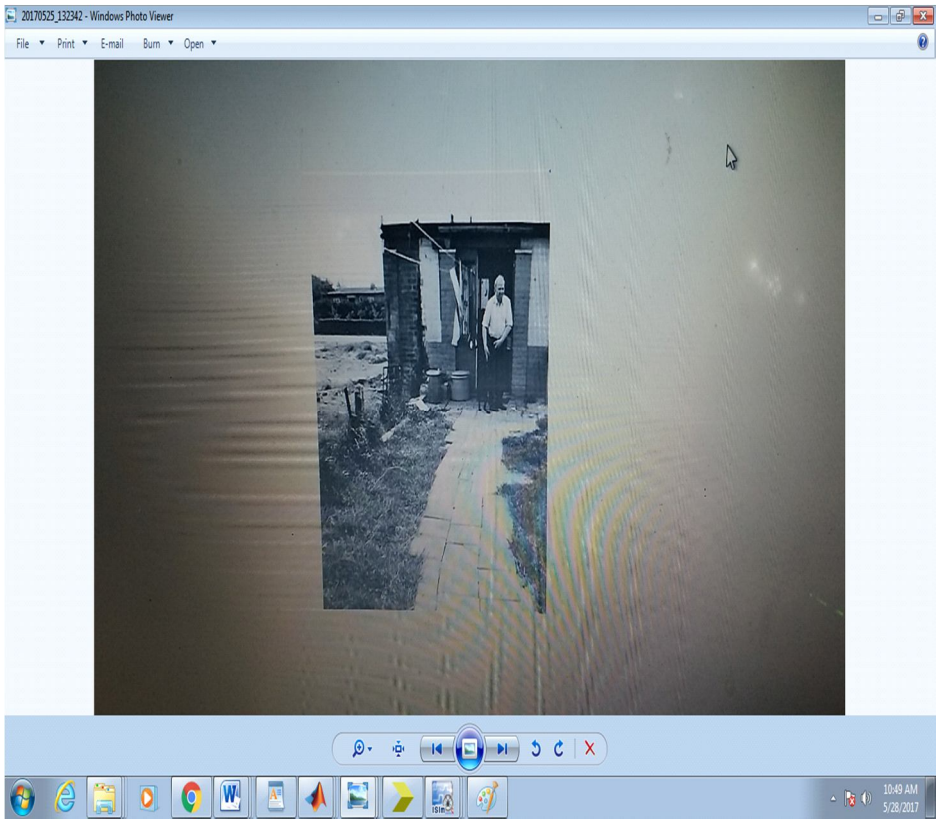


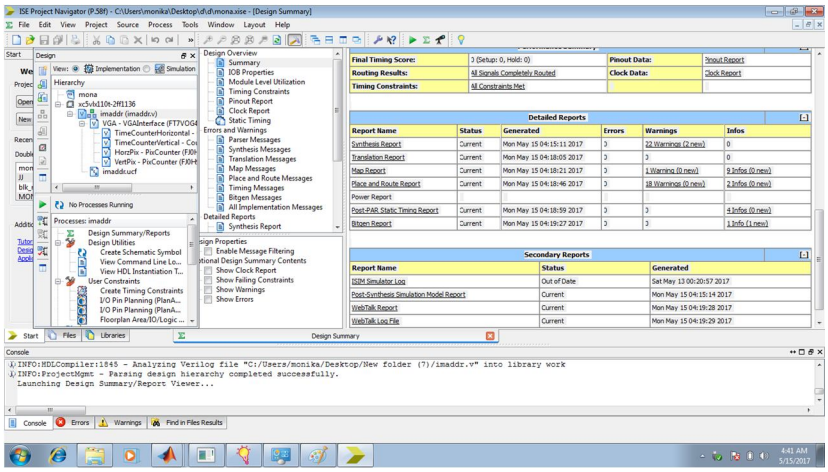


Fig-8 synthesis report

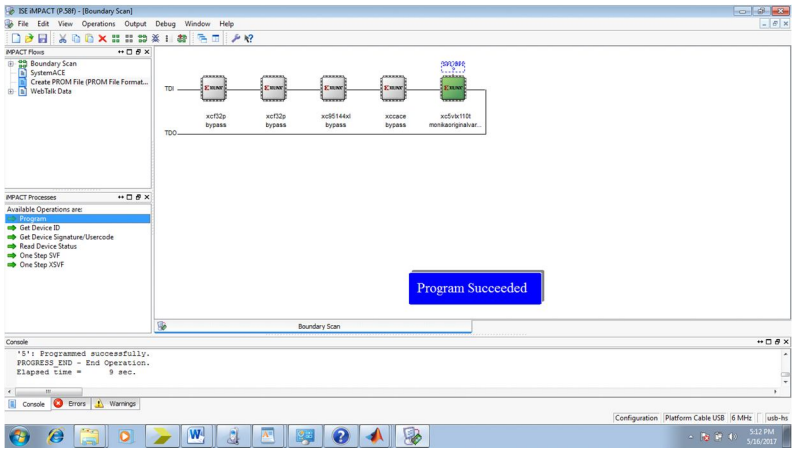
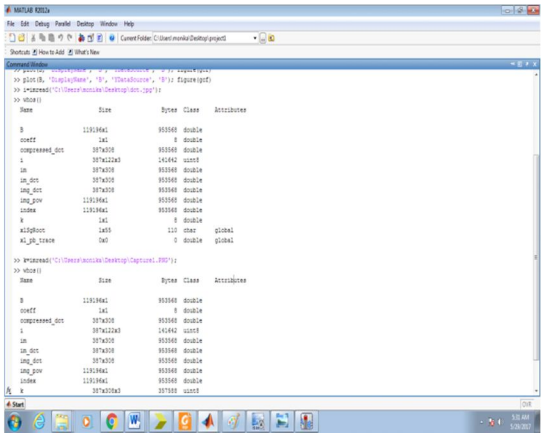


Fig-9 FPGA simulation



Compressed image detail

V. CONCLUSION

The DCT is widely used for compression system. In comparison with different transform which uses lots of multipliers and adder, It needs less multiplier and adders. The total power used in this project is 1.042 w. no. of slices used 1out of 69120. Only 1% is utilized here. This is comparatively low to the previous technique of implementing 2D DCT. 8 luts are used out of 69,120.

The utilization is 1%. Which is very less than popular algorithm of chen's of implementing 2D DCT and other algorithm. Total fan out is 1.39 and 34.5% compression is done using this technique.

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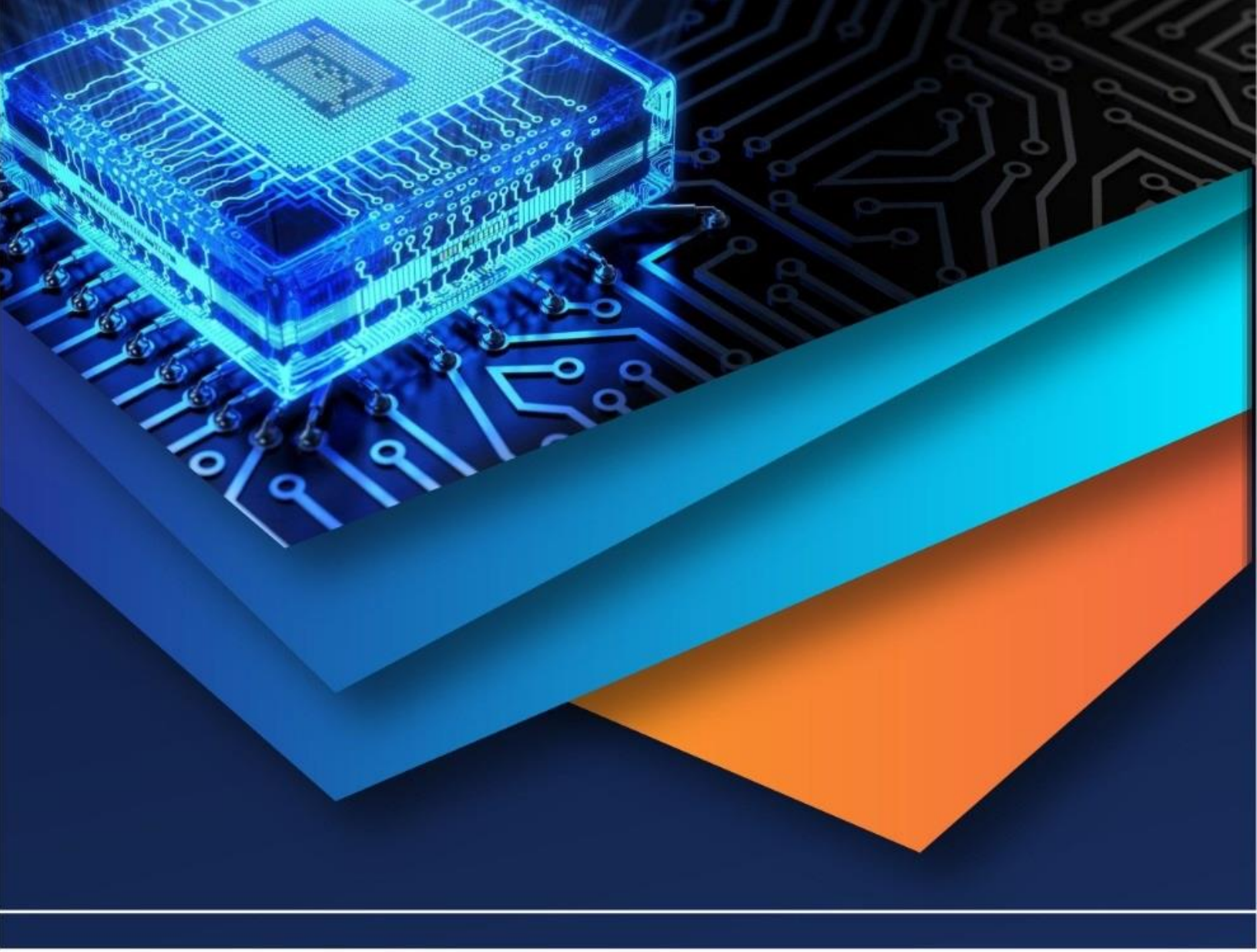

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