iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VII **Month of publication:** July 2017

DOI:

www.ijraset.com

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887
Volume 5 Issue VIII, July 2017- Available at www.ijraset.com

Simulation of a Novel Multi-Level Inverter Topology for Induction Motor Drive Applications

Ravi Kumar Kanaparthi[1] , Chandra Sekhar Gujjarlapudi[2]
[1]*Department of Electrical and Electronics Engineering, Aravindhaksha Educational Society's Group of Institutions*
[2]*Department of Electrical and Electronics Engineering, Sri Mittapalli College of Engineering*

Abstract: This paper presents a novel multilevel inverter for inductor motor drive applications. The use of MLIs in medium and high power applications are increasing due to reduced voltage stress across the switches and lower total harmonic distortion (THD) of the output waveform. But the conventional MLIs requires more number of switches as the level increases for reducing the THD of the output waveform. This paper presents a new MLI inverter topology with reduced number of power electronic components. The proposed inverter produces thirteen level output voltage using only 9 switches and a diode. For generating thirteen level output voltage conventional Hbridge MLI uses 12 switches, which increase the cost as well as switching losses. This paper presents the comparison between cascaded H-bridge MLI and symmetrical and asymmetrical configuration of the proposed inverter. Finally induction motor fed from the proposed MLI is simulated in MATLAB/SIMULINK environment and the corresponding results are presented.

Keywords— Induction motor, Multilevel inverter, symmetrical configuration and Total harmonic distortion, Voltage source inverter.

I. INTRODUCTION

The use of induction motors (IMs) are increasing day by day in industry sector for high power applications. The main advantages of IMs are rugged in construction, easy maintenance, less cost and sufficiently high efficiency, etc. Speed control of IM requires a suitable inverter to change the voltage and frequency [1] applied to it. Normally we do two stage conversion, i.e. convert the ac power from supply mains to dc (rectification) and then it is converted to again ac (inversion) to control the speed of the machine. Generally we use a voltage source inverter (VSI) for this job. But the conventional H-bridge VSI produces a square wave output voltage waveform which contains infinite number of odd
harmonics. For getting the sine wave output we prefer PWM based inverter, but the main disadvantage of PWM inverter [2] is switching losses are high and also it is limited to low power applications. For medium and high power applications, we are using multilevel inverters (MLI) [3-6]. The main advantage of MLI is that the output voltage is almost nearer to sine wave. The other advantages of MLI are reduced dv/dt stress across the switches, and less THD. Generally multilevel inverters are categorized into three types depending upon their configuration. They are Diode clamped MLI, Flying capacitor MLI, and Cascaded H-bridge MLIs. The main problem associated with Diode
clamped MLIs [7] is that requirement of extra diodes in addition to the switches which increase the cost. In flying capacitor MLIs [8-10], control is complicated and large numbers of capacitors are expensive as the level increases. Cascaded H-bridge MLI [11] are more expensive as the level increases and also it requires separate dc sources. To overcome the above disadvantages this paper proposes a new multilevel inverter topology with fewer switches compared to conventional MLIs. Finally the induction motor fed by the proposed MLI is presented in this paper.

II. CASCADED H-BRIDGE MLI TOPOLOGY

The general structure of cascaded H-bridge multilevel inverter in symmetrical configuration is shown in the figure 1. Each H-bridge uses four switches. For N number of levels level, the no of H-bridge required is given by the following formula,

$$\text{Number of levels} = 2N + 1$$

Where,
N = number of H-bridges
Here each H-bridge is connected in series so that the outputs of each bridge are added up to get the required output level [12-13]. For generating seven level output voltage, we require three H-bridges in symmetrical configuration. So it requires 12 switches to generate seven level output voltage which increases the switching losses and cost also.

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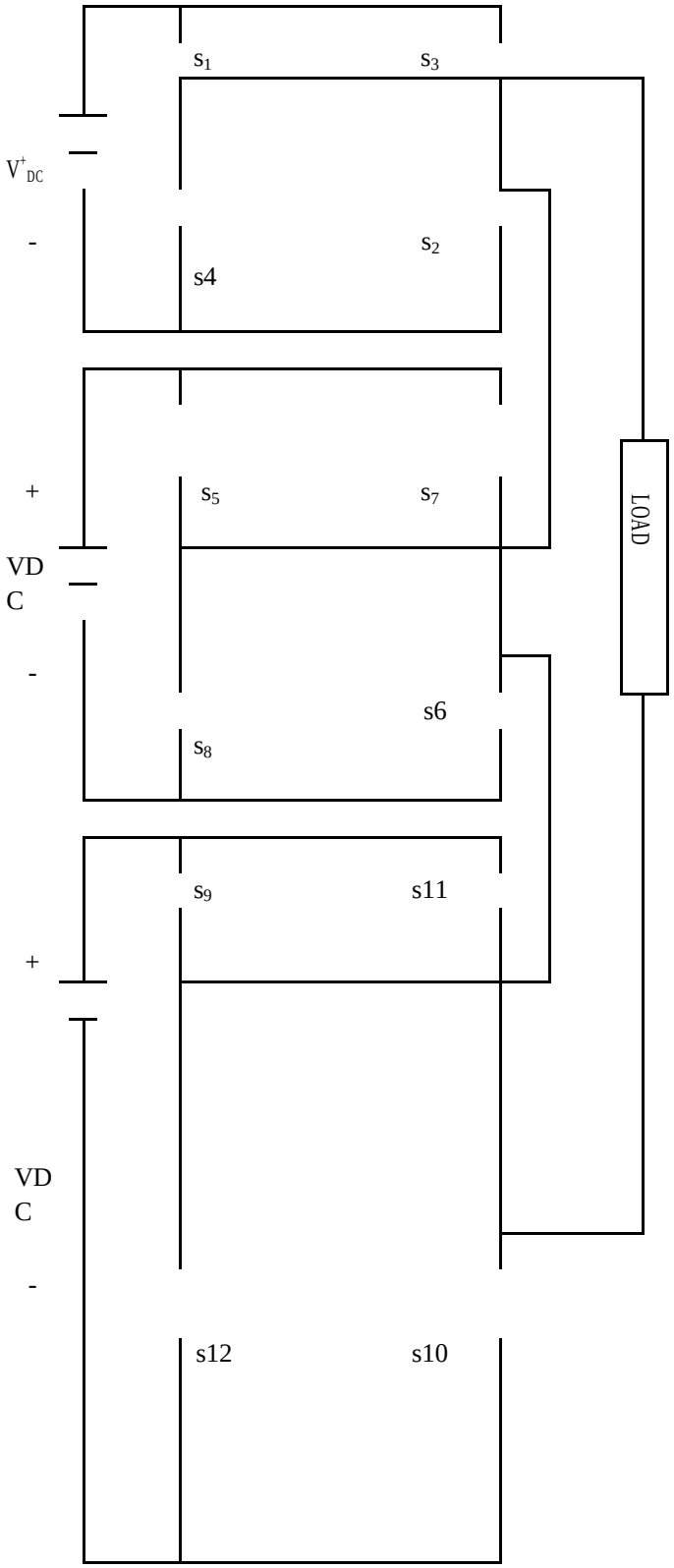

Figure 1: Symmetrical configuration of cascaded H-bridge multilevel inverter

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Asymmetrical configuration of cascaded H-bridge multilevel inverter is shown in figure2.

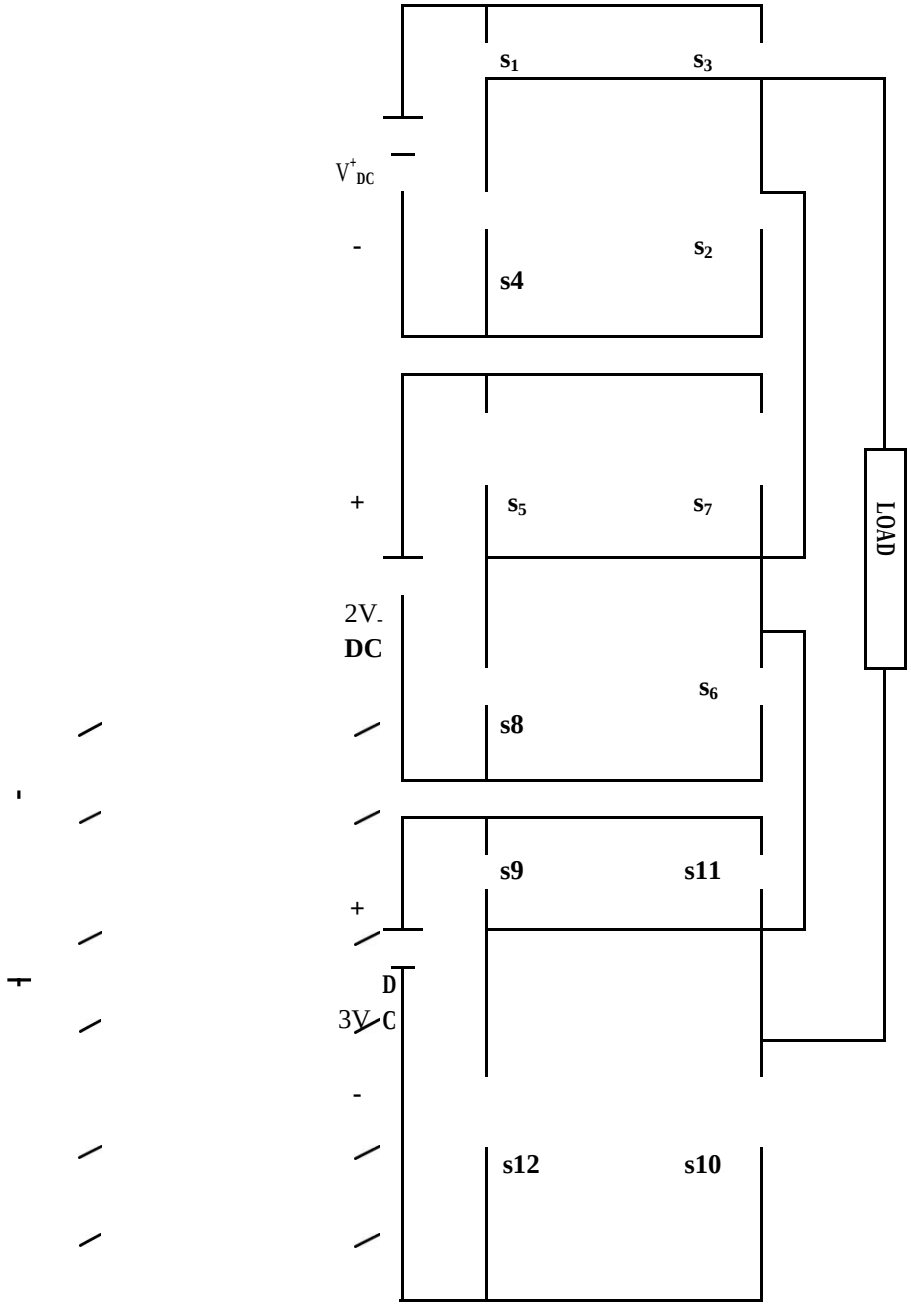

Figure 2: Asymmetrical configuration of cascaded H-bridge multilevel inverter

It requires three H-bridges with three different dc input voltages to generate thirteen level output voltage. It also uses twelve switches to get the required output voltage
which means switching losses and cost also high. To avoid the above problems this paper presents a new multilevel inverter topology with fewer switches to generate the required output voltage.

III. PROPOSED MULTILEVEL INVERTER TOPOLOGY

A. Symmetrical configuration

The following figure 3 shows the symmetrical configuration of the proposed MLI topology.

s VDC

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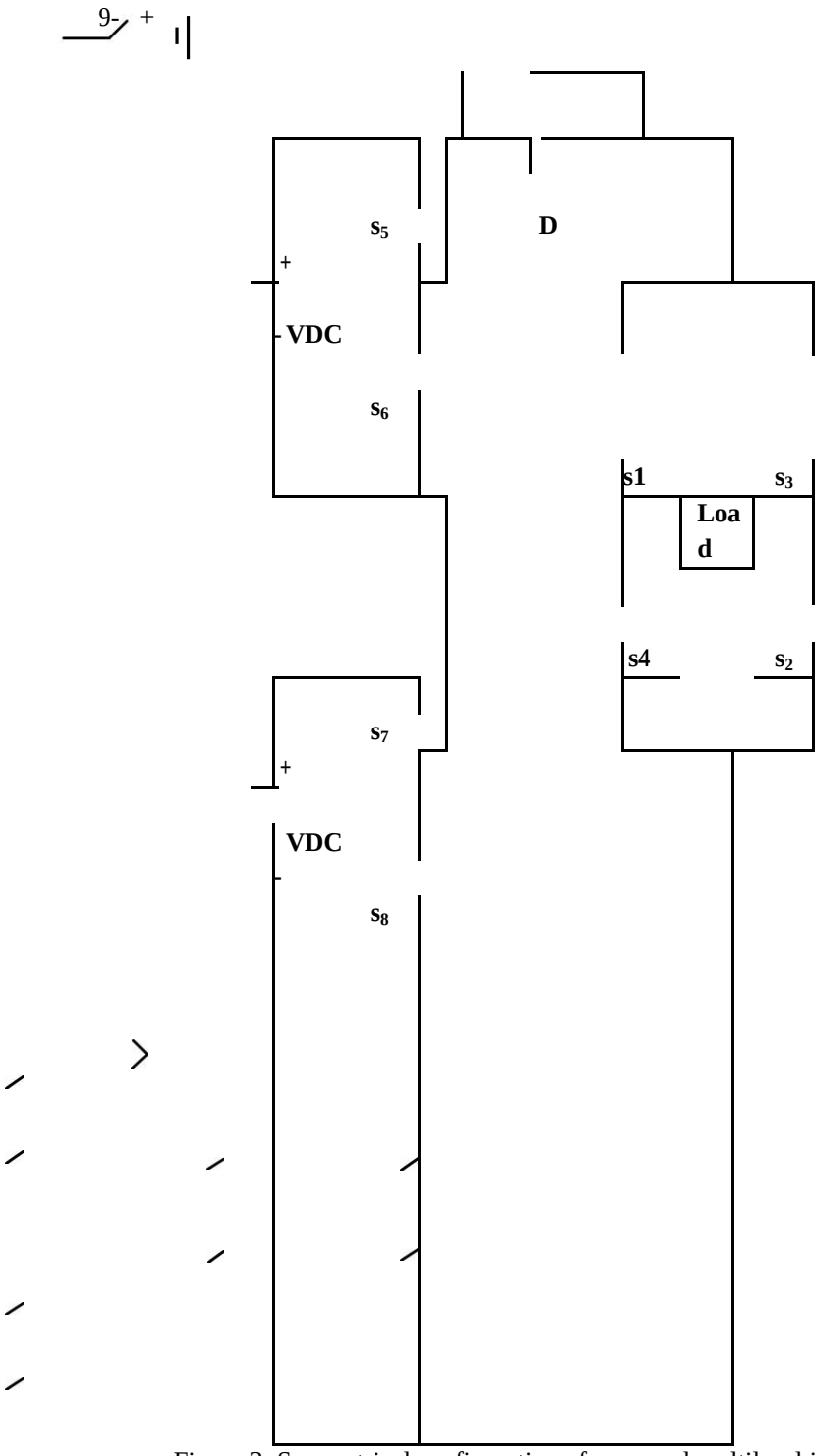

Figure 3: Symmetrical configuration of proposed multilevel inverter

It consist of nine switches $S_{1,}$ $S_{2,}$ S_3 … $S_{9\ to}$ achieve seven level output voltage. Compared to symmetrical configuration of cascaded H-bridge MLI (uses 12 switches), the proposed multilevel inverter topology uses less switches. Since the switches are less, the switching losses and cost are low. The following figure 4 shows the ideal waveform of seven level output voltage.

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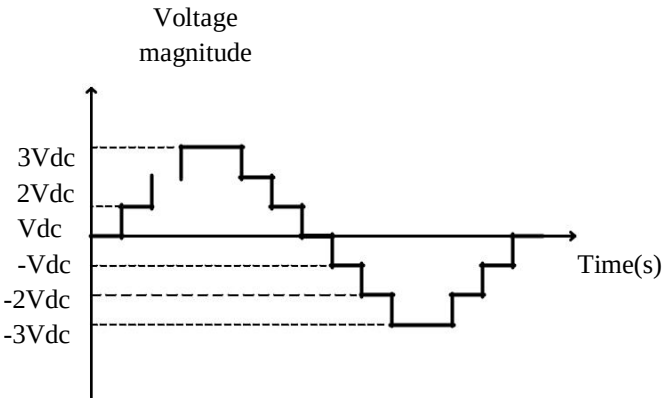

Figure4. Ideal seven level output voltage waveform

The output voltage waveform consists of seven levels ± 3Vdc, ± 2Vdc, ± Vdc and 0. The following table I shows the switching pattern for the proposed MLI in symmetrical configuration.

Table I: Switching pattern for proposed Symmetrical MLI

S1	S2	S3	S4	S5	S6	S 7	S8	S9	Voltage level
1	1	0	0	1	0	0	1	0	+Vdc
1	1	0	0	1	0	1	0	0	+2Vdc
1	1	0	0	1	0	1	0	1	+3Vdc
0	1	0	1	0	0	0	0	0	0
0	0	1	1	1	0	0	1	0	-Vdc
0	0	1	1	1	0	1	0	0	-2Vdc
0	0	1	1	1	0	1	0	1	-3Vdc

B. Asymmetrical Configuration

Asymmetrical configuration means the use of different dc voltage ratings. More number of levels can achieved with less number of switches is the main advantage of asymmetrical configuration. The following figure 5 shows the asymmetrical configuration of proposed multilevel inverter.

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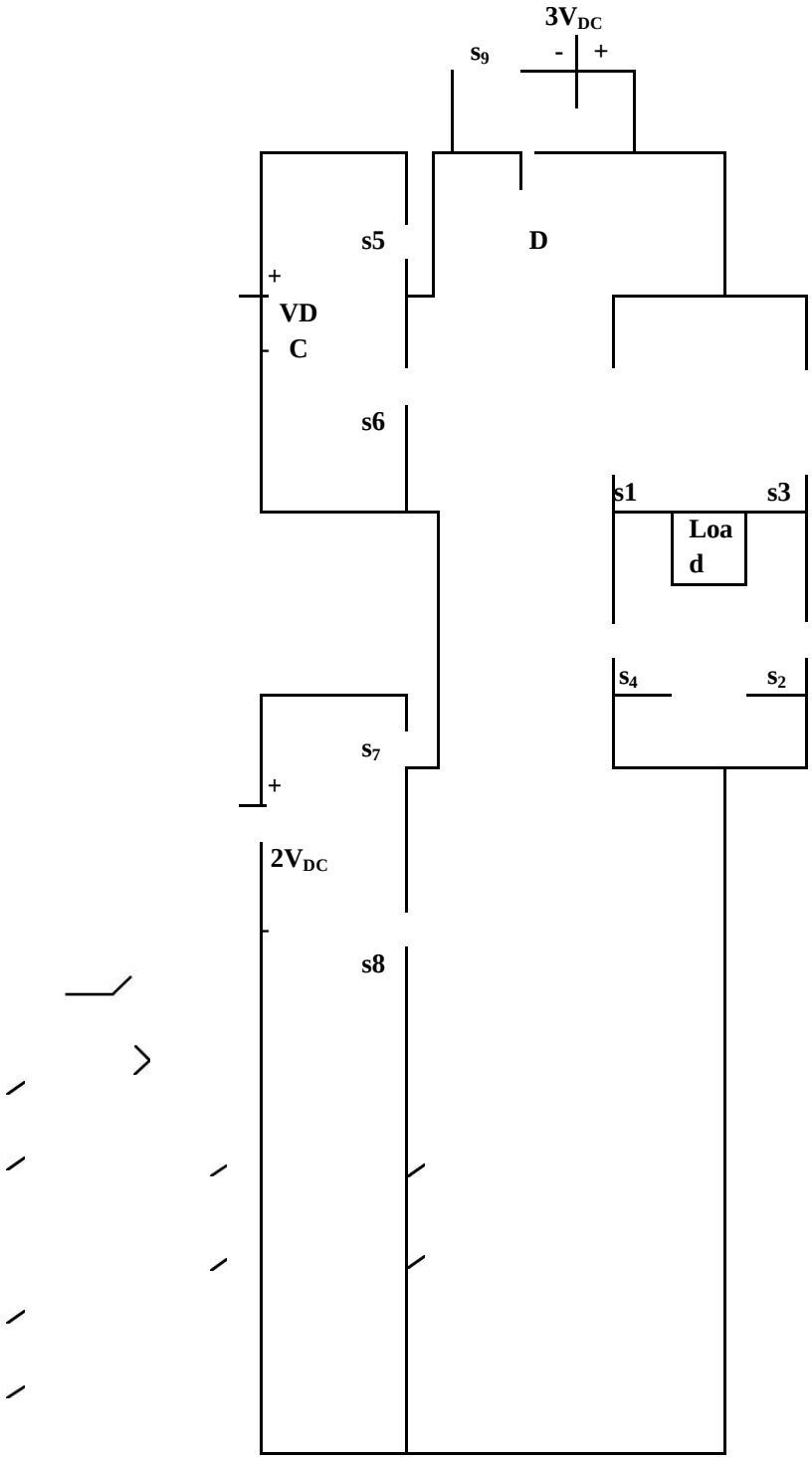

Figure 5: Asymmetrical configuration of proposed multilevel inverter

When compared to the asymmetrical configuration of cascaded H-bridge MLI, the proposed asymmetrical MLI uses only nine switches to generate thirteen level output voltage. The following figure 6 shows the ideal waveform of thirteen level output voltage.

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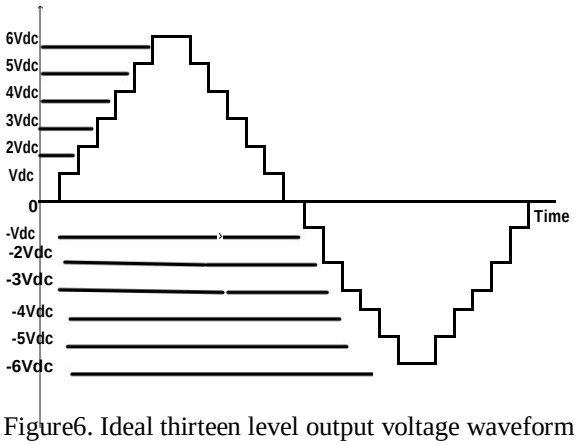

Figure6. Ideal thirteen level output voltage waveform

The output waveform consists of 13 levels: ± 6Vdc, ± 5Vdc, ± 4Vdc ± 3Vdc, ± 2Vdc, ± Vdc and 0. The following table II shows the switching pattern for the proposed MLI in asymmetrical configuration.

Table II: Switching pattern for proposed Asymmetrical MLI

S1	S2	S3	S4	S5	S6	S7	S8	S9	Voltage level
1	1	0	0	1	0	0	1	0	+Vdc
1	1	0	0	0	1	1	0	0	+2Vdc
1	1	0	0	1	0	1	0	0	+3Vdc
1	1	0	0	1	0	0	1	1	+4Vdc
1	1	0	0	0	1	1	0	1	+5Vdc
1	1	0	0	1	0	1	0	1	+6Vdc
0	1	0	1	0	0	0	0	0	0

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0	0	1	1	1	0	0	1	0	-Vdc
0	0	1	1	0	1	1	0	0	-2Vdc
0	0	1	1	1	0	1	0	0	-3Vdc
0	0	1	1	1	0	0	1	1	-4Vdc
0	0	1	1	0	1	1	0	1	-5Vdc
0	0	1	1	1	0	1	0	1	-6Vdc

Power electronic components required for the proposed MLI and cascaded H-bridge multilevel inverter is shown in the following table III.

Table III: Comparison between proposed MLI and cascaded H-bridge multilevel inverter in symmetrical configuration

Type of MLI	**Number of switches for 7-level output voltage**
Cascaded H-bridge MLI (symmetrical)	**12**
Proposed MLI (symmetrical)	**9**

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IV. INDUCTION MOTOR FED BY THE INVERTER

Speed control of induction motor can be achieved in three different ways. First one is to control the voltage applied to the stator of the IM, but this method gives the poor performance. Second method is to control the frequency of voltage, but this method may push the IM into saturation. In order to address the above concerns, third method known as V/F control, in which both voltage and current has to be varied. For this purpose we need an inverter to change the both frequency and voltage applied to IM. Conventional inverters can do this job, but these are having so many problems such as high THD, more switching losses and low efficiency. For eliminating the above disadvantages this paper proposes a new multilevel inverter topology. The following figure shows 7 the inverter fed induction motor.

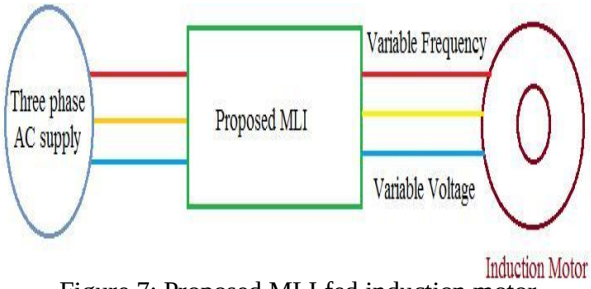


Figure 7: Proposed MLI fed induction motor

The following table shows the cost data for the proposed MLI topology and cascaded H-bridge MLI topology.

Type of MLI	No of switches(IGBT) used	Cost of switches(IGBT) used in rupees	No of DC sources Required	Cost of DC sources Required
Proposed MLI (Symmetrical Configuration)	9	9*200= 1800/-	3	3*600 = 1800
Cascaded H-bridge MLI (Symmetrical Configuration)	12	12*200=2400/-	3	3*600 = 1800

From the above table, the cost of IGBT switches used in the proposed MLI is less compared to cascaded MLI topologies, where as the cost of the DC sources is same for both the topologies.

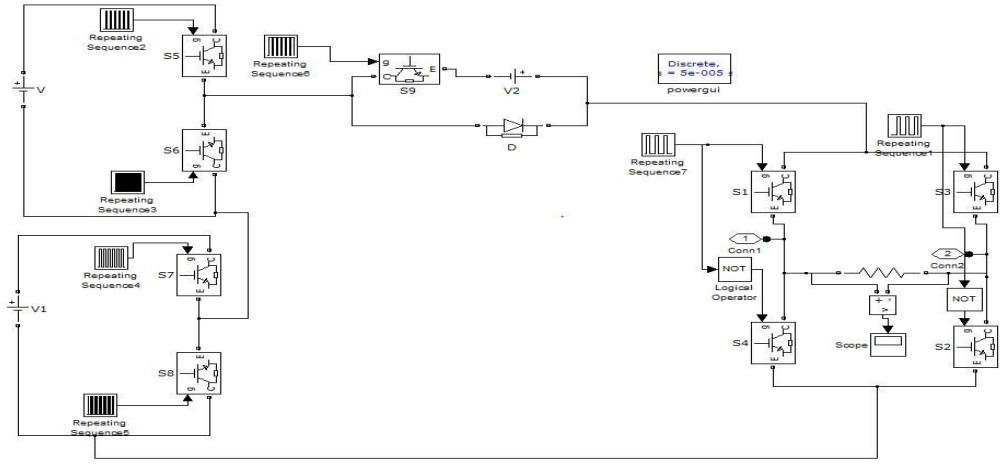


Figure8: Matlab/Simulink diagram of proposed seven level MLI in symmetrical configuration.

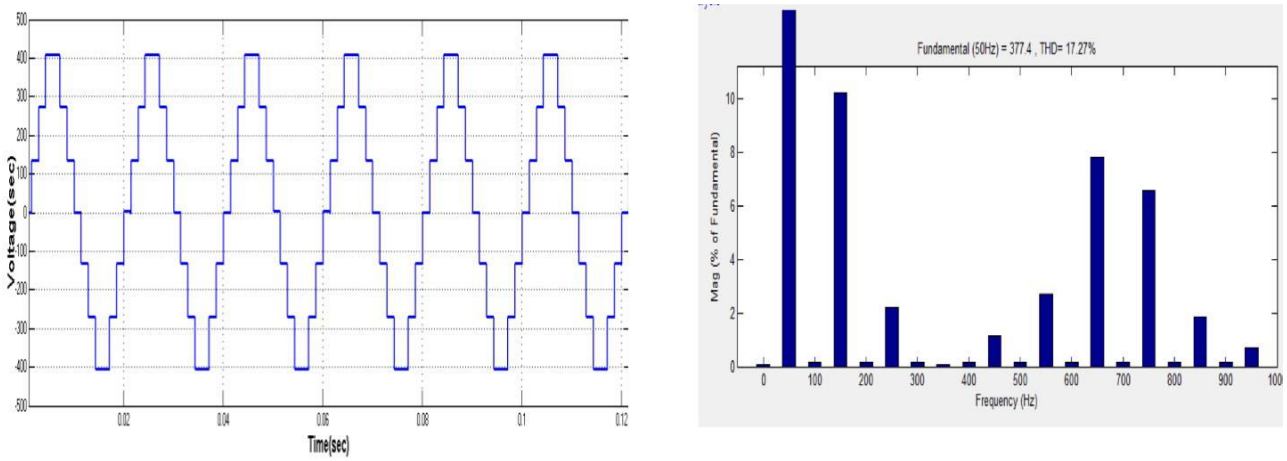


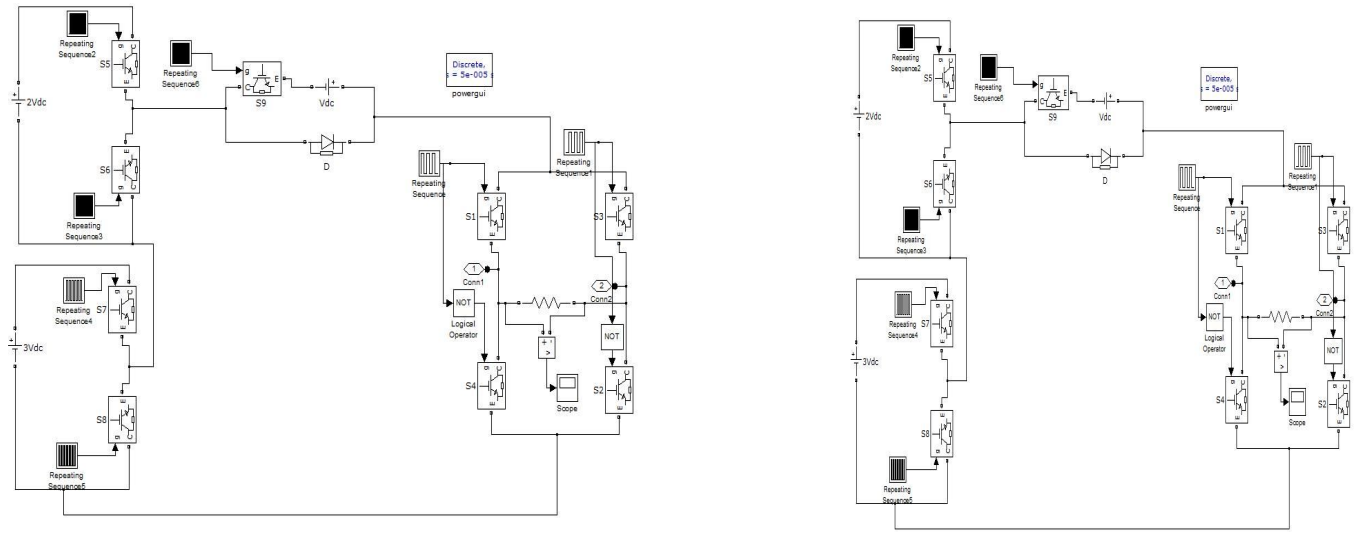
Figure9: Output voltage waveform and harmonic spectrum of proposed 7-level MLI (Asymmetrical topology)

V. INVERTER LOSSES

Mainly, two kinds of losses (i.e., conduction and switching losses) are associated with the switches [14]. As the switches reduced these losses are also reduced. In the proposed MLI topology, we are using nine switches which are less compared to cascaded MLI topology. Hence switching losses are less for the proposed MLI.

VI. SIMULATION RESULTS

Matlab/Simulink diagram of proposed seven level MLI (Symmetrical configuration) and its output voltage wave form is shown in the following figures 8 and 9. From figure 9 , the wave form contains seven level output voltage and here the inverter uses nine switches. The proposed seven level MLI's harmonic spectrum is shown in figure 9 and THD value for this inverter is 17.27%. Matlab/Simulink diagram of proposed thirteen level MLI
(Asymmetrical configuration) and its output voltage wave form is shown in the following figures 10 and 11. From the figure 11, the wave form contains thirteen level output voltage and here the inverter uses nine switches. The proposed thirteen level MLI's harmonic spectrum is shown in figure 11 and THD value for this inverter is 14.21%%. Finally the proposed MLI applied to a induction motor is shown in the figure 12. The corresponding waveforms (phase voltages, stator currents, rotor speed and the electromagnetic torque) are shown in the figures 13 and 14 respectively.



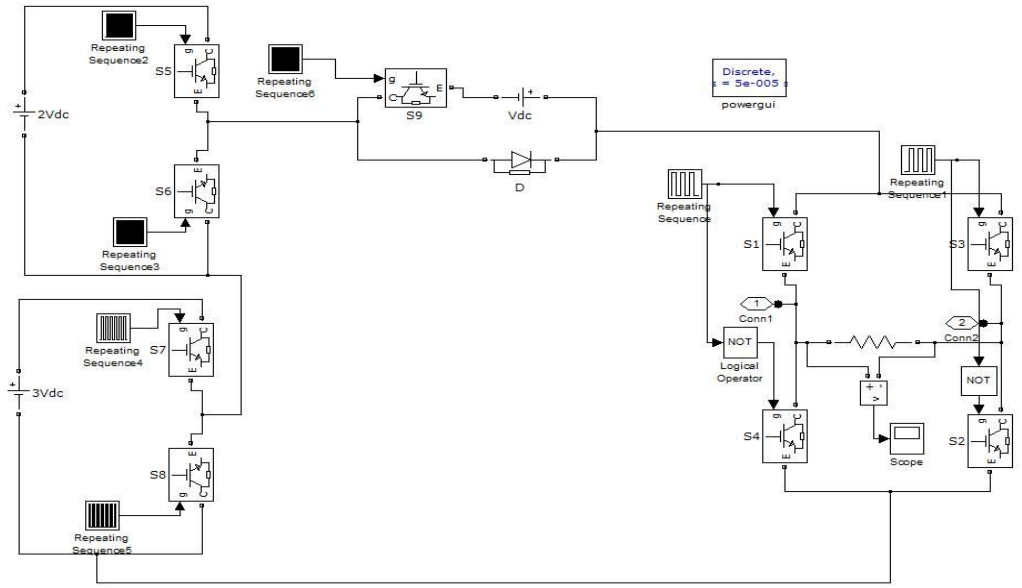


figure10: Matlab/Simulink diagram of proposed thirteen level MLI in Asymmetrical configuration

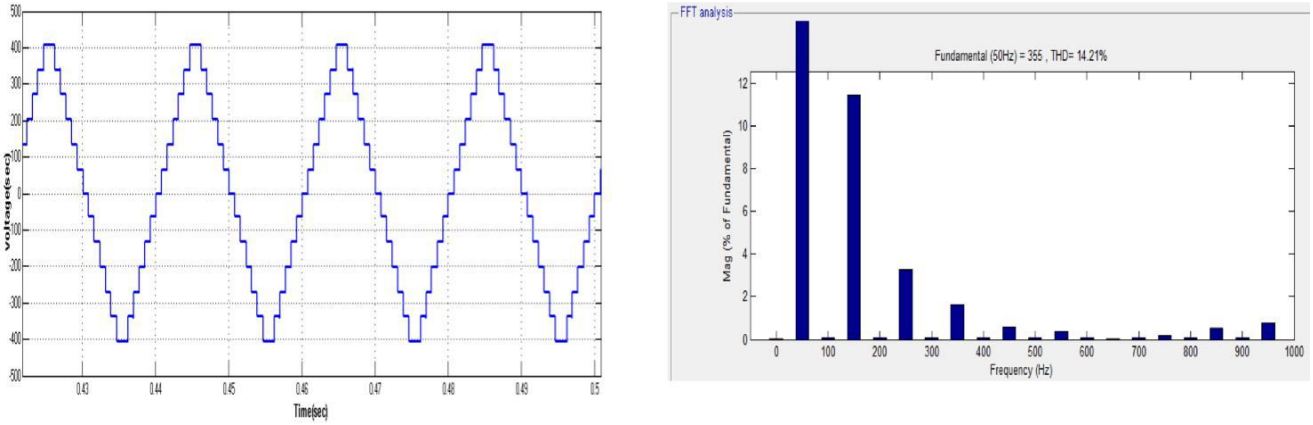


Figure11: Output voltage waveform and harmonic spectrum of proposed 13-level MLI (Asymmetrical topology)

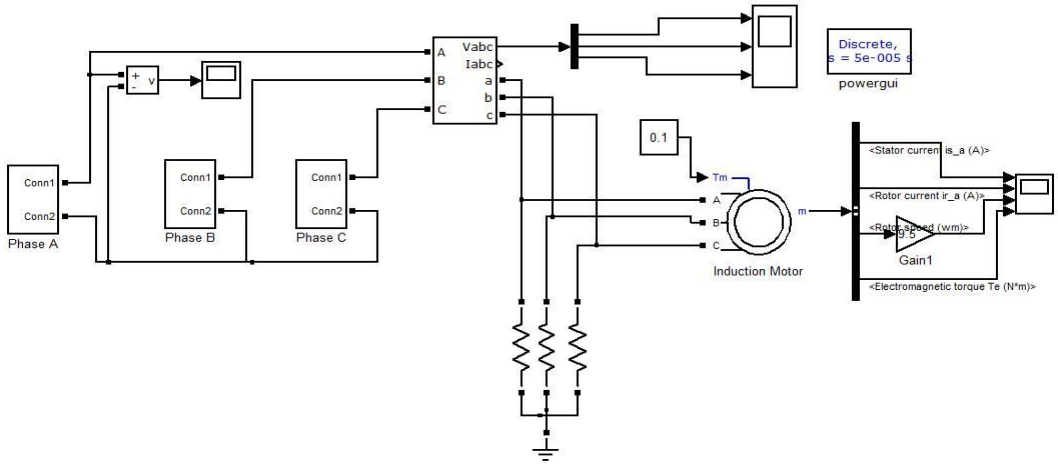


Figure 12: Proposed MLI fed induction motor system

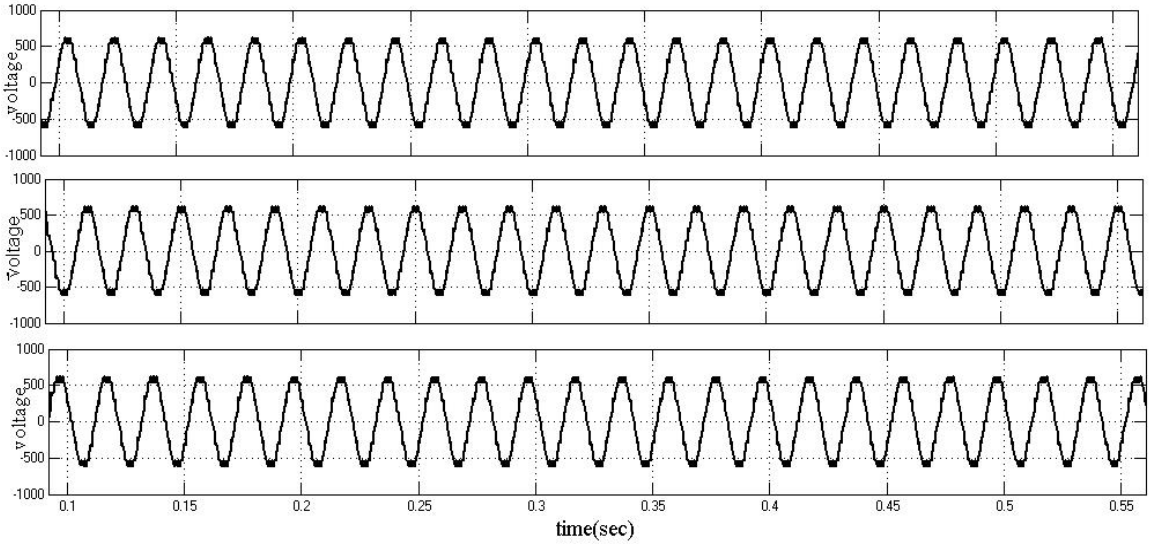


Figure 13: Three phase voltages applied to induction machine

The following table V shows the voltage and current THD content for the proposed multilevel inverter and cascaded NLI topologies.

Type of MLI	Voltage THD value	Current THD value
Proposed MLI in symmetrical configuration	17.27%	17.27%
Cascaded H- MLI in symmetrical configuration	18.2%	18.2%

VII. CONCLUSION

This paper proposes a new multilevel inverter topology for induction motor drive applications. The proposed MLI uses only nine switches in symmetrical and asymmetrical configuration to generate seven level and thirteen level output waveform respectively. As compared to conventional MLI the proposed inverter utilizes lees switches so that the switching losses and cost also is low. The proposed MLI can also used to drive the induction motor. Finally the proposed MLI feeding induction motor is proposed.

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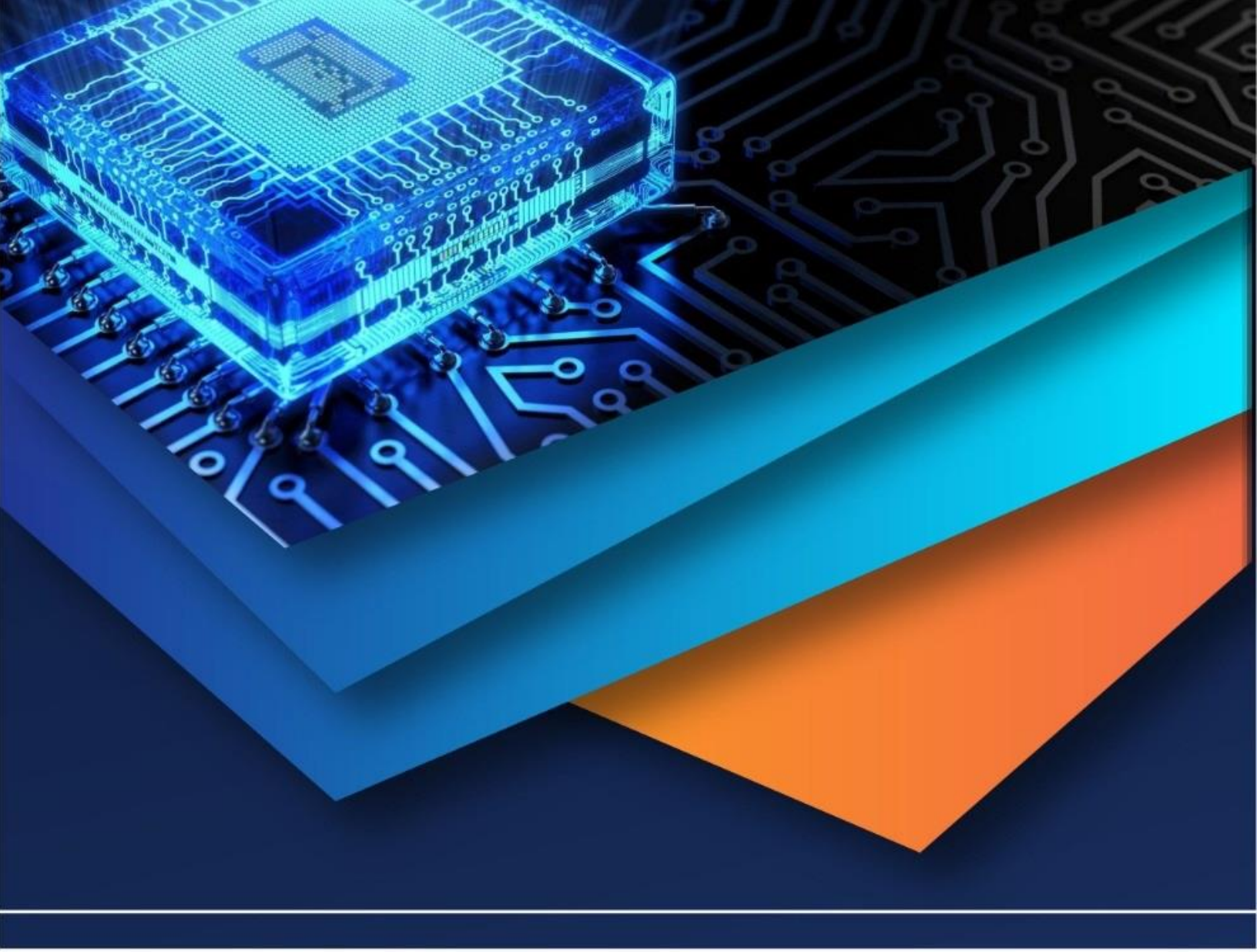

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