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Performance Evaluation of 6T FinFET SRAM and 6T CMOS SRAM Cell

Sundeep Kaur[1], Mandeep Kaur[2]
[1,2] *M. Tech student, Department of ECE, Punjabi University, Patiala, India*

Abstract: Memory occupies more than 70 percent of area in today's system on chip and the tendency remains to be rises in coming years. As the technology is scaling the bulk MOSFET faces a variety of challenges which lead to become more intense leakage. Below 32nm technology, FinFET is the most promising substitute to bulk CMOS technology due to decreased short channel effect. The proposed 6T SRAM cell is designed using MOSFET, FinFET at 16nm and 45nm technology node and its performance parameters such as power, delay, Power Delay Product (PDP).
Keywords: SRAM, FinFET, PDP, HSPICE.

I. INTRODUCTION

The incorporated circuit innovation is advancing at a great pace since the creation of first MOS microchip in 1970. The major driving force behind this advance is the procedure of scaling. The scaling of MOS transistor has brought about high thickness, high performance chips. Yet, this scaling down is blocked by numerous undesirable issues that emerge in MOS device as the device size goes on shrinking [1]. Out of these issues, control dissemination is a major drawback. It has been record as one of the difficulties in International Technology Roadmap for Semiconductors (ITRS) 2012. Different low power outline systems utilizing CMOS are executed but they see certain confinements. Consequently the requirement for new transistor innovation arises. In this report, one such innovation, FinFET innovation is examined. From the point of view of circuit operation, a FinFET carry on particularly like MOSFET. Nonetheless, two gates give a more prominent control over the channel due to which many execution parameters can be adjusted. A 6T SRAM cell stores 1 bit of information in two cross coupled inverters framing a lock and utilizes two transistors for read and compose operation. Word line is utilized to enact get to transistor which encourages the correspondence of interior cell hubs with input/yield ports of cell called bit-lines. Amid read operation bit-lines are driven high and low separately by two cross coupled inverters in 6T SRAM cell which enhances SRAM data transmission when contrasted with DRAM. 6T SRAM cell might be planned at reasonable innovation hubs by utilizing CMOS and FinFET [2-3]

A. SRAM Design Tradeoffs

1) *Read and Write Stability:* The base voltage that can be come to amid read operation is called as perused voltage is dictated by division of voltage between pull down transistor and get to transistor. Read soundness can be affirmed by low get to transistor driving quality which diminishes read voltage. In compose operation, the most extreme voltage that can be come to is called compose voltage which is dictated by division of voltage between get to transistor and draw up transistor. Compose security can be affirmed by solid get to transistor driving quality which diminishes compose voltage [4-5].
2) *Area and Yield* : The most vital properties of memory plan its thickness and usefulness. Usefulness for vast recollections is secured by giving great clamor edge between yields. The commotion edges can be diminished by appropriate measuring of the gadget. Additionally by choosing limit voltages and supply voltage the usefulness can be made strides. Upsizing of transistors diminishes thickness of memory as cell territory increments [4-5].

The methodology of proposed work is appeared in Fig.1 which introduced the fundamental concentration of research work in outlining of conventional 6T SRAM cell.

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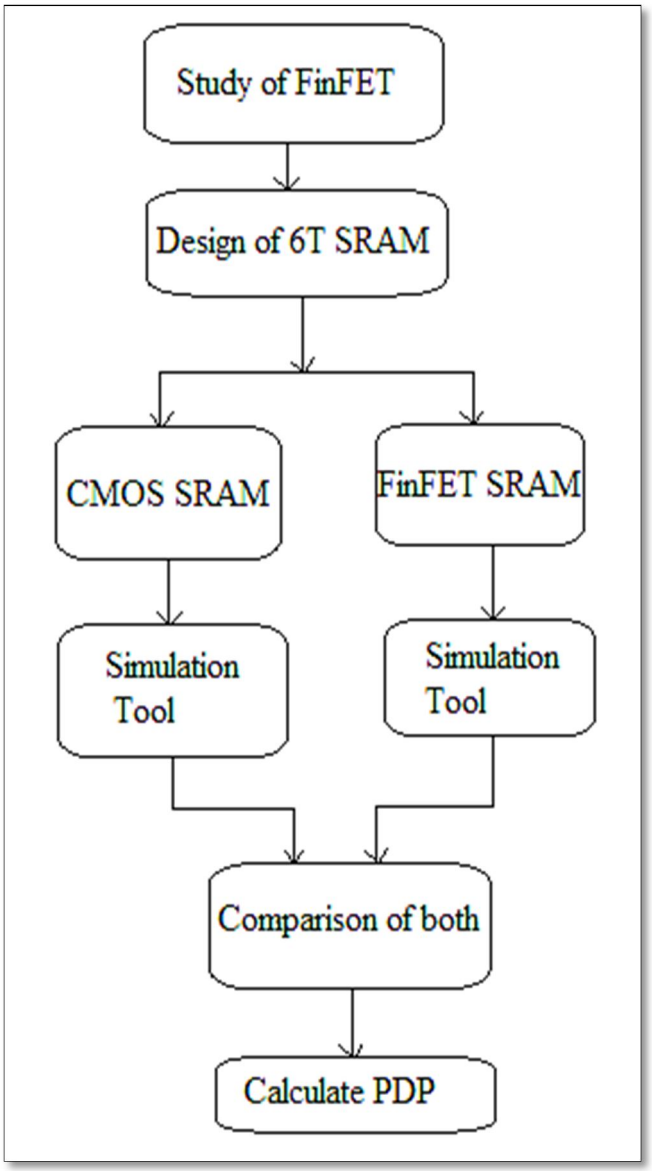
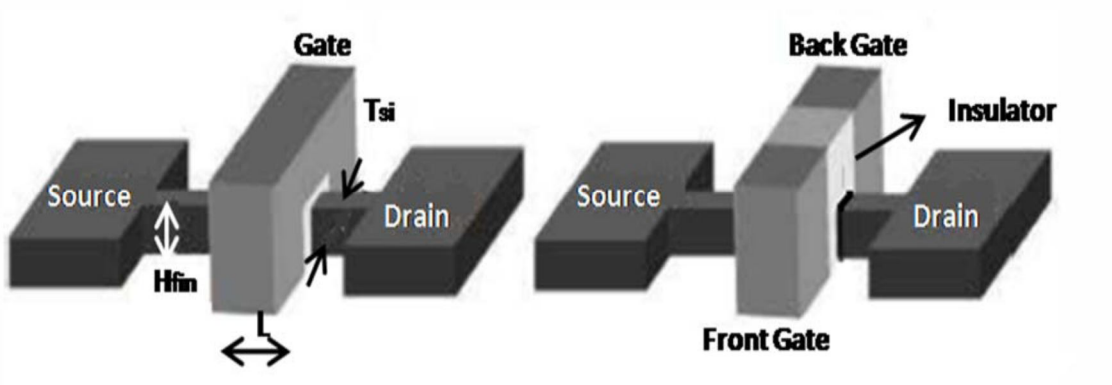


Fig. 1 Design Methodology

This paper starts with brief introduction of FinFET. Section II describes the FinFET device structure. Section III depicts the operation of conventional SRAM cell. Section IV describes the simulation results and section V describes the experimental results of the proposed cell in terms of Power, Delay and Power Delay Product (PDP). Finally, section VI concludes the proposed paper.

II. FINFET DEVICE STRUCTURE

The constant down scaling of the mass MOSFET makes many short channel effects, leakage currents and device varieties beneath 32nm. But the non-organizer FinFET has better control on short channel effects, better yield, low leakage currents and reduce the obstacle in downsizing of transistors [6]. In Double Gate (DG) FinFET the second gate is added inverse to the customary entryway as in MOSFET. The operation of FinFET relies on its two gates. At the point when the two entryways are at same potential then the mode is said to be Shorted Gate (SG) operation. At the point when both the entryways are at the diverse potential then one gate is utilized for exchanging the device and other gate is utilized to control the limit voltage of the transistor, this mode is said to be Independent Gate (IG) operation [6]. The entryways of the FinFET are made on the vertical side of fin, though the source and drain are on the level side as shown in fig.2.



(a) (b)

Fig.2 3D perspective of (a) shorted entryway FinFET (b) independent gate FinFET [7].

The quantized width (W) is the various factor of height of the fin (Hfin). The quantized width of the Shorted Gate (SG) FinFET can be evaluated as:

$$W = 2\times Hfin + Tsi \quad (1.1)$$

While for Independent Gate (IG) FinFET the fin thickness (Tsi) can be disregarded for quantized width estimation:

$$W = 2 \times Hfin \quad (1.2)$$

In both the cases to builds the width of the device number of fins are expanded [7].

III. OPERATION OF CONVENTIONAL 6T SRAM CELL

The conventional 6T SRAM cell using FinFETs is shown in Fig. 3. This cell is made up six transistors. Two pairs of inverters are connected such that the output of one is fed to the input of the other and vice versa. This feedback connection stabilizes the storage nodes in the cell. Two other transistors are utilized as access transistors and are associated to the storage nodes (Q and QB) of the two inverters. The signals word line (WL), bit line (BL) and bit line bar (BLB) control the operation of the cell. When WL is high, the access transistors are turned on providing the access to the storage nodes. For write operation, BL and BLB are set according to the value to be written (complement of each other) and Q and QB are pulled to the required levels. For read operation, BL and BLB are pre charged to high voltage. Either BL or BLB discharge depending upon the values of Q and QB, thus data is read. Fig. 3 6T SRAM cell using FinFET.

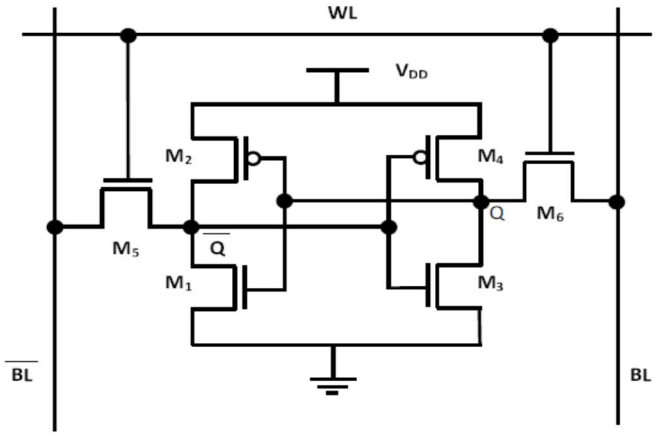


Fig. 3 FinFET based 6T SRAM Cell [8]

IV. SIMULATION RESULTS

6T SRAM cell is planned and its execution parameters are analyzed at 45 and 16nm technology nodes. The SPICE simulator is utilized for reproduction prepares and Predictive Technology Model (PTM) parameters are utilized for both 16 and 45nm technology nodes. The simulations of the previously mentioned modes are clarified in this section.

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A. 6T FinFET Based SRAM Cell

1) Firstly Write and Hold Operation is Performed which are shown in fig. 4. *:* In first stage (0 to 20ns), Word Line (WL) is ON and information given on bit lines BL, BLB for that period are written to nodes of the SRAM cell Q and QB separately. Second stage (20 to 40ns) is the hold mode in which Word Line (WL) is OFF and information given on bit lines for that period is not written on the nodes of the cell in light of the fact that both access transistors are in OFF state with logic '0' at entryways voltage. Similarly simulations is done for 200ns depending upon voltages gave.

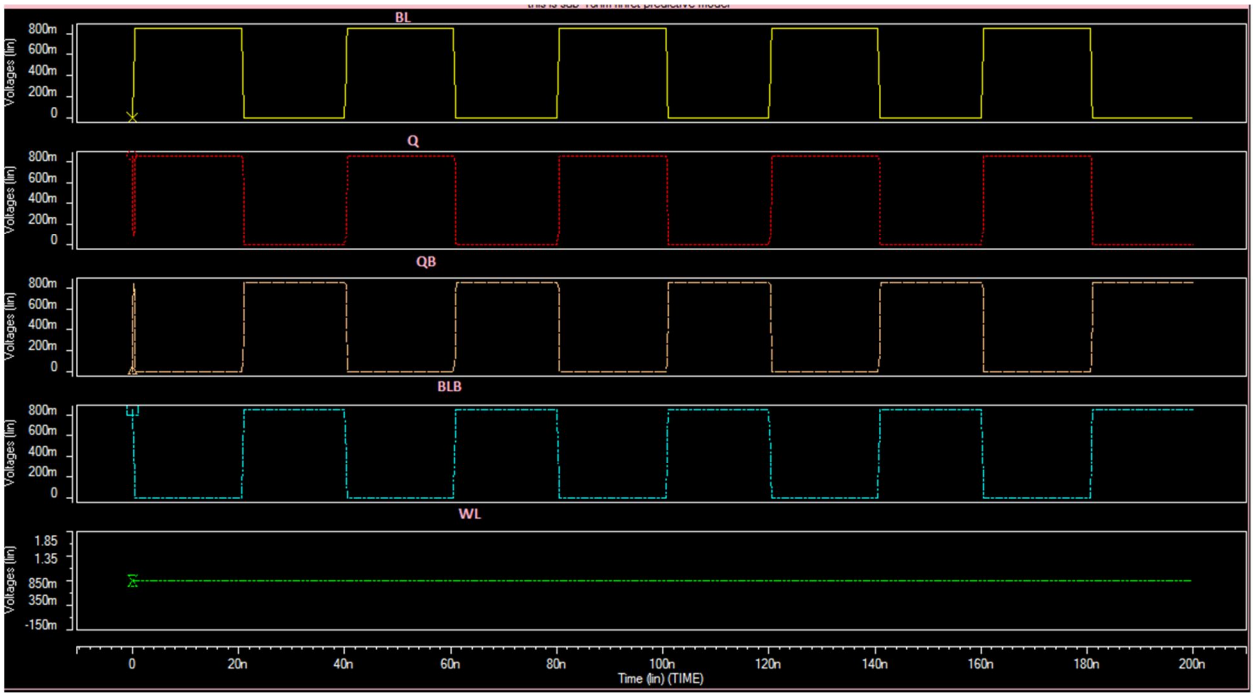

Fig.4 Write and Hold Operation of 6T SRAM at 16nm.

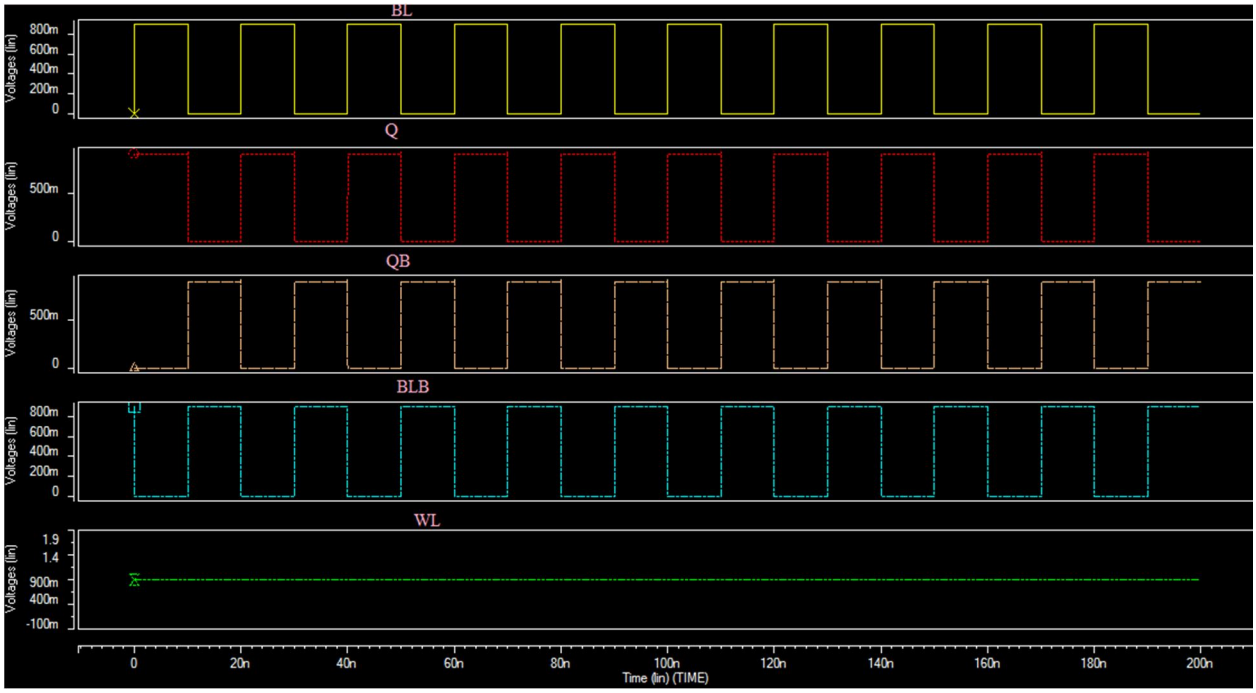

Fig.5 Write and Hold Operation of 6T SRAM at 45nm.

2) In Read Operation Data Written on Node Q is Read as shown in Fig. 5.: In first stage (0 to 20ns) WL is ON, Q is high (VDD). Bit Lines are precharged to half of the VDD. BL will get charged to VDD from its precharged value. Similarly BLB will be discharged to 0 potential 'GND'. So, charging and discharging of BL and BLB represents logic '1' is stored on node Q and logic '0' is stored on node QB. Similarly in second stage (20 to 40ns), WL is OFF and information stored on Q is logic'1' then BL will not charge or discharge and stays at its precharged value (half of the VDD). So, read operation is performed when WL is ON; since if access transistors are OFF information stored on nodes Q and QB will not be transferred to Bit lines. Similarly simulation is done for 200ns depending upon voltages gave.

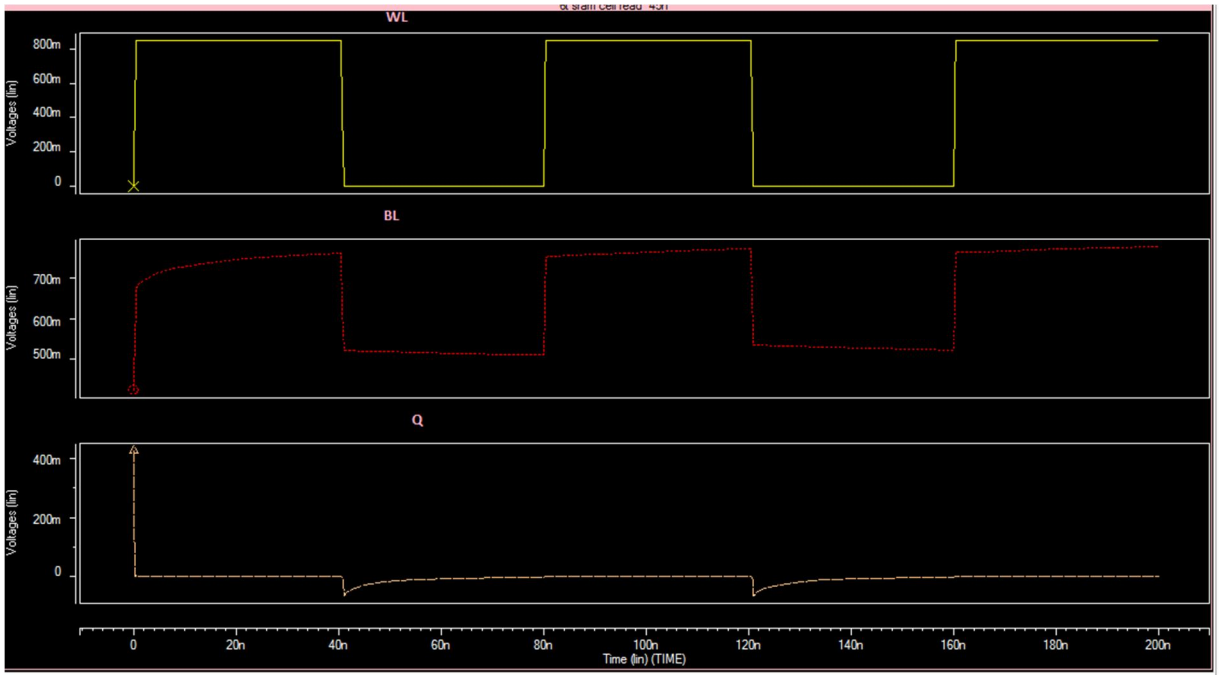

Fig. 6 Read Operation of 6T SRAM.

V. RESULTS AND DISSCUTIONS

This section includes the analysis of various parameters of both FinFET based SRAM cells at 16nm technology node. Table 1 show the parameters used at 16nm technology node.

Table 1: Parameters of 16nm technology node

Parameters	16nm technology node
VDD	0.85
IGF(nm)	16
IGB(nm)	16
TOXF (nm)	1.35
TOXB (nm)	1.35
TSI (nm)	9
HFIN (nm)	26
HGF (nm)	26

A. Power Delay Product (PDP)

Power Delay Product (PDP) is multiplication of average power dissipated and propagation delay. Power Delay Product (PDP) is calculated by performing transient analysis of SRAM cells. Table 2, 3, 4 and 5 shows the reduction in PDP in the conventional 6T SRAM cell in both read and write mode.

Table 2: Average power, Delay and PDP of SRAM cells in Read mode at 16nm

Transistor Type	Power(nW)	Delay(ns)	PDP(aJ)
MOSFET	1.58	7.50	1.18
FinFET	1.21	1.01	1.23

Table 3: Average power, Delay and PDP of SRAM cells in Read mode at 16nm

Transistor Type	Power(nW)	Delay(ns)	PDP(aJ)
MOSFET	3.14	7.20	2.26
FinFET	4.27	8.11	3.46

Table 4: Average power, Delay and PDP of SRAM cells in Read mode at 45nm

Transistor Type	Power(nW)	Delay(ns)	PDP(aJ)
MOSFET	6.81	2.24	1.65
FinFET	7.04	7.99	5.63

Table 5: Average power, Delay and PDP of SRAM cells in Write mode at 45nm

Transistor Type	Power(nW)	Delay(ns)	PDP(aJ)
MOSFET	1.84	2.00	3.69
FinFET	1.73	8.48	1.46

VI. CONCLUSIONS

In the proposed work we have use similar procedure parameter for MOSFET and FINFET. And both are compared with SOI MOSFET at 16nm and 45nm node. MOSFET 6T SRAM and FINFET 6T SRAM are designed using HSPICE. In this paper decrease the Power Delay Product (PDP) of conventional 6T SRAM cell. FinFET based SRAM cell can be utilized to invent memories below 32nm without any Short Channel Effects (SCE).

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