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LPHSRA: Low Power High-Speed Routing Algorithm for 3D-Network on Chip

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Abstract: ***Low Power High-speed routing algorithm is a congestion controlled hybrid routing algorithm. When congestion and routing distance reduces, then the device can able to offer with low power and low latency. Particularly, to perform multiple tasks in Internet of Things should have a smart device with low latency high-speed multiprocessors are required. The objective of this paper is to propose low power high-speed routing algorithm for Network on Chip. Low power high-speed routing algorithm (LPHSRA) which includes XYD and virtual channel router architecture. Therefore, experimental work of LPHSRA was carried out with respect to 8-bit, 16-bit, and 32-bit. As and when a number of bits increases, then its area, power, and latency also get increases. Routing algorithm has designed into three categories, such as Best-path, Average-Path, and worst-path (most critical path). According to the experimental and Xilinx reports, the performance of 3D-mesh showed reduced latency and low power for Best-path. The entire experiment work for 3D-Mesh and its router architecture carried out by using Xilinx-14.3 and target on the Vertex-7 FPGA.***

Keywords: Network on Chip, XYD routing algorithm, Shortest path routing algorithm, Low latency, and congestion.

I. INTRODUCTION

In day to day life, a number of Processing Elements (PEs) are increasing in System on Chip (SoC), that becomes a major problem because whenever number of PEs is increased the power, area, and latency also increases. To handle those many PEs in a single chip become a tedious job. Nowadays, designing a System on Chip communication architecture becomes a challenge. Whenever IP (Intellectual property) cores are interconnected with a point to point connection or bus-based connectivity[1], [2] then it leads to cause high power consumption, unpredictable delays, and severe on chip synchronization errors [3].

To manage the complexity in System on Chip, Network on Chip (NoC) is a novel trend and promising alternative architecture when compared to the traditional methods. NoC able to offer better scalability, low power consumption, reusable, estimation of predictable delays when compared to the earlier methods. A modern SoC architecture called as NoC as shown in figure-1.

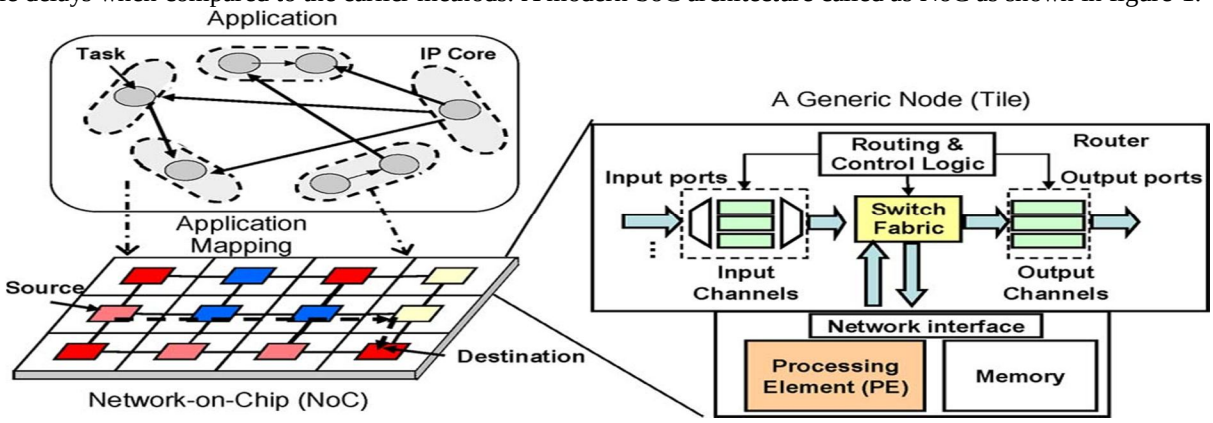

Figure-1. Network on Chip based Multiprocessor System on Chip (NoC based MPSoCs)

There are two types of NoCs such as Heterogeneous and homogeneous NoCs. Heterogeneous NoCs consists of various types IP Cores or PEs but whereas in Homogeneous NoCs having with unique IP cores or unique PEs. Fig-1 shows that heterogenous NoCs are interconnected with various IP cores and each local router associated with one different IP core. Each and every local router interconnected with neighboring routers.

Heterogeneous IP cores may be CPU or DSP modules, video processors, embedded memory blocks, etc. Each router generates the address to reach the source to the destination node via Network Interface (NI). Initially, the packet begins with the local processing element or processor which is interfaced with local router. The router will decide where to reach the destination. More previously,

NI plays a major role which enables communication interface between the cores and local routers. Therefore, the packet is stored virtually at the input channel, and then router takes the decision to transmit the packets.

Transmission time period is not only to take a decision for transmission by the router, which includes allocating the channel, and transverse the neighboring links to the next router and etc. Once after assigning the target to the router, the process will be repeated until to reach the target final destination. Therefore the performance process among the communication cores, transmitting packets, generating address and network interface between the cores and among the connectivity of local routers are the major challenges.

NoC depends on the target application to decide the characteristics of communication latency, computation components in NoC is speed and power, Characteristics of the size of the network and buffer length entirely depends on the application, all these computation elements are the major challenges for current Electronic design automation tools. There are some outstanding research problems which are left in the NoC design. To this contrast this paper aimed at algorithm level, circuit level of abstraction. So designer perspective to design the on-chip interconnect for a wide range of applications. Figure-2 represents the flow of NoC architecture analysis and optimization, this flow clearly shows from the choice of application down to the layout level considerations. Here, the significant and more precious stretch on various difficult issues in NoCs.

Here, in this section explicitly consider most difficult issues of NoC research those are broadly classified such as 3D-NoC logic design and optimization techniques for various applications, NoC structure and optimization process, NoC synthesis, validation and tape-out process as shown in figure-2.

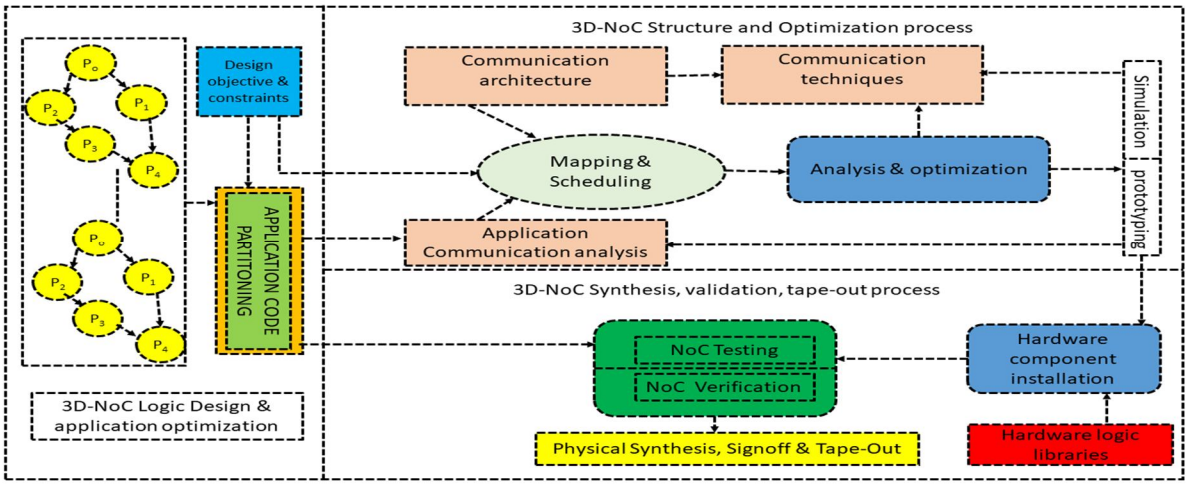

Figure-2 3D-NoC standard architecture optimization flow.

A. 3D-NoC Logic design and Application optimization

Initially, the step is to find the target application and their detailed specifications. First, we have to determine the related traffic patterns and bandwidth requirement for each and every node in the network. The main target is to reduce the latency and optimize the power consumption. Power consumption is completely based on the switching mechanism, multi-core devices are the power hungry devices, so, to reduce the power consumption is a big tedious job. 3D-NoC logic design enables to operate the IP core when it requires doing the particular operation. This is how power can optimize and at the same time if communication distance between the IP cores can also optimize the power. There is an important thing is to arrange the shared memory architecture in the 3D-NoC router. 3D-NoC router plays a major role in multi-core device applications. Application portioning is another big task, there are two types of architectures such as homogeneous and heterogeneous. In homogeneous or heterogeneous applications clock plays an important role because depends on the application, the clock needs to be designed either synchronous or asynchronous. All these design techniques are impacting for the network traffic, energy, and power performance.

B. 3D-NoC Communication Structure and Optimization

To understand the congestion traffic and design specification which helps to architect the optimized topology. Their several topologies are available such star, bus, ring, MESH, Torous and etc. Among all these, Mesh topology is most popular architecture and it is simple for design optimization. It has more significant key impacts such as design, power, area, latency optimization, and overall performance. In order to manage the traffic congestion, an efficient routing algorithm is essential.

C. 3D-NoC Communication Architecture Evaluation

In 3D-NoC communication architecture needed to determine the congestion point, critical path and power estimation, and etc. Simulation analysis can able to estimate the number of cycles required to complete the packet transmission. With this information, the physical designer can proceed with floor planning, placement, and routing. In addition, in a back-end design flow area occupied, power consumption, latency estimation can able to predict accurately.

D. NoC Design Validation and Synthesis

Once after the design is ready, it requires logic hardware component libraries, parasitic issues, temperature libraries, clock information, power libraries and etc. All these component libraries are required for synthesis process. To validate the synthesis design and prototyping the hardware components, efficient CAD tools are essential. Now a day's all SoC and NoC design are power hungry devices. So, here the main research problem about power consumption and latency issues in 3D- NoC. In the next section discussed related work of power consumption and latency of NoC architectures. The next sections are organized as follows: in section-2 briefly described as NoC related work, in section-3 explanation of 3D-NoC router architecture, in section-4 3D-NoC experimental results and in section-5 conclusion with a future scope.

II. RELATED WORK

Chen Wu et al. [4] proposed an efficient application mapping re-configurable technique to achieve the optimized power consumption with low latency. Even though an efficient mapping technique, there will be some intermittent and transient faults are commonly occurred in NoC design. In a mapping technique, communication will be occurred based on the priority and an importance is given for each node in clustered network. There are two techniques to find the node in a clustered network such as branch node priority reorganization and partial importance utilization given for some elective nodes and which is adapted to determine the search efficiency. With the proposed techniques has several advantages such as flexibility, reconfigurability, power optimization, low latency with the high-speed communication process.

Amir-Mohammad et al. [5] proposed a high performance with lower power interconnect logic to implement the bi-directional bi-synchronous architecture for 3D-NoC. 3D-NoC consumes less area than 2D-NoC, but it is difficult to implement the 3D-NoC design. In fact, the number of links between the router and each layer in 3D-NoC will be increased. Power aware bi-directional bi-synchronous vertical channels can able to the utilization of less power and it can enhance the interlayer communication architecture. Bidirectional Bisynchronous vertical channels can also to optimize the latency without degrading the function.

Xiao hang Wang et al. [6] proposed a Hierarchical Ring Cluster (HRC) for 3D-NoC. HRC has three layers such as initially nodes are formed as a group and it is converted into rings, next is to make rings into cubes, finally, all cubes are made of the well-established network. Routing mechanism also made into hierarchal fashion, circuit switching connectivity made for rings with low latency, and data wants to communicate with higher layer than traditional XY routing algorithm was used with the help of wormhole switching. HRC architecture offers lower latency with less power consumption when compared to the traditional methods.

C. Marcon et al. [7] proposed an efficient 3D-NoC designed with respect to low latency and less area for multi core applications. 3D-NoC architecture is scalable in terms of area, but it consumes a lot of power and it offers parallel communication with more density [8]. 3D-NoC can able to reduce the communication distance, it increases the throughput and also it offers less latency with the short execution of the application.

Kan Wang et al. [9] proposed Three Stage Synthesis Flow (TSSF) with Multiple Supply Voltages for 3D-NoC. These two techniques solve all kind of issues like layer assignment, voltage level assignment, 3D NoC synthesis and also physical design. A unique design style of layer assignment with voltage level assignment where it achieves less power consumption. During the synthesis process, there is one of the most important tasks is assigning hardware components and its position of the core to each layer in 3D-NoC. The most tedious job in 3D-NoC is interlayer communication between the network components and IP cores. Transitive Closure Graph (TCG) can able place the hardware components properly and repacking technique is applied to 3D-NoC for reducing the power consumption.

Lev Kurbanov et al. [10] proposed P-medians searching algorithm to achieve better system performance in 3D-NoC. In modern 3D-NoC, it has a problem with interconnectivity links between the cores and routers. Majorly, in 3D-NoC vertical links are difficult to interlink between the layers, P-median algorithms can able to solve the problem of interconnections and placement of IP cores.

Vasilis F. Pavlidis et al. [11] explained the 3D-NoC for future multiprocessors, 3D-NoC consists of a maximum number of planes when compared with the 2D-NoC. Speed and power models of 3D-NoC are easier to achieve good performance when compared to the traditional approach of 2D-NoC. In the next section will be discussed with 3D-NoC router architecture.

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III. LOW POWER HIGH-SPEED ROUTING ALGORITHM (LPHSRA)

A. 3D-NoC Virtual Channel Router Architecture

NoC router is a significant role in multiprocessor applications, here the router acts as a controller and it manages the network traffic. Instead of a direct connection between the core to core or processor to processor NoC router and its network interface was introduced.

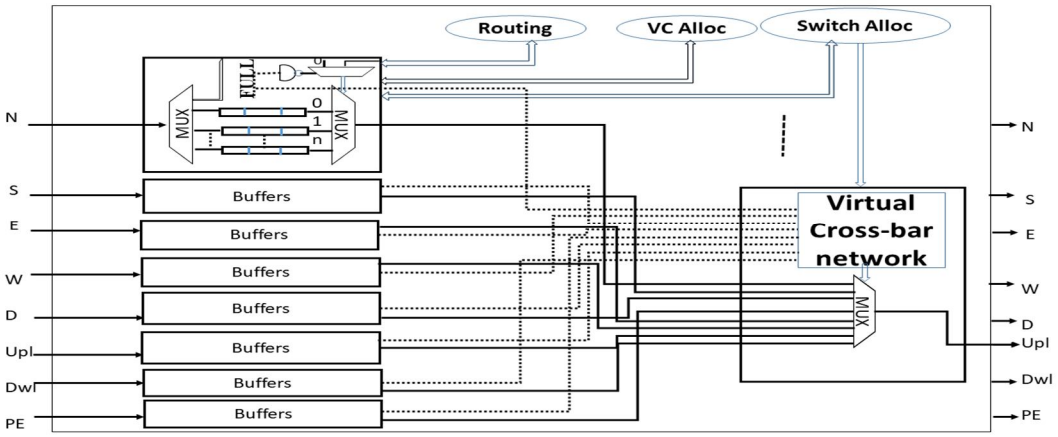


Figure-3: 3D-NoC Virtual Channel (VC) Router architecture

Here the main advantage of NoC router it controls the packet transmission and balances the network traffic by enhancing the network throughput. Every traditional wormhole router [8] has five directional ports such as East [E], West [W], North [N], South [S], and local port. Each input port has one buffer storage associated with it. Each and every router associated with the neighboring router and the local port is interfaced with processor or core. Network interface interconnected between router to router and router to the core. The main drawback of wormhole router architecture, Packet transmission wait and Queue process it is just kind of deadlock problem this happens during transmission when the number of packets is waited behind on the input port then deadlock issues naturally occur. So, this process generally consumes a lot of power and of course, it consumes less area. To avoid this problem in wormhole router, Virtual Channel (VC) Router is introduced [12]. VC router can able to solve the issue of deadlock and power consumption by increasing the virtual storage in the router design.

The above figure-3 shows the 3D-NoC Virtual Channel router architecture for multiprocessor applications. To eliminate thewait and queue process in wormhole router architecture, by using virtual cannel the issue can be solved. Now for 3D-NoC router architecture has nine directional ports such as East [E], West [W], North [N], South [S], Diagonal port [D], vertical uplink (upl), vertical downlink (Dwl), and local port [13] & [14]. Usually, 2D-NoC router has only five directional ports. Routing section decides the direction for transmission of the packets and when switch allocation doesn't give grants for transmission of packets then VC allocation will be instruct to all virtual buffer to store the packets temporarily. Virtual cross-bar network is depended on the release of grants from the switch allocator, then cross-bar network decided to link to the neighbouring router. This 3D-NoC router architecture is used for examining the 4x4x3 3D-Mesh topology as shown in figure-4.

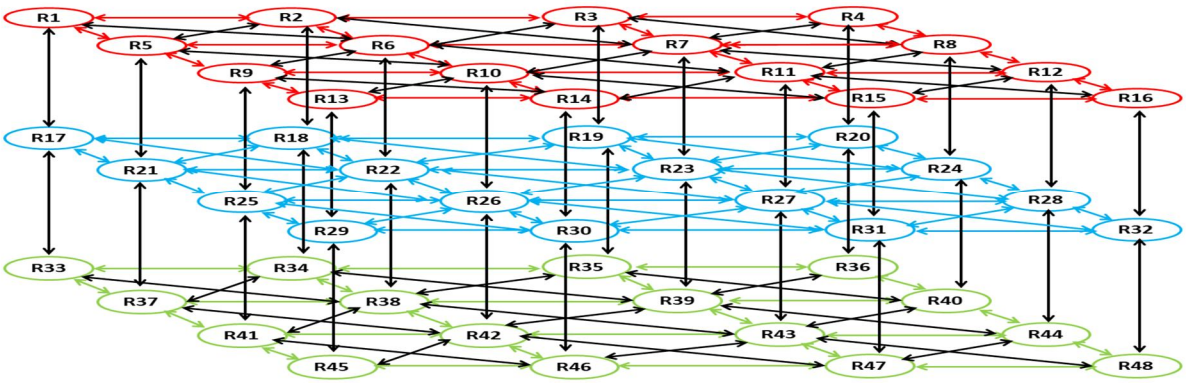


Figure-4: 4x4x3 3D-Mesh topology

B. XYD V_Ul &V_Dl Dimension Ordered Routing Algorithm for 3D-Mesh

$X = X_{source} - X_{Destination}$ (X-direction: horizontal direction)
$Y = Y_{source} - Y_{Destination}$ (Y-direction: lateral direction)
$D = D_{source} - D_{Destination}$ (D: diagonal direction)
$V\_Ul = V\_Ul_{source} - V\_Ul_{Destination}$ (V_Ul: Vertical upper link)
$V\_Dl = V\_Dl_{source} - V\_Dl_{Destination}$ (V_Dl: Vertical Down link)
If X=0,Y=0,D=0,V_Ul=0,V_Dl=0 then
Destination=local port;
If X>0,Y=0,D=0,V_Ul=0,V_Dl=0 then
Destination=East direction;
If X=0,Y<0,D=0,V_Ul=0,V_Dl=0 then
Destination=West direction;
If X>0,Y<0,D=0,V_Ul=0,V_Dl=0 then
Destination=North direction;
If X>0,Y>0,D=0,V_Ul=0,V_Dl=0 then
Destination=South direction;
If X=0,Y=0,D>0,V_Ul=0,V_Dl=0 then
Destination=Diagonal direction;
If X=0,Y=0,D=0,V_Ul>0,V_Dl=0 then
Destination=Vertical uplink direction;
If X=0,Y=0,D=0,V_Ul=0,V_Dl>0 then
Destination=Vertical downlink direction;

A typical dimension ordered routing algorithm for 3D-Network on Chip as expressed each and every step in 3.1. Here, X- plane represents horizontal direction, Y-plane represents lateral direction, D-plane represents diagonal direction, V_Ul-plane represents vertical uplink direction, and V_Dl-plane represents vertical downlink direction. All these directions are decided and instructed by the router. XYD routing helps to manage the congestion problems in 3D-NoC. In the next section will be discussed experimental work of 3D-NoC router and 3D-Mesh.

B. Pipelined Data Path Format

Router design has six stage pipelined architecture for 3D-Mesh NoC such as Buffer write, routing computation, Virtual channel allocation, Switch allocator, Switch traversal, and Link traversal. Buffer Write is used to allow the data at the input, Routing Computation is instructing the packets to decide the target, Virtual Channel allocation is involved when input buffer storage is full, no more data packets will be allowed by the virtual storage until the operation complete, Switch allocator used to decide the storage in VCA and crossbar network by releasing the grants, Switch Traversal used to established a path between input to output, and Link Traversal establishes communication link among the corresponding neighboring routers. In the next section will be discussed with experimental results.

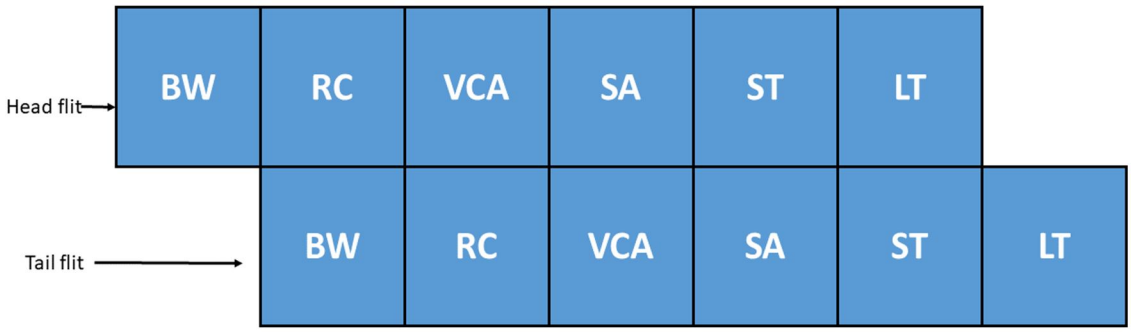
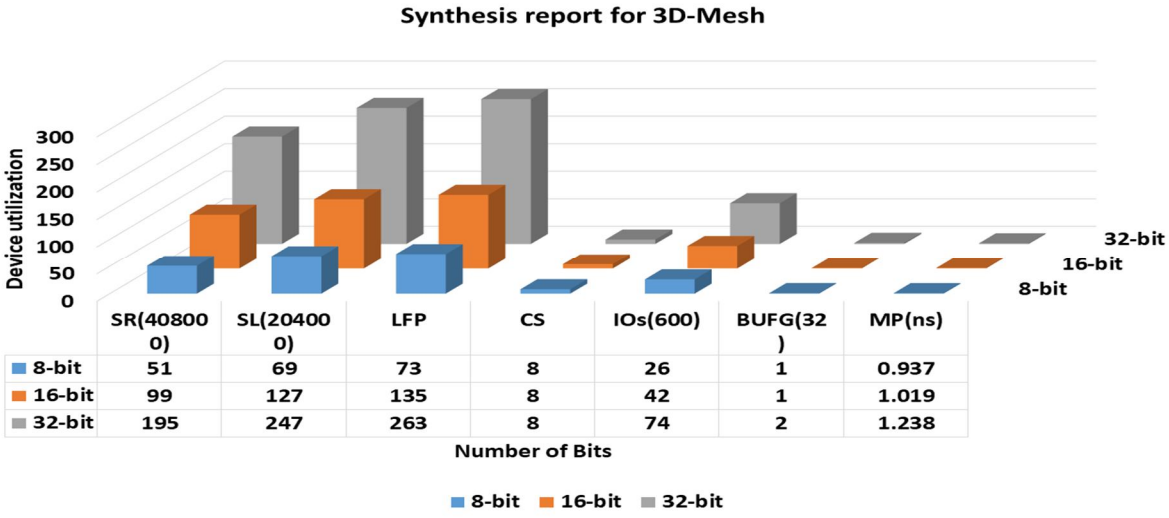


Figure-5: Pipeline Data path format for 3D-NoC virtual channel router architecture

C. Experimental Work

3D-NoC architecture with router design has evaluated in terms of latency, utilization of power, throughput and area utilization. The entire experimental work carried out by using Xilinx-14.3 targeted on vertex-7 FPGA. Here, each router has to take six cycles to execute the operation, there are three categories of performance has evaluated for 3D-Mesh NoC like Best, Average, worst case for determining the latency and throughput. Best is the most optimized path, the average is the medium distance path, worst is the largest distance path or critical path. The best path is always communicated via a diagonal shortest path, average path utilizes the both diagonal, as well as another path, depends on the network traffic, and the Worst case path is the maximum distance path which is the most critical path distance to communicate among the nodes in 3D Mesh network.

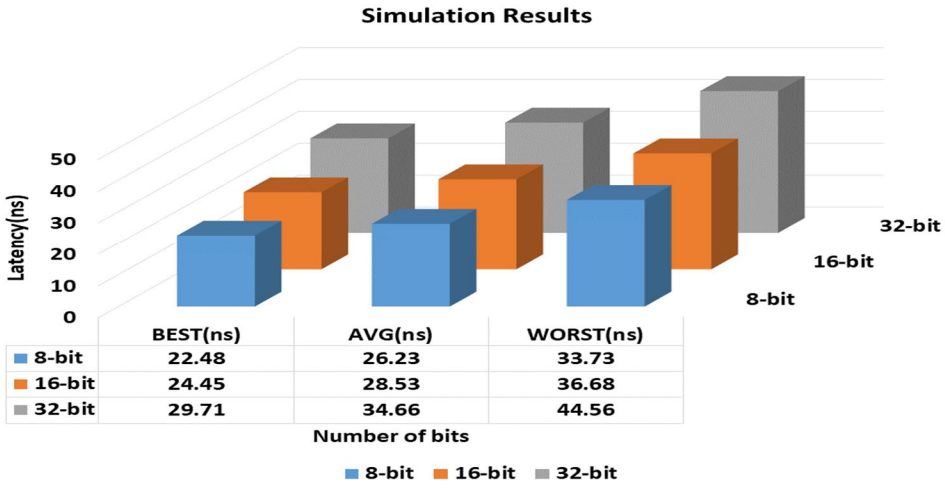
Synthesis and Simulation result elaborately carried by using Xilinx 14.3, the 3D-NoC design made and tested with different bit configuration such as 8-bit, 16-bit and 32-bit. As long as the size of the bits increases then simultaneously utilization of area also increases. In wormhole router architecture there is no number of the buffer so that, the utilization of would decrease, but in this virtual channel, router design occupies more area than wormhole router. The main advantage of virtual channel router can able to reduce the latency and power consumption. The 3D-NoC router is not only targeted for the latency and power, it also can enhance the throughput. The device utilization and it summary as shown in figure-6.



	SR(408000)	SL(204000)	LFP	CS	IOs(600)	BUFG(32)	MP(ns)
8-bit	51	69	73	8	26	1	0.937
16-bit	99	127	135	8	42	1	1.019
32-bit	195	247	263	8	74	2	1.238

Figure-6: Device utilization summary of 3D-Mesh NoC

The above figure-6 shows the utilization of a number of slices, Flip-Flops, Input and outputs, buffers, and minimum time period of 3D-Mesh. Closely to observe the figure-6, when the bit size increases then all parameters are also slightly increased.



	BEST(ns)	AVG(ns)	WORST(ns)
8-bit	22.48	26.23	33.73
16-bit	24.45	28.53	36.68
32-bit	29.71	34.66	44.56

Figure-7: Simulation results of 3D-Mesh

According to the synthesis report, the minimum time period is considered for transmission latency and overall latency got estimated by Hop counts for 3D-Mesh. The minimum time period for 8-bit 3D-Mesh is 0.937ns, for 16-bit is 1.019ns, and for 32-bit is 1.238ns as shown in figure-7. To transmit the packets from Router (R1) to the router (R48) via best path (diagonal direction), it requires a minimum of 22.48ns for 8-bit data, at average 26.23nsand worst case it requires 33.73ns. Similarly, for 16bit data via a best path, it requires a minimum of 24.45ns, at average 28.53ns, and at the worst case minimum of 36.68ns. In the same way, for 32-bit data it requires via the best path is 29.71ns, at average 34.66ns and at the worst case it requires 44.56.

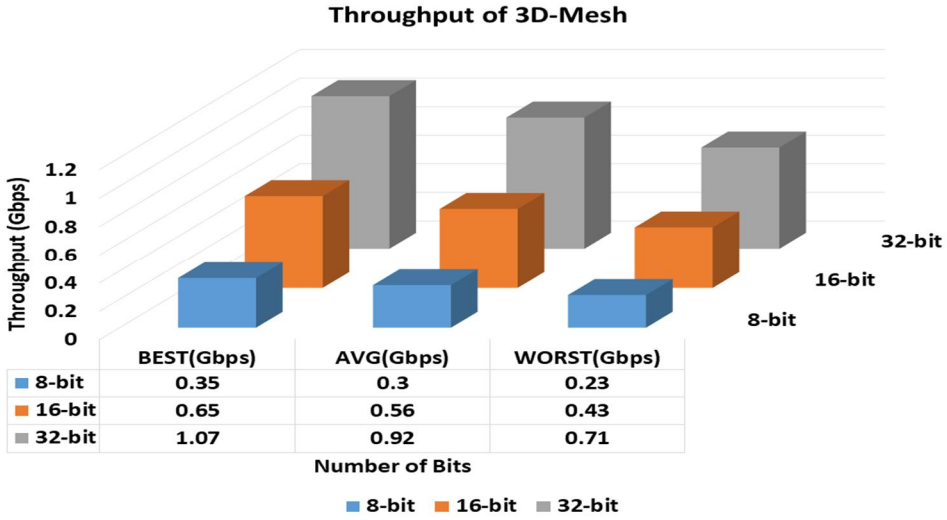


Figure-8: Transmission throughput of 3D-mesh

The transmission throughput estimated according to the simulation report as shown in figure-8. As per the transmission throughput report for 8-bit via best path is 0.35Gbps, at average 0.35Gbps and at worst case 0.23Gbps. In the same way for 16-bit via best path is 0.65Gbps, at average 0.56Gbps and at worst case 0.43Gbps. Similarly, for 32bit data via best path 1.07, at average 0.92Gbps and at worst case 0.71Gbps.

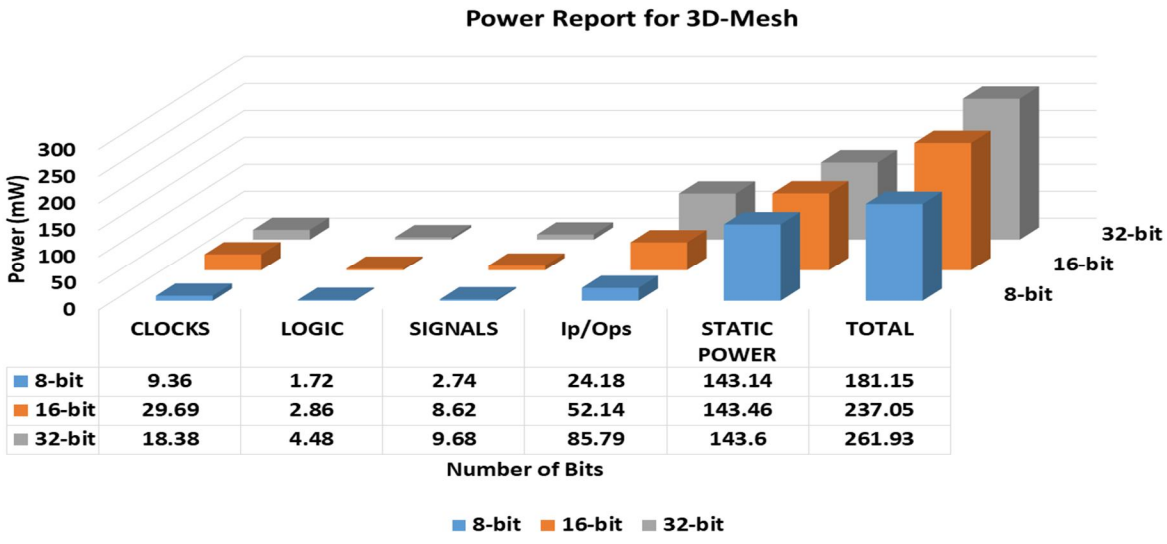


Figure-9: Power report for 3D-Mesh

Power report of 3D-Mesh, for 8-bit data overall power consumption is 181.15mW (Static + Dynamic power). Similarly, for 16–bit data it consumes 237.05mW and for 32-bit data is 261.93mW. Notice, as long as the number of bits increases, then its area, latency, and power consumption also increase.

V. CONCLUSION

As per the experimental work and Xilinx reports of 3D-Mesh, the results showed better performance in terms of utilization of power, less area with low latency. As and when the number of bits increases, simultaneously the area, power, and latency also increases. According to the simulation reports, the throughput shows better for Best-path. XYD routing algorithm instructs the direction and it is incorporated in the virtual channel router architecture. This routing algorithm helps to manage the congestion problems. Therefore, finally conclude that overall performance of 3D-Mesh showed better in terms of reduction in latency with low power.

VI. ACKNOWLEDGMENT

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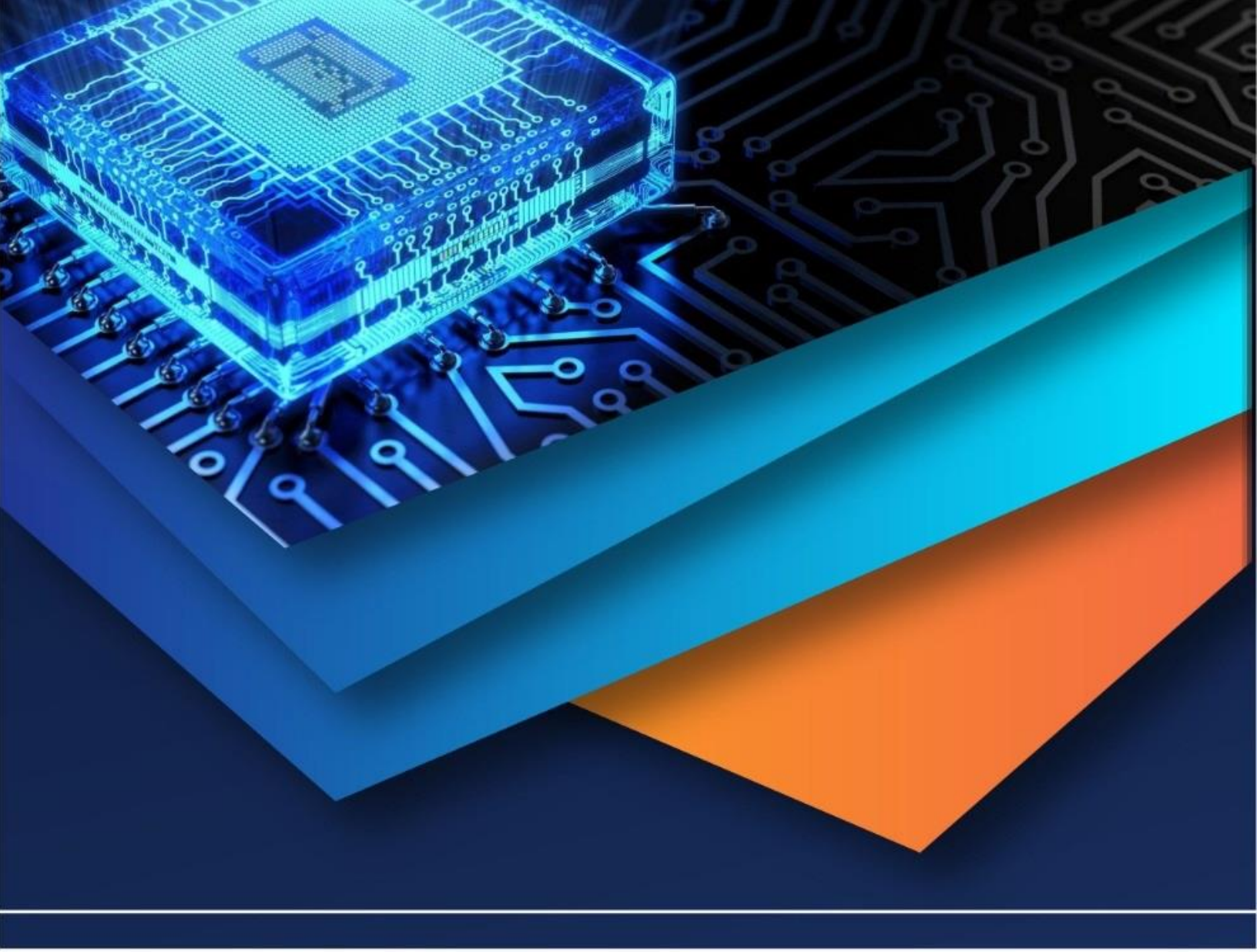

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