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Vertical-Horizontal Binary Common Sub-Expression Elimination for Reconfigurable Transposed Form FIR Filter

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Abstract: ***The Power is the main challenging factor in very large scale integrated circuits. Transpose form fir filters produce better results compared to the direct form FIR filters for reconfigurable applications. In the existing method, the possibility of realization of FIR filter in transpose form configuration Using Common Sub expression Elimination was explored. . This paper explains comparison of two different architectures for low complexity FIR filters namely Constant shift method (CSM), programmable shift methods (PSM) and vertical-horizontal binary common sub-expression elimination (VHBCSE). The FIR filters can efficiently implemented by using constant multiplier architecture based on vertical –horizontal binary common sub-expression elimination (VHBCSE) instead of common sub-expression elimination (CSE). This technique is capable of reducing the average probability of using the switching activity of the multiplier block adders compared to that of existing algorithm i.e., Binary Common sub-expression elimination (BCSE) algorithm. The filter architecture is capable of operating for word length filter coefficient without any overhead in the hardware circuitry. This VHBCSE produce the better power results.***
Keywords: Constant shift method (CSM), Programmable shift method (PSM), Vertical-Horizontal Binary Common Sub-expression Elimination (VHBCSE), and Binary common sub-expression elimination (BCSE.)

I. INTRODUCTION

FINITE-IMPULSE response (FIR) digital filter plays an important role in digital signal processing applications, such as speech processing, loud speaker equalization, echo cancellation, adaptive noise cancellation, and various communication applications, including software-defined radio (SDR) and so on . These applications require FIR filters of large order to meet the frequency specifications. These filters need to support high sampling rate for very high-speed digital communication. The number of multiplications and additions required for each filter output, increases linearly with the filter order. Since there is no redundant computation available in the FIR filter algorithm, real-time implementation of a large order FIR filter in a resource contained environment is daunting and challenging task.

A. FIR Filter

A finite impulse response (FIR) filter is very simple form and straightforward filter. The impulse response is of finite duration $\boldsymbol{N}$ and is equal to zero after and before (since it is causal). It is non-recursive as it depends only on the input. The values $\boldsymbol{hi}$ of the impulse response are called filter coefficients, or filter weights. If the filter is of size $\boldsymbol{N}$, the filter order is of size $\boldsymbol{N-1}$.

$$h = [h0\ h1 \ldots\ hi \ldots\ hN-1]$$

The output is calculated as the discrete-time convolution as given below.

$$x(n) = h0(n)+h1x(n-1)+\cdots+hN-1x(n-N-1) = \sum hix\,(n-i)$$

The great advantages of FIR filters are that they are unconditionally stable and gives linear phase response They are also very simpler
to implement in particular applications. However they usually require more delay and computation than their recursive counterparts.
In any FIR filter, the multiplier block is the major constraints or element, which define the performance of filter. Since many years, many high speed multipliers are proposed and realized such as array multiplier, Booth multiplier, Wallace multiplier etc. Every multiplication follows partial product generation and summation of those partial products. Every partial product is generated by multiplying each bit of multiplier with each bit of multiplicand. These partial products will be added to final result.

The main reason for complexity of filter is increase of adder steps in the multiplier block as the filter order increases, to reduce the complexity Common Sub-Expression Elimination (CSE) algorithm is used. The Previous methods for common sub-expression elimination algorithm to reduce complexity of filter are depends on Canonical Signed Digit (CSD) and graph based. In CSD method the data is in the form {1, 0,-1} and the number of partial products will get reduced. There are lot of implementation methods for reconfigurable FIR filter designs that include fully programmable multiply-accumulate (MAC) based filter processor or the filter coefficients that can be stored in registers. Here two different methods are used to design multiplier block i.e., constant shift method (CSM) and programmable shift method (PSM) to reduce the complexity of FIR filter. The present project work explains about the implementation of Vertical Horizontal Binary Common Sub-Expression Elimination Algorithm (VHBCSE), comparison with previous methods.

Section II describes the literature survey of previous architectures with respect to multiplier block design. Section III explains about designs of multiplier block using common sub-expression elimination algorithm and vertical horizontal binary common sub-expression elimination algorithm. Section IV explains the comparison between the previous architectures and VHBCSE and the synthesis report. Section V has conclusion.

II. LITERATURE SURVEY

Since many years so many experiments were done to reduce the complexity of the multiplier block design from that one of the methods is the greedy common sub-expression which is discussed in [1]. Greedy common sub-expression elimination (CSE) algorithm depends on the canonic signed digit representation of filter coefficients for implementing low complexity FIR filters is proposed in this paper. The look-ahead algorithm is used which chooses the maximum number of frequently occurring sub-expressions to completely eliminate redundant computations in coefficient multiplication and then there is reduction of the number of adders required to implement the filter.

In Previous days a new algorithm is discussed in [2] for implementation of high speed multiplier less filters used to reduce the area. The high speed multipliers designed with the common sub-expression with architecture based on pipeline implementation of two coefficients are seen in [2]. A new algorithm called non-recursive signed common sub-expression elimination (NR-SCSE) is discussed, and several applications in the area of multiplier less finite-impulse response (FIR) filters are developed in this paper.

Moreover the implementation for low complexity filters are going on and one among them is the sub-expression sharing of coefficients in [3] for the filter design. This paper explained the methods for optimizing the design of Canonical Sign Digit (CSD) multipliers, and in particular the gains that can be obtained by sharing sub-expressions in architectures, In the case where several multipliers are present in a network of operators, for instance in an FIR filter, the savings achieved by identifying common sub-expressions can be as much as 50% of the total number of operators. This is one of the efficient technique for identifying sub-expressions. Later on for efficient digital filter using Novel reconfigurable multiplier blocks are discussed in [4]. Again using the CSD method the multiplier blocks are designed but with re configurability i.e., changing coefficients at run time.

Here in this paper [5], the DFG (Data Flow Graph) merging process find similarities among the DFGs, and produces a single data path that can be dynamically reconfigured and has a low area cost, when considering both hardware blocks and interconnections. A new technique for the Data flow graph merge problem, and estimated it using programs from the Media benchmark. This algorithm execution time meet the fastest existing solution to this problem and produces data paths with an overall average area reduction of 20%.

Recently two methods for the design of multiplier block are discussed in [5] to reduce the number of one's in the coefficients for effective multiplication. One is vertical common sub-expression (VCSs) and the other is horizontal common sub-expression (HCSs). In the VCSs the coefficients present in adjacent columns are paired to increase the efficiency in the multiplication. Here in HCSs the coefficients present in same row are paired, as the name itself says that it is horizontal common sub-expression. These two methods are used to reduce the Logical Depth (LD) of adder steps present in multiplier block, To apply this canonical sign digit (CSD) is used instead of binary representation i.e., {1, 0, -1}. Design examples of FIR filters show that our method offers an average adder reduction of 18% over the best known CSE method, without any increase in the logic depth.

III. MULTIPLIER ARCHITECTURES

Mostly The filters are in the direct form, but transposed form filters produce better results compared to direct form in reconfigurable applications and here a new architecture is implemented using a algorithm called binary common sub-expression elimination algorithm. This algorithm deals with the elimination of binary common sub-expressions (BCSs) that occur within the coefficients and is used to reduce the computations in coefficient multipliers by reusing most common bit patterns (BCSs). Two architectures

namely, constant shift method (CSM) and programmable shift method (PSM) are implemented for eliminating the common-sub expressions. The FIR filter design is based on transposed direct form method as shown in figure given below. These two architectures are placed in the place of multiplier generally used in filters i..e (b0,b1,b2,..bN).

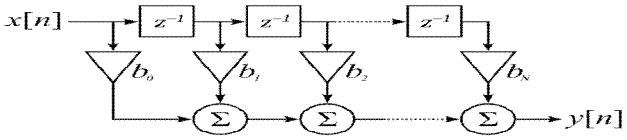

Fig-1. Trasposed Form FIR Filter

A. Architecture of CSM:

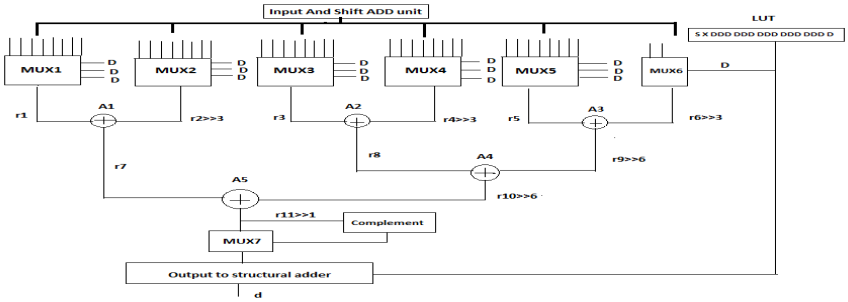

Fig .2 .Architecture of PE for CSM

The constant shift method architecture is designed as shown in figure.2 and the functions of the PE are explained detailed in [6]. The main problem in the CSM architecture is, if the number of bits increases, the number of adder steps in architectures also increases which increases the over-head in the circuitry, but compared to earlier designs this architecture is advantageous as it gives high-speed filters at the cost of little increase in area and power consumption. The CSM partition the filter coefficients into fixed number of groups in FIR filter. The earlier designs used a conventional shift and add unit but here the BCSs based shift and add unit is designed. The coefficients are divided into groups of 3 bits and send to the multiplexers as select signals (4 multiplexers are used here). In CSM four multiplexers are required and the shift and add unit is used four times; this in turn increases the additions.
The final shifter has the constant shifts in CSM architecture and the final shifter varies for different architectures. . The coefficients are directly stored in the look up table (LUT) and complete redundancy in coefficient multiplication is not avoided. If the output of any multiplexer becomes zero, the adder corresponding to the mux will be used, which is not necessary if the output is zero.

B. Architecture of PSM

The programmable shift method (PSM) is designed as shown in figure given below and detail explanation is given in [6]. The problems happen in the CSM architecture can be reduced in this architecture by pre-analysis part in which filter coefficients are analysed using the BCSE algorithm in earlier designs. The coefficients are stored in the coded format in the LUTs. The PSM does not have constant shifts, this can be the advantage compared to CSM and the shifts are programmable can have any shifted value based on the coefficient provided.

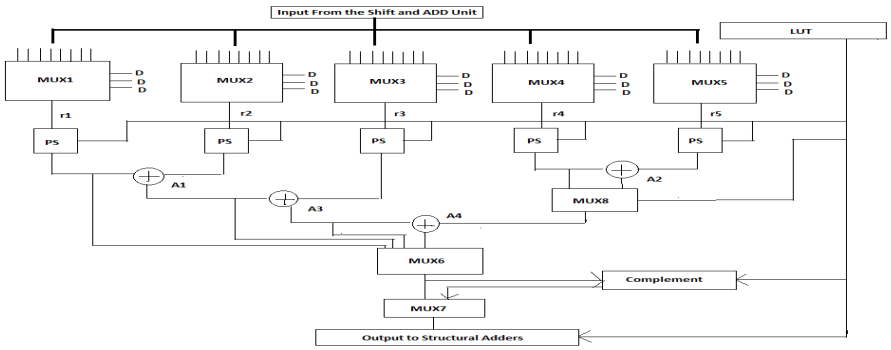

Fig .3. Architecture of PE for PSM

C. Architecture of VHBCSE:

The circuit diagram of vertical horizontal binary common sub-expression elimination (VHBCSE) algorithm is shown in below figure. To overcome the problem in CSM there are many techniques and VHBCSE algorithm is one among them. In a reconfigurable constant multiplier, the coefficient values can be dynamically programmable Therefore, the idea behind the reconfigurable multiplier is to consider the worst case (which involves the largest number of addition steps) whereby all the relatively better cases will also be taken care of. Hence, considering a reconfigurable multiplier having 16-bit input (X) and the 16-bit coefficient (H), the worst case condition will occur for the coefficient of values 16'HFFFF.

In VHBCSE algorithm, a 2-bit vertical BCSE has been applied first on the adjacent coefficient followed by 4-bit and 8-bit horizontal BCSEs to detect and eliminate and eliminate as many BCSs as possible which are present within each of the coefficient.

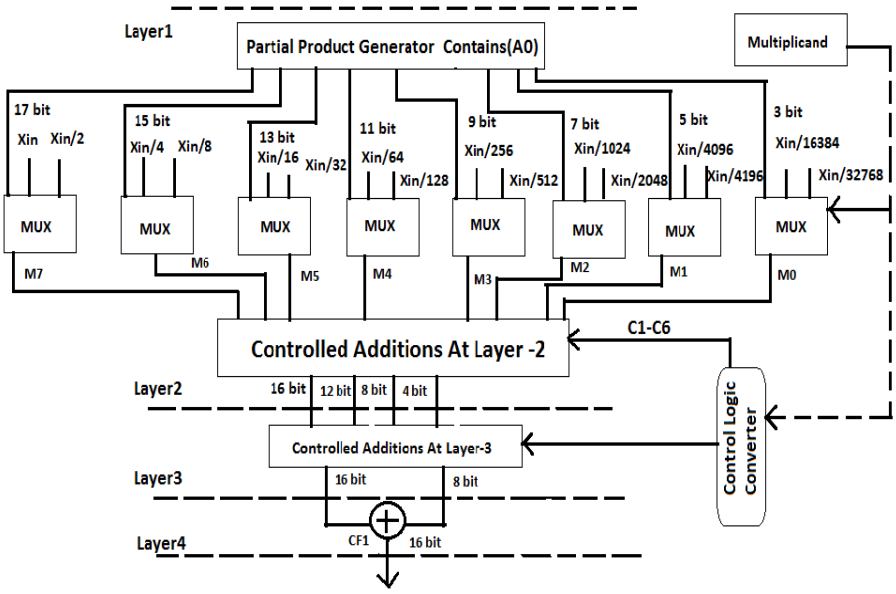

Fig .4. Reconfigurable Multiplier Architecture

IV. SIMULATION RESULTS

In this section, the design results of CSM, PSM and VHBCSE are presented and compared with [6], [7], and VHBCSE. The device utility for VHBCSE is as shown in below figure.

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	60	3,840	1%	
Number of occupied Slices	40	1,920	2%	
Number of Slices containing only related logic	40	40	100%	
Number of Slices containing unrelated logic	0	40	0%	
Total Number of 4 input LUTs	69	3,840	1%	
Number used as logic	60			
Number used as a route-thru	9			
Number of bonded IOBs	46	97	47%	
Average Fanout of Non-Clock Nets	2.05			

Fig .5. Simulation Results

The power consumption of VHBCSE is less compared to previous architectures as shown in table below.

Filter Length 20-Tap	Power(mW)		
	VHBSCE	2-bit BCSE[8]	3-bit BCSE [6]
Generic	3.58	4.30	6.27

Table -1: Power Comparisons Of Different Architectures.

V. CONCLUSION

The two architectures CSM, PSM and VHBCSE are designed using Verilog. The CSM architecture produces high speed filters and PSM produces low area and flexibility of changing the filter coefficients word length dynamically. These architectures are implemented for 20-tap FIR filter that has coefficients of 16-bit. VHBCSE Technique results in reduction of switching activity compared to the CSM and PSM, comparison of these two architectures results in reduction of power.

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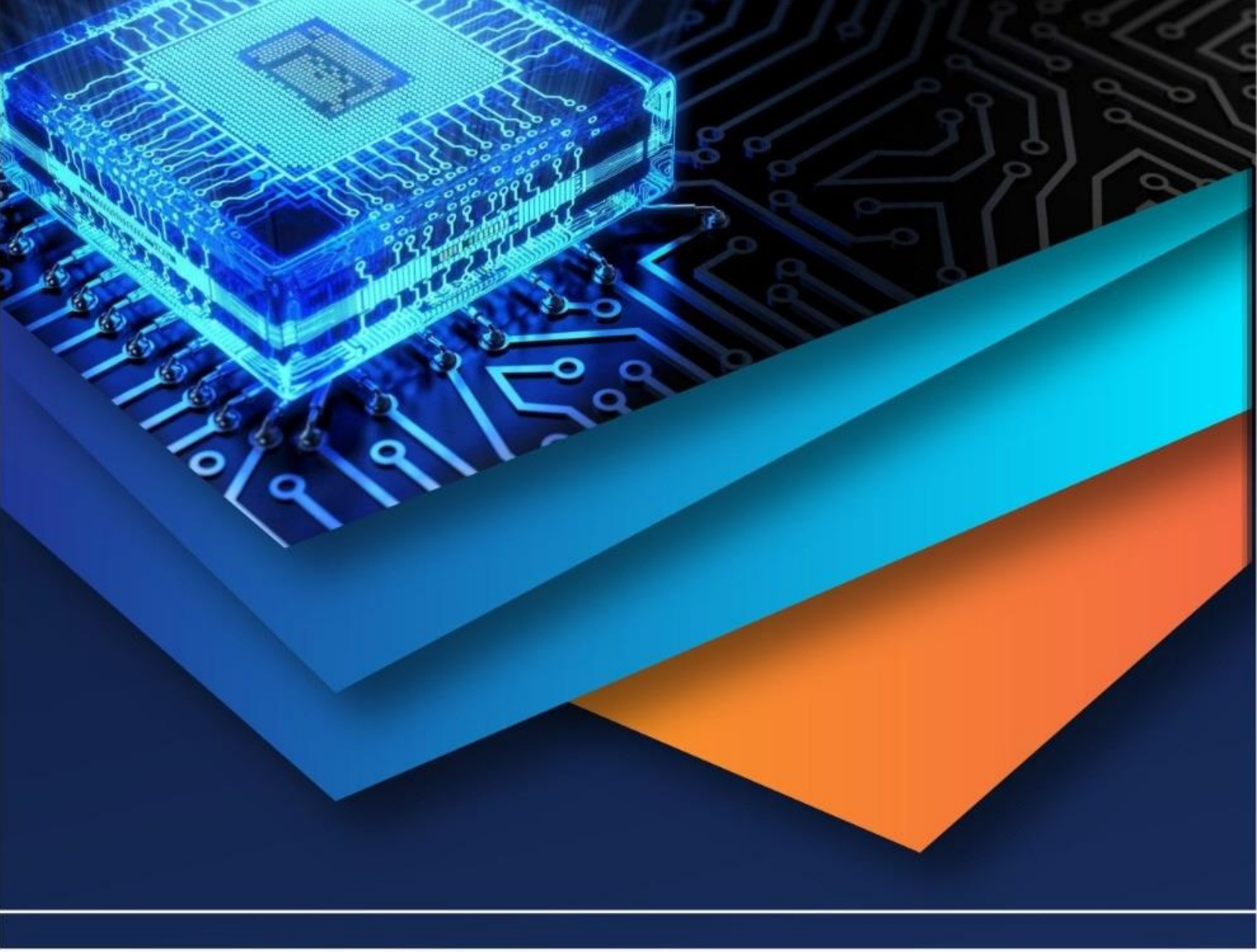

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