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An Extensive Evaluation of Futuristic Gate All Around Junctionless Nanowire MOSFET Using Numerical Simulation

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Abstract: This paper present an extensive review of homogeneously doped Junctionless Cylindrical Gate All Around (JL-C-GAA) MOSFET using numerical simulations to look into deep physical insight of the device. The electrical and analog/RF performance has been investigated. The JL-C-GAA FET is more immune to short channel effect than the devices having p-n junctions. It also offers steeper subthreshold slope than the inversion mode MOSFET. Device physics and band diagrams are also described in this paper as it has different principle of working from conventional MOSFET device having junctions. Atlas-3D device simulation tool has been used for the numerical simulations.

I. INTRODUCTION

Drastic reduction in channel length of planner MOSFET to achieve higher speed of operation and smaller size result in short channel effect like hot carrier effect, DIBL, gate leakage. These effects deteriorate the device performance in terms of device reliability. Conventional MOSFET [1-4] device are based on junctions (p-n junctions) which allows device to block or allow the current flow. But as the device physical dimensions are scaling down the nanometre regime the junction depletion width is a important factor. In case of nanoscaled device the junction depletion width is huge in comparison to device channel length. At nanoscale formation of ultrashap source and drain junction with high doping is a technological bottleneck. It also increases the complexity and cost of the fabrication. Another type of junction is metal-semiconductor junction (Schottky Barrier) [5]. Device based on Schottky Barrier junction called Schottky Barrier (SB) MOSFETs[5]. However the problem of junction depletion is not an issue in SB device but they suffers with a major problem of ambipolarity[6] in which at negative bias a n-MOS device starts acting as p-MOS. So for digital application it not appropriate. The possible futuristic solutions are junctionless MOSFET[7-11] which is based on the architecture of MOSFET originally proposed by Lilielfied [7-8] in 1925. The proposed device is a simple resistor, and when the gate voltage is applied on it allows the carriers to deplete and hence inflecting the device conductivity. As it is desired to work this device similar to MOSFET it is necessary that ideally device should be fully depleted the semiconductor carriers so it can offer infinite resistance in off state. Unfortunately in the absence of technology in late 1925 it could not be possible to fabricate this device.

J. P. Colinge, et.al., [9-10] fabricated the device called junctionless MOSFET in 2010. The device has uniformly doped n+ thought the source-channel-drain. Hence their is no gradient of doping concentration and no diffusion take place which results in cost effectiveness as the ultrafast annealing technique is not required and device can be made even at shorter channel length. Two essential requirements for the Junctioless device[9-11] are : (1) Higher doping is required to offer reasonable amount of on current, (2) device diameter should be thin enough to be fully depleted of carriers so the device remain of in its initial stage [2 Junctionless MOSFET].

Even though the junction related problems can be solved using the Junctionless device architecture but to further suppress the short Channel Effects (SCEs) many multigate MOSFET devices e.g. dual gate[11-14] pigate, omega gate, quadruple gate, Gate All Around (GAA)[11-14] has been proposed and extensively investigated. Among all of them gate all around is the best solution since these provides the all around control of the channel. The rectangular structure leads to the corner effect, cylindrical structure give the best way to get rid of this problem and also improve the SCE. In cylindrical GAA [11] MOSFET gate surrounds the silicon pillar completely and therefore controls the channel potential in a more effective way resulting in increased immunity to short channel effect, hot carrier effect DIBL, leakage current etc.[11-14]. This paper extensively investigate and summarize the Cylindrical Junctionless GAA MOSFET using the numerical simulations. The Analog/RF [15-19] performance at different channel length is investigated.

II. DEVICE STRUCTURE AND OPERATION PRINCIPLE OF JUNCTIONLESS GAA

A. Structure of Cylinderical Junctionless transistor and Simulation

Figure 1 a. shows the 3 D view of Cylindrical Junctionless Gate All Around MOSFET. Figure 1 b. shows ht e cross sectional view of Junctionless GAA MOSFET. The models incorporated in simulations are: Auger recombination model for Direct transition of three carriers, CONSRH uses concentration dependent lifetimes, CONMOB model for concentration dependent mobility, FLDMOB model for high electric field velocity saturation, CVT model for perpendicular electric field, FERMI carriers statics for electron and holes, BGN model to correctly model the bipolar current gain. Newton-Gummel method has been adopted for numerical solution. The quantum effect [20] has not been taken in to consideration in present analysis. ATLAS-3D[21] device simulation tool for the numerical simulation.

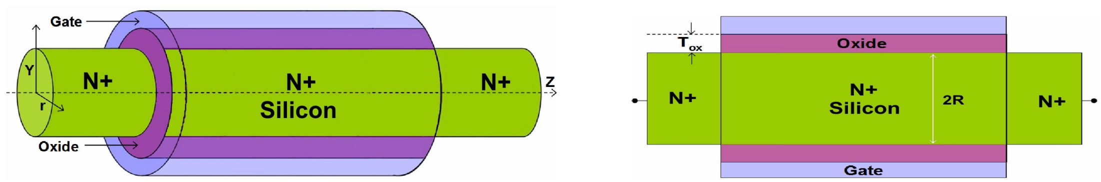

Fig. 1.(a) 3D View of Junctionless GAA MOSFET, (b) Cross sectional view of the Junctionless GAA MOSFET, Gate length L = 16, 20, 30, 40 nm, Radius of Si pillar t_{Si} = 10 nm , Doped n-type substrate N_D =1 × 10^{18} cm^{-3}, SiO_2 thickness t_{ox} = 2 nm, dielectric permittivity of SiO_2 is ε_{ox} = 3.9, work-function of the metal gate electrode Φ_m = 5 eV. These are device nominal parameters for complete work unless otherwise stated.

B. Band diagram of Cylindrical Junctioless GAA

Figure 2 shows the energy band diagram of the Junctionless. Figure2.(a) shows the device on state in which all the bands are flat. Normally n type silicon pillar is a conduction nanowire and it follows

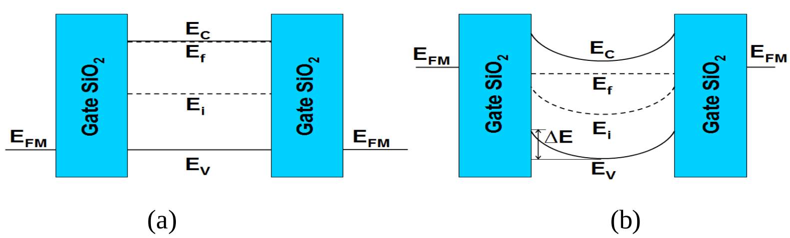

Fig. 2.Energy-Band diagram of n-channel JL MOSFET, (a) Flat Band (device on condition), (b) in off state channel is fully depleted [7]

the band diagram same as figure a, but as the gate terminal is formed the device is fully depleted. One thing which is to be noticed that the device radius must be thin enough to be fully depleted. When the device is fully depleted the band structure is looks alike in figure2(b). As the gate voltage is applied the device energy level again aligned at the same level and the device is turned on.The concentration of electrons in n-type junctionless MOSFET is shown in figure 3 [9].

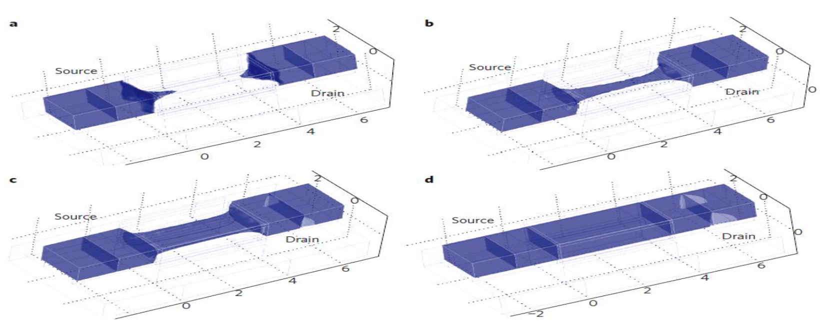

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Fig. 3.Electron concentration contour plots in an n-type junctionless gated resistor.(a) below threshold (V_{th}) the channel region is depleted of electrons; (b) at threshold a string-shaped channel of neutral n-type silicon connects source and drain; (c) above threshold the channel neutral n-type silicon expands in width and thickness; (d) when a flat energy bands situation is reached the channel region has become a simple resistor [9].

III. RESULTS AND DISCUSSION

The results are divided in to three parts part A. describes the electrical characteristic of Cylindrical Junctionless Gate All around MOSFET [8]. Part B presents the Analog/RF [12-15]performance of the device. In part C, Gains of the device are investigated. All these results are investigated at different channel length and different radius.

A. Electrical Characteristics

Figure 4 a. shows the variation of drain current as a function of applied gate voltage at applied drain bias V_{DS} of 0.5 V.

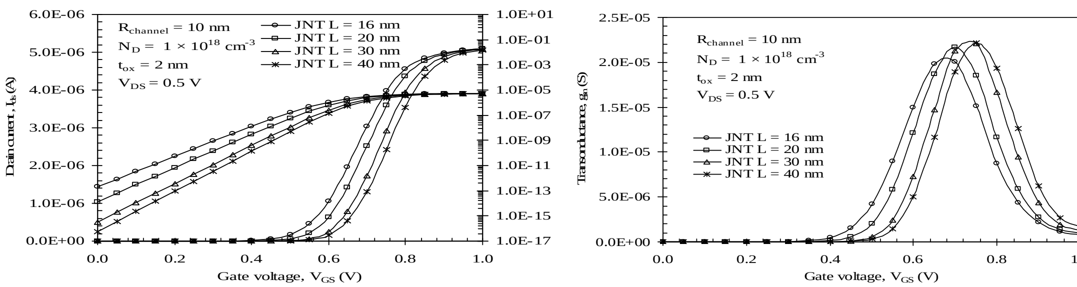

Fig. 4.(a) Variation of drain current , (b) Variation of transconductance; as function of applied gate voltage V_{GS} at applied drain bias V_{DS} = 0.5 V.

It clearly shows that at all channel lengths device on current (I_{on}) is almost same and even at short channel lengths below 20 nm device offers good off current (I_{off}). However drive current to off state current ratio of the device reduces at shorter channel length but it is still acceptable. Figure 4 b. depicts the variation of transconductance (g_m) as a function of applied gate voltage at applied drain bias V_{DS} of 0.5 V. The high value of transconductance can be clearly observed and as the channel length reduces device shows lesser reduction in g_m. For 30 and 40 nm channel length peak transconductance value is same and very less variation when going 20 nm to 16 nm range. Drain current variation as a function of applied drain voltage is shown in figure 5 a. at a applied gate bias V_{GS} of 1.0 V. Device offers same current for all the channel lengths, this shows that device is very immune to short channel effects. Figure 5 b. shows the variation of output conductance (g_d) as a function of applied drain voltage. It shows that there is very marginal variation in g_d while reducing the channel length. It is the result of no source drain junction resistance so it offers almost similar g_d for all observed channel lengths.

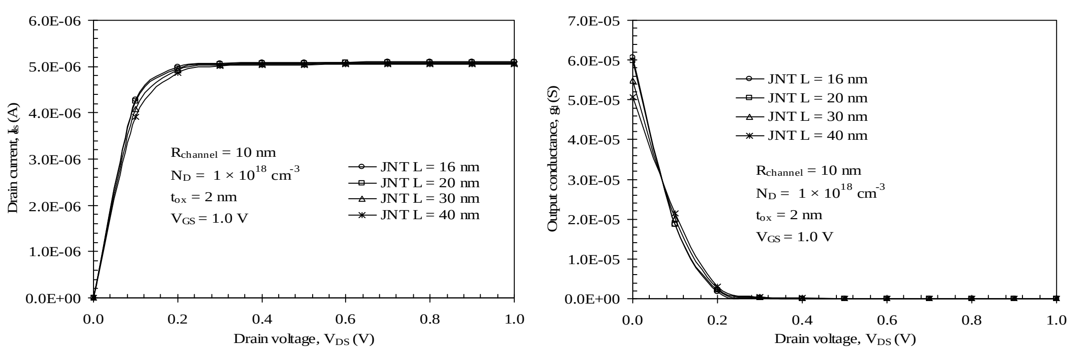

Fig. 5.(a) Variation of drain current, (b) Variation of output conductance; as function of applied drain voltage V_{DS} at applied gate bias V_{GS} = 0.5 V.

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B. Analog/RF Performance

An important parameter to investigate analog performance of a device is device efficiency defined as ratio of transconductance to drain current (g_m/I_{ds}) also called Transconductance Generation Factor (TGF). Higher g_m/I_{ds} indicates stronger capability of the device to convert dc power in to ac gain performance at a certain drain bias. Figure 6 a. shows the variation of TGF as a function of applied gate voltage. Figure 6 b. shows the variation of cut off frequency. Device at all channel lengths offers frequency in Gega-Hertz range so good candidate for high frequency applications.

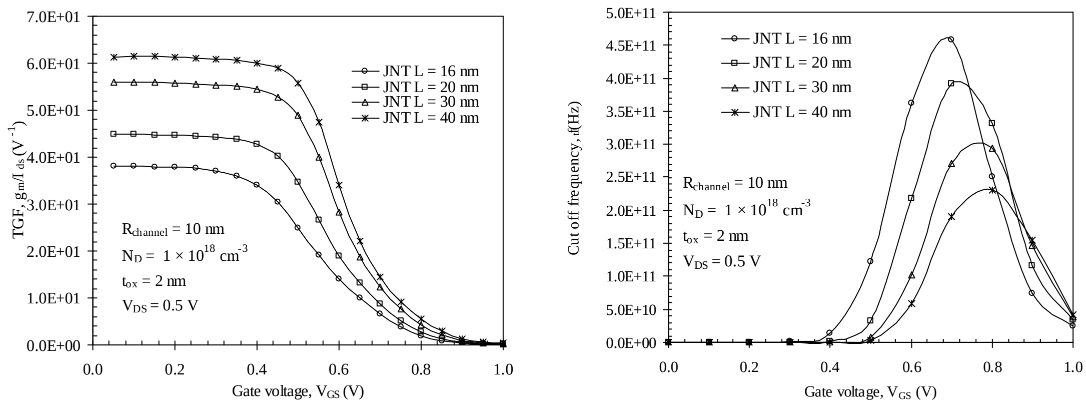

Fig. 6.(a) Variation of Transconductance Generation Factor (TGF), (b) Variation of Cut off frequency (f_t); as function of applied gate voltage V_{GS} at applied drain bias V_{DS} = 0.5 V.

C. Current Gain

Figure 7a. shows the current gain of the device at different channel length. Higher value of early voltage is required for the high open loop device gain (A= V_{EA}·TGF). Figure 7 b. shows variation of early voltage as a function of applied drain voltage and device offer good V_{EA}.

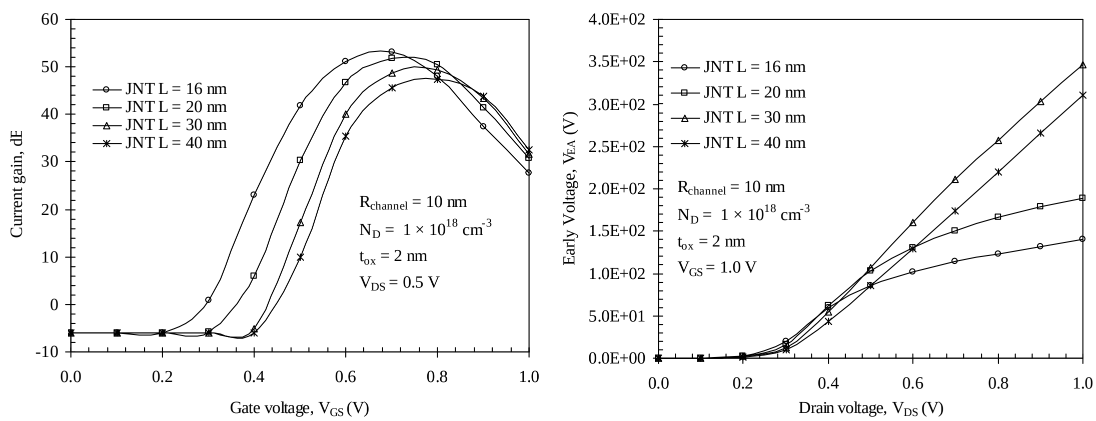

Fig. 7.(a) variation of Current Gain, as function of applied gate voltage V_{GS} at applied drain bias V_{DS} = 0.5 V. (b) variation of Early Voltage as function of applied drain voltage V_{DS} at applied gate bias V_{GS} = 0.5 V.

D. Device Perfromance metrices

DIBL is the measure of the effect of drain bias on the threshold voltage which depends on the minimum surface potential region in the channel. And can be given as:

$$\text{DIBL} = \left| \frac{V_{th}(\text{high } V_{DS}) - V_{th}(\text{low } V_{DS})}{\text{High } V_{DS} - \text{Low } V_{DS}} \right|$$

The DIBL at different channel length has been obtained and summarized in table 1. Subthreshold Slope is the measure of the device speed and the fundamental limit of the SS for MOSFET device is 60~70 mV/decade. The Cylindrical Junctional GAA MOSFET offers steeper subthreshold slop close to the fundamental limit of SS even at shorter channel lengths. All the results are tabulated in table 1.The device also offer higher value of I_{on}/I_{off} ratio which is very essential parameter for the digital applications.

TABLE I.
TABLE STYLES

Performance metrces	**Junctionless Gate All Around MOSFET with 10 nm channel radius**			
	JNT 16 nm	***JNT 20 nm***	***JNT 30 nm***	***JNT 40 nm***
Subthreshold Slope (SS)	82 mV/decade	74 mV/decade	65 mV/decade	62 mV/decade
DIBL	123 mV/V	65 mV/V	34 mV/V	12 mV/V
Ion/Ioff	2.46E+07	3.76E+08	1.52E+10	8.67E+10

IV. CONCLUSION

Cylindrical Junctionless GAA MOSFET device at various channel length has been demonstrated and their analog/RF performance has been compared. The device physics of the Junctionless GAA MOSFET has also been presented. Due to reduced Short Channel effects and DIBL with reduced complexity of fabrication Junctionless GAA is promising candidate for the future device size reduction. It also offers the stepper subthreshold slope so the device operates at higher speed. The I_{on}/I_{off} ratio is also very good even at shorter channel lengths so the device can perform excellent for digital application.

V. ACKNOWLEDGMENT

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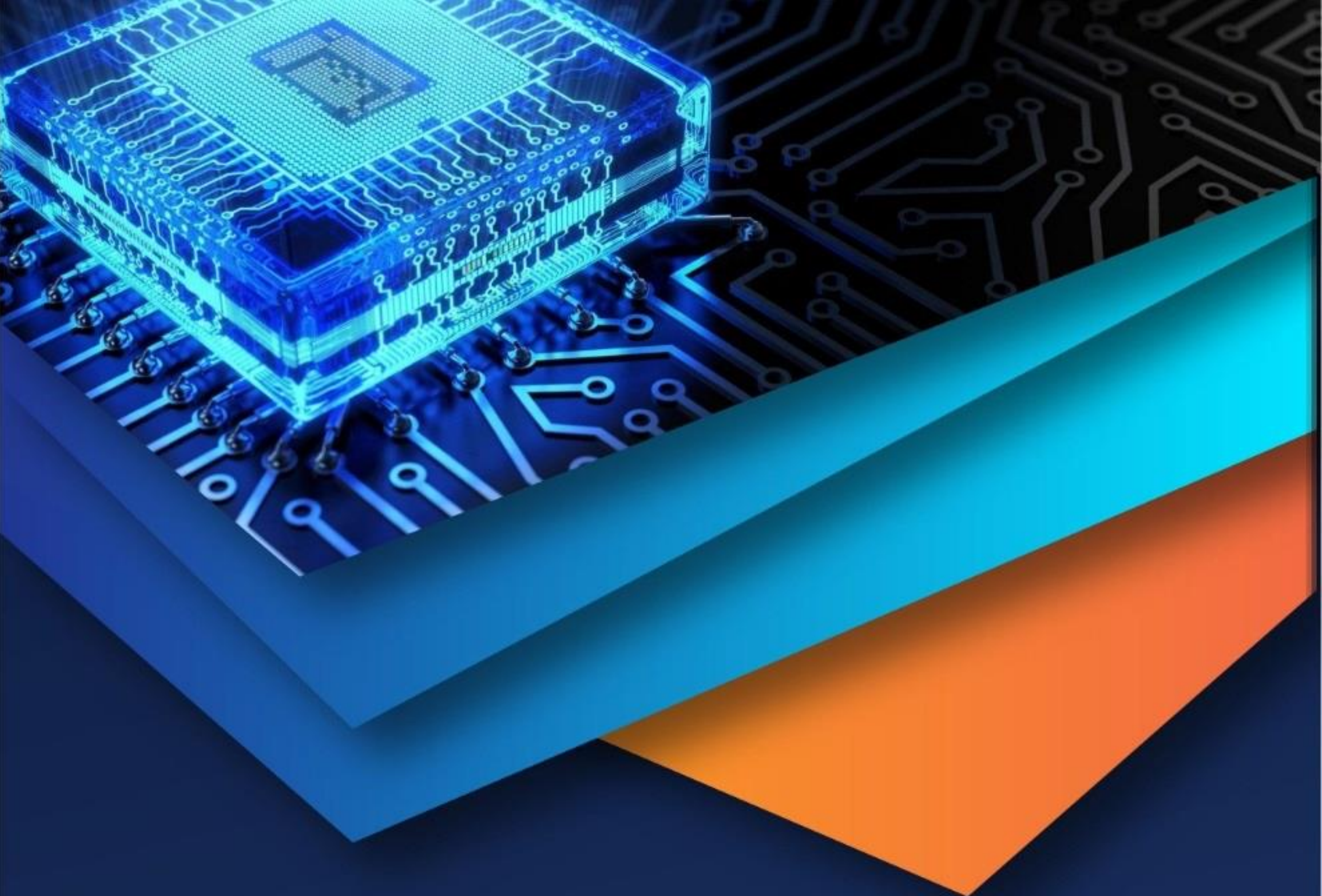

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