iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: Issue **Issue:** ssue-1 **Month of publication:** October 2014

DOI:

www.ijraset.com

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Special Issue-1, October 2014
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology(IJRASET)

Implementation of HDLC Protocol Using Verilog

K. Durga Bhavani[1], B. Venkanna[2], K. Gayathri[3]

[1,2,3]*Dept. of ECE*
[1,2]*RGUKT-Basar*
[3]*Intell Engg. College-Anatapur*

Abstract— A protocol is required to transmit data successfully over any network and also to manage the flow at which data is transmitted. HDLC protocol is the high-level data link control protocol established by International Organization for Standardization (ISO), which is widely used in digital communications. High-level Data Link Control (HDLC) is the most commonly used Layer2 protocol and is suitable for bit oriented packet transmission mode. This paper discusses the Verilog modeling of single-channel HDLC Layer 2 protocol and its implementation using Xilinx.

Keywords- High –Level Data link Control (HDLC), Frame Check Sequence (FCS), and Cyclic Redundancy Check (CRC)

I. INTRODUCTION

HDLC protocol is the high-level data link control protocol established by International Organization for standardization (ISO), which is widely used in digital communication and are the bases of many other data link control protocols [2]. HDLC protocols are commonly performed by ASIC (Application Specific Integrated Circuit) devices, software programming and etc.

The objective of this paper is to design and implement a single channel controller for the HDLC protocol which is the most basic and prevalent Data Link layer synchronous, bit-oriented protocol. The HDLC protocol (High –Level Data link Control) is also important in that it forms the basis for many other Data Link Control protocols, which use the same or similar formats, and the same mechanisms as employed in HDLC.

HDLC has been so widely implemented because it supports both half duplex and full duplex communication lines, point to point(peer to peer) and multi-point networks[1]. The protocols outlined in HDLC are designed to permit synchronous, code-transparent data transmission. Other benefits of HDLC are that the control information is always in the same position, and specific bit patterns used for control differ dramatically from those in representing data, which reduces the chance of errors.

II. HDLC PROTOCOL

The HDLC Protocol Controller is a high-performance module for the bit-oriented packet transmission mode. It is suitable for Frame Relay, X.25, ISDN B-Channel (64 Kbits/s) and D-Channel (16 Kbits/s) The Data Interface is 8-bit wide, synchronous and suitable for interfacing to transmit and receive FIFOs. Information is packaged into an envelope, called a FRAME [4]. An HDLC frame is structured as follows:

FLAG	ADDRESS	CONTROL	INFORMATION	FCS	FLAG
8 bits	8 bits	8 /16 bits	variable	8	8 bits

Table 1. HDLC Frame

A. Flag

Each Frame begins and ends with the Flag Sequence which is a binary sequence 01111110. If a piece of data within the frame to be transmitted contains a series of 5 or more 1's, the transmitting station must insert a 0 to distinguish this set of 1's in the data from the flags at the beginning and end of the frame. This technique of inserting bits is called bit-stuffing [3].

B. Address

Address field is of programmable size, a single octet or a pair of octets. The field can contain the value programmed into the transmit address register at the time the Frame is started.

C. Control

HDLC uses the control field to determine how to control the

communications process. This field contains the commands, responses and sequences numbers used to maintain the data flow accountability of the link, defines the functions of the frame and initiates the logic to control the movement of traffic between sending and receiving stations.

D. Information or Data

This field is not always present in a HDLC frame. It is only present when the Information Transfer Format is being used in the control field. The information field contains the actually data the sender is transmitting to the receiver.

E. FCS

The Frame Check Sequence field is 16 bits. The FCS is transmitted least significant octet first which contains the coefficient of the highest term in the generated check polynomials. The FCS field is calculated over all bits of the addresses, control, and data fields, not including any bits inserted for the transparency. This also does not include the flag sequence or the FCS field itself. The end of the data field is found by locating the closing flag sequence and removing the Frame Check Sequence field (receiver section) [5].

III. HDLC Module Design

In this design, HDLC procedures contain two modules, i.e. encoding-and-sending module (Transmitter) and receiving-and-decoding module (receiver). The function diagram is shown as below.

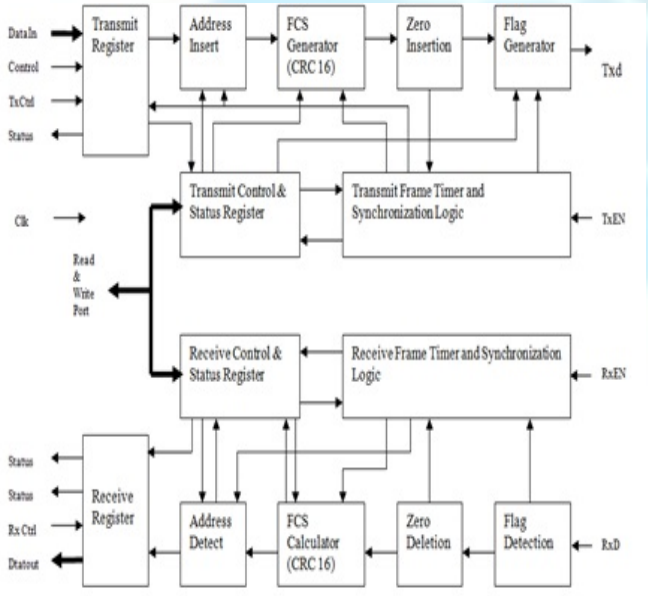

Fig.1. HDLC Block Design

Form this diagram we know that, transmitter module includes transmit register unit, address unit, FCS generation unit, zero insertion unit, Flag generation unit, control and status register unit and transmit frame timer and synchronization logic unit. Receiver module includes receive register unit, address detect unit, FCS calculator unit, zero detection unit, flag detection unit, receive control and status register unit and frame timer and synchronization logic unit.

A. Transmitter Module

The Transmit Data Interface provides a byte-wide interface between the transmission host and the HDLC Controller. The Transmit data is loaded into the controller on the rising edge of Clock when the write strobe input is asserted. The Start and End bytes of a transmitted HDLC Frame are indicated by asserting the appropriate signals with the same timing as the data byte.

The HDLC Controller will, on receipt of the first byte of a new packet, issue the appropriate Flag Sequence and transmit the Frame data calculating the FCS. When the last byte of the Frame is seen the FCS is transmitted along with a closing Flag. Extra zeros are inserted into the bit stream to avoid transmission of control flag sequence within the Frame data.

The Transmit Data is available on TxD pin with appropriate to be sampled by Clk. If TxEN is de-asserted, transmit is stalled, and TxD pin is disabled.

A transmit control register is provided which can enable or disable the channel. In addition it is possible to force the transmission of the HDLC Abort sequence. This will cause the currently transmitted Frame to be discarded. The transmit section can be configured to automatically restart after an abort, with the next frame, or to remain stalled until the host microprocessor clears the abort.

B. Receiver Module

The HDLC Controller Receiver accepts a bit stream on port RxD. The data is latched on the rising edge of Clock under the control of the Enable input RxEN. The Flag Detection block searches the bit stream for the Flag Sequence in order to determine the Frame boundary. Any stuffed zeros are detected and remove and the FCS is calculated and checked. Frame data is placed on the Receive Data Interface and made available to the host. In addition, Flag information is passed over indicating the Start and the End byte of the HDLC Frame as well as showing any error conditions which may have been detected during receipt of the Frame.

In normal HDLC protocol mode, all Receiver Frames are presented to the host on the output register. A status register

is provided which can be used to monitor status of the Receiver Channel, and indicate if the packet currently being received includes any errors.

IV. RESULTS

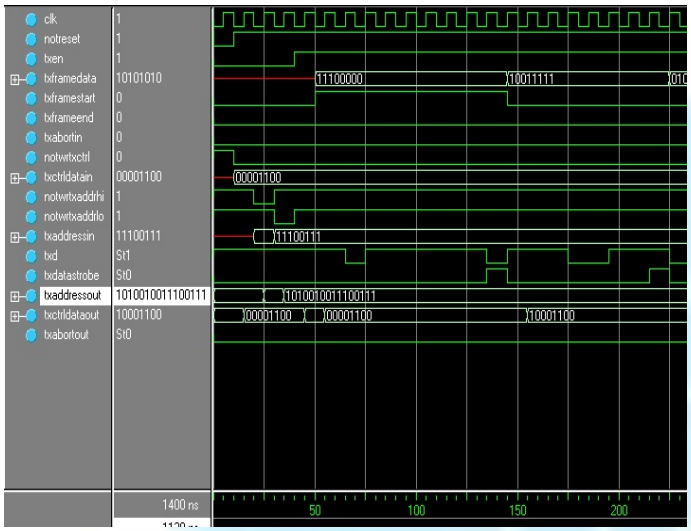

Fig.2. Simulation Waveform

Device Utilization Report: Clock Frequency: 78.2 MHz

Resource	Used	Avail	Utilization
IOs	60	180	33.33%
Function Generators	205	1536	13.35%
CLB Slices	103	768	13.41%
Dffs or Latches	108	1536	7.03%

Table 2. Synthesis Report

V. CONCLUSION

We designed HDLC protocol sending and receiving RTL level modules in Verilog and had them tested successfully, which has the following advantages like easy to program and modify, suitable for different standards of HDLC procedures, match with other chips with different interfaces. So this proposed method can be more useful for many applications like a Communication protocol link for RADAR data processing.

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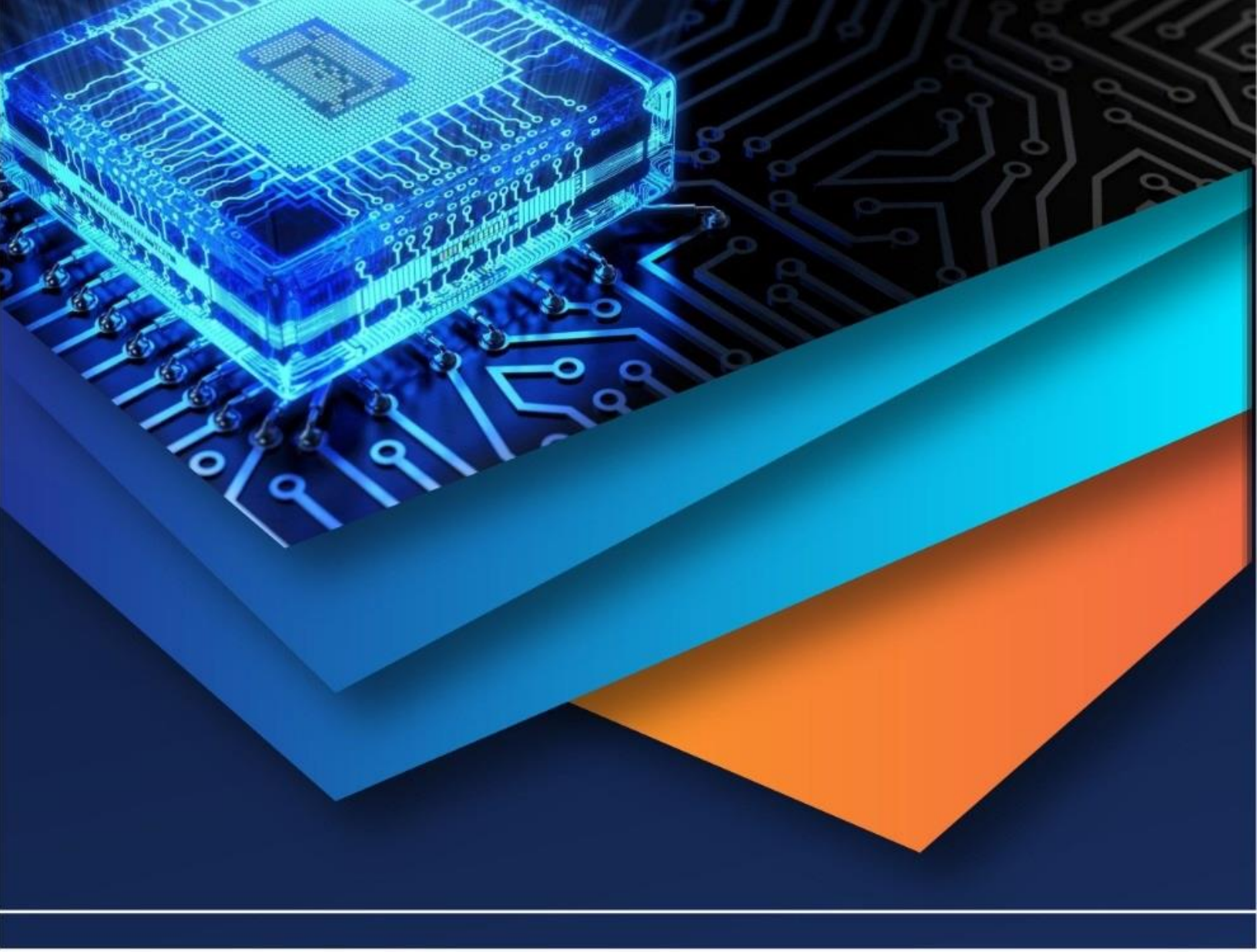

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