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Simulation Analysis of Three, Five, Thirteen, Fifteen, Twenty One and Thirty One Level Cascaded H-Bridge Multilevel Inverter

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Abstract: Multilevel inverters (MLI) becomes more accepted over the last few years in high power application of electrical engineering with the advantage of less disturbances and the possibility to work at lower switching frequencies as compared to conventional two-level inverters. In this paper the simulation of single phase multilevel inverter is present. Simulation of three level, five level, seven level, nine level, eleven level, thirteen level and fifteen level inverters are done in MATLAB. These different level inverters are realized by neutral point clamped (NPC) or diode clamped topology of multilevel inverter. In this paper pulse width modulation control strategy is used for control the switches at appropriate conducting angles. The comparative results are presented for multilevel inverter up-to fifteen level which shows the total harmonic distortion is reduces as the number of level increases.

I. INTRODUCTION

Multilevel converters (or inverters) have been used for dc-to-ac power conversion in high power applications such as utility and large motor drive applications. Multilevel inverters provide more than two voltage levels.

A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. There are three major multilevel topologies: cascaded, diode-clamped, and capacitor-clamped [l-11]. For the number of levels (M) or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. Instead, each voltage level can be supported by a capacitor and proper control [6-7, 1].

However, for M>3 and applications involved in active power transfer, such as motor drives, these multilevel converters all require either isolated dc power sources or a complicated voltage balancing circuit and control to support and maintain each voltage level [7]. In this aspect, the three existing multilevel converters are neither operable nor complete for real (active) power conversion because they all depend on outside circuits for voltage balancing. For the number of levels (M) no greater than 3 (i.e., M13), or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level.

The purpose of this paper is to increase the voltage level to achieve sinusoidal waveform & compare different voltage level by increasing the level through simulation.

II. TOPOLOGIES OF MULTILEVEL INVERTER HAVE BEEN INVESTIGATED IN THE LITERATURE.

A. Flying Capacitor Multilevel Inverter (FCMLI)

Many capacitors are required which makes this topology heavy and cumbersome. In this, load cannot be directly connected to generate the zero voltage level. Instead, the zero level is obtained by connecting the load to the positive or negative bar through the flying capacitor with opposite polarity with respect to the dc-link [4] as shown in Fig.1a.

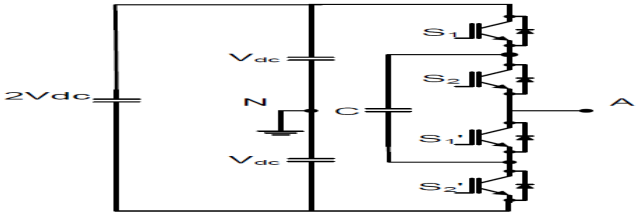

Figure 1a.A 3-level flying capacitor inverter[4]

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B. Diode-Clamped Multilevel Inverter

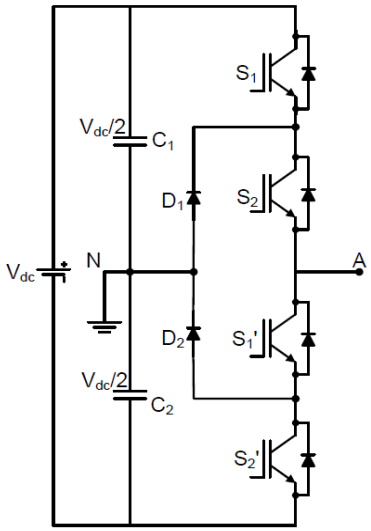

Figure 1b. A 3-level Diode-clamped inverter [4]

Diode-clamped multilevel inverter as shown in Fig.1b is the name given based on neutral-point clamped PWM inverter proposed to higher number of levels. The diode-clamped multilevel inverter has been wide accepted for its capability for high voltage with high efficiency in a efficient operation. An NPC-MLI inverter is mainly composed of two traditional two-level VSIs connected one over the other with the required modifications.

Here the name diode clamped (DC) makes more sense, since there are more voltage-level clamping nodes than only connected to the neutral N. As far as the main concern is the number of clamping diodes needed to share the voltage which is increased dramatically. This fact makes it difficult to control the unbalancing problem in the dc-link capacitor [6]. It is the most commonly used topology in the industry for a number of levels equal to three. An NPC-MLI inverter is mainly composed of two traditional two-level VSIs connected one over the other with the required modifications [4].

C. Cascaded H-Bridge Multilevel Inverter PWM H-Bridge

CHB-MLIs shown in Fig.1c are formed by the back to back series connection of two or more single-phase H-bridge inverters, hence as the name suggest cascade [11]. Each cascade H-bridge corresponds to voltage source in each bridge,. Therefore, a single H-bridge converter is able to generate three different voltage levels. And series connection of N such bridges will be able to produce 2N+1 levels in the output of the inverter. This series connection is known as cascaded H-bridge multilevel inverter [4].

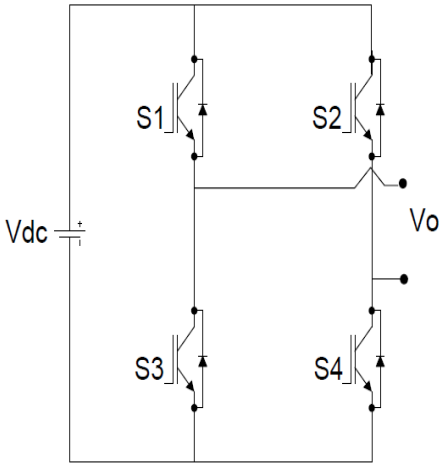

Figure 1c A 3-level cascaded H-bridge inverter[4]

The multilevel inverters perform power conversion in multi- level voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability Considering these advantages multilevel inverters have been gaining considerable popularity in recent years.

Comparing with two level inverter system having the same power, multilevel inverters has the advantages that the lower harmonic components on the output voltages, Electro Magnetic Interference (EMI) problem could be decreased much as given in Table 1. Due to these merits, many studies about multilevel inverters have been performed at simulation level [5].

III. DETAILED ANALYSIS OF CASCADED H-BRIDGE MULTILEVEL INVERTERS (CHB-MLI)

An alternative multilevel inverter topology with less power devices requirement compared to previously mentioned topologies is known as cascaded H-bridge multilevel inverter (CHB-MLI) and the topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. Owing to this property, CHB-MLIs have also been proposed to be used with fuel cells or photovoltaic arrays in order to achieve higher levels [8,11].

The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generates three voltage levels as $+V_{dc}$, 0, $-V_{dc}$ by connecting the DC source to the AC output by different combinations of four switches, S_{A1}, $S_{A1}{}^{1}$, S_{A2}, and $S_{A2}{}^{1}$ as seen in first cell of Fig. 2. The CHB-MLI that is shown in Fig.2 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain $+V_{dc}$, S_{A1} and $S_{A2}{}^{1}$ switches are turned on, whereas - Vdc level can be obtained by turning on the S_{A2} and $S_{A1}{}^{1}$. The output voltage will be 0 by turning on S_{A1} and S_{A2} switches or $S_{A1}{}^{1}$ and S_{A2} switches. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as seen in Eq. (4). The switching states of a CHB-MLI (sw) can be determined by using Eq. (4)

$$m = 2n+1 \quad (1)$$

$$sw = 3^{m} \quad (2)$$

The first leg phase voltage (V_{an}) of Fig. 2 is constituted by multiplying V_{a1} and V_{a2} values of series connected H-bridge cells and will generate a stepped waveform as seen in Fig. 3.

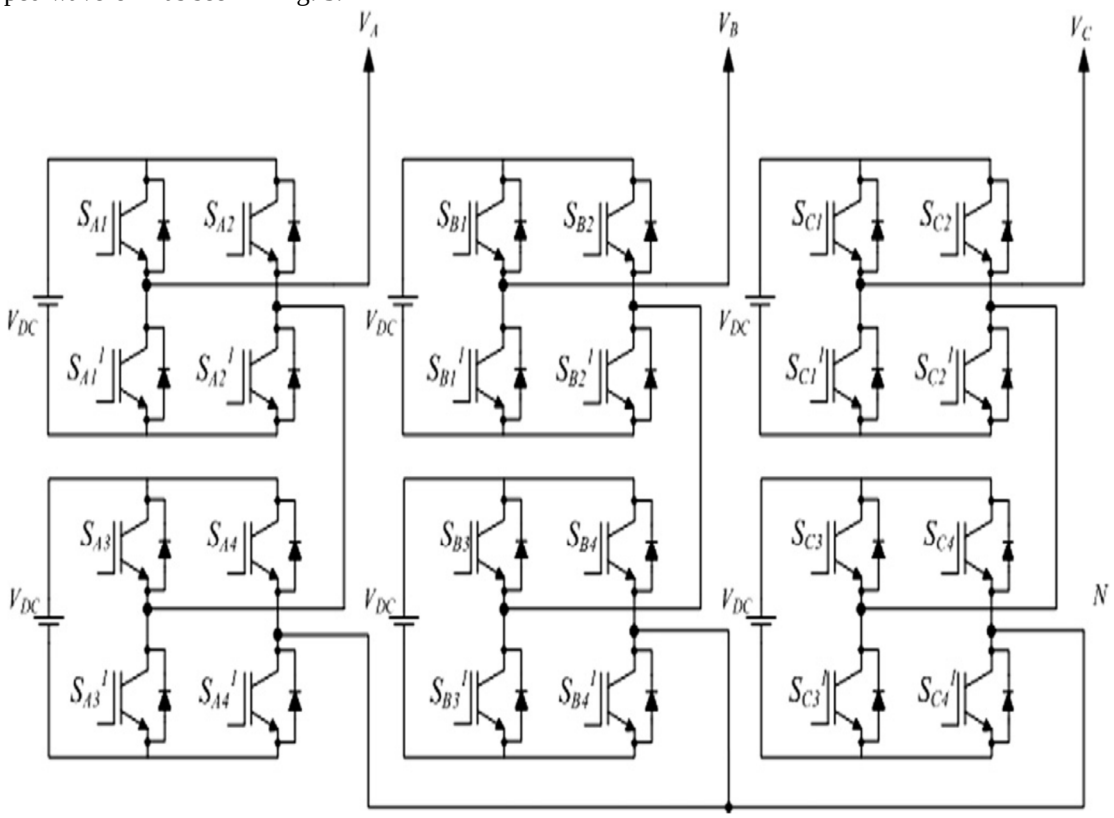

Fig. 2. Three-phase five-level topology of cascaded H-bridge multilevel inverter

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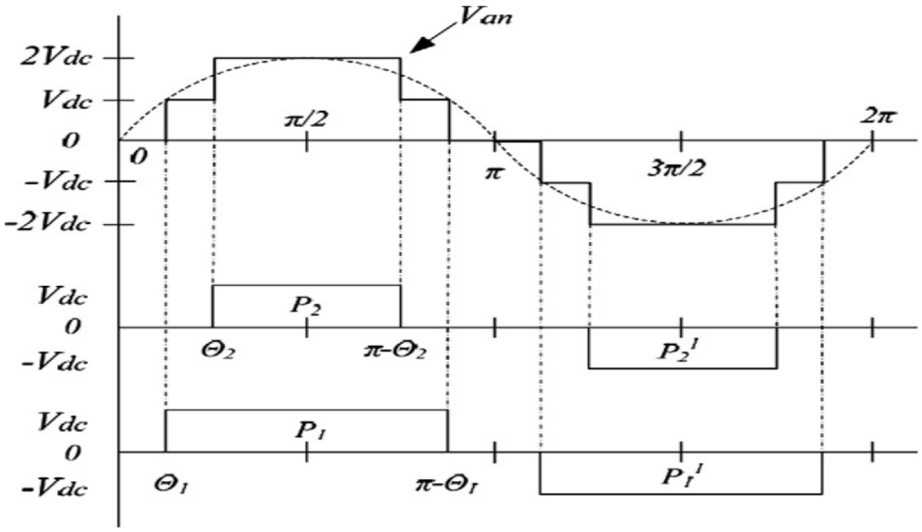

Fig. 3. Phase output voltage waveforms of a five-level topology CHB-MLI with two separate DC sources

Positive output pulses are shown with P_1 and P_2 while the negative ones are indicated as P_1^1 and P_2^1. The Fourier series expansion of the general multilevel stepped output voltage is shown in Eq. (6) and the transform is applied for Fig. 3 in Eq. (7), where n is the harmonic number of the output voltage of inverter.

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_5)] \frac{\sin(n\omega t)}{n} \quad (6)$$

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2)] \frac{\sin(n\omega t)}{n} \quad (7)$$

IV. COMPARISON OF CONVENTIONAL TWO LEVEL AND MULTILEVEL INVERTERS

CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources. There are numerous studies have been performed on CHB-MLIs for connecting renewable energy sources with AC grid and power factor correction.

Table 1 Comparison of conventional two level inverters and multilevel inverters [5].

S. No	Conventional inverter	Multilevel inverter
1	Higher THD in output voltage	Low THD in output voltage
2	More switching stresses on devices	Reduced switching stresses on devices
3	Not applicable for high voltage applications	Applicable for high voltage applications
4	Higher voltage levels are not produced	Higher voltage levels are produced
5	Since dv/dt is high, the EMI from system is high	Since dv/dt is low, the EMI from system is low
6	Higher switching frequency is used hence switching losses is high	Lower switching frequency can be used and hence reduction in switching losses
7	Power bus structure, control schemes are simple	Control scheme becomes complex as number of levels increases
8	Reliability is high	Reliability can be improved, rack swapping of levels is possible

V. SIMULATION MODEL AND RESULT ANLYSIS

Simulation is done in MATLAB to obtain the operation of multilevel inverter up-to thirty-one level. Figure 4.1 shows the model which is developed in MATLAB for a three level inverter. Subsystem shown in figure 4.2 represents the control strategy for switches.

A. Case 1: A 3-Level Cascaded H-bridge Multi level Inverter

Three phases H-bridge type three level inverter employing different multi carrier single reference modulation schemes is shown in Fig 4.1. The subsystems for this figure are shown similar to that of a flying capacitor type design and hence not shown. The capacitor rating is 2200 micro farads and input DC voltage is 30V and output AC is 62V Ph-N.

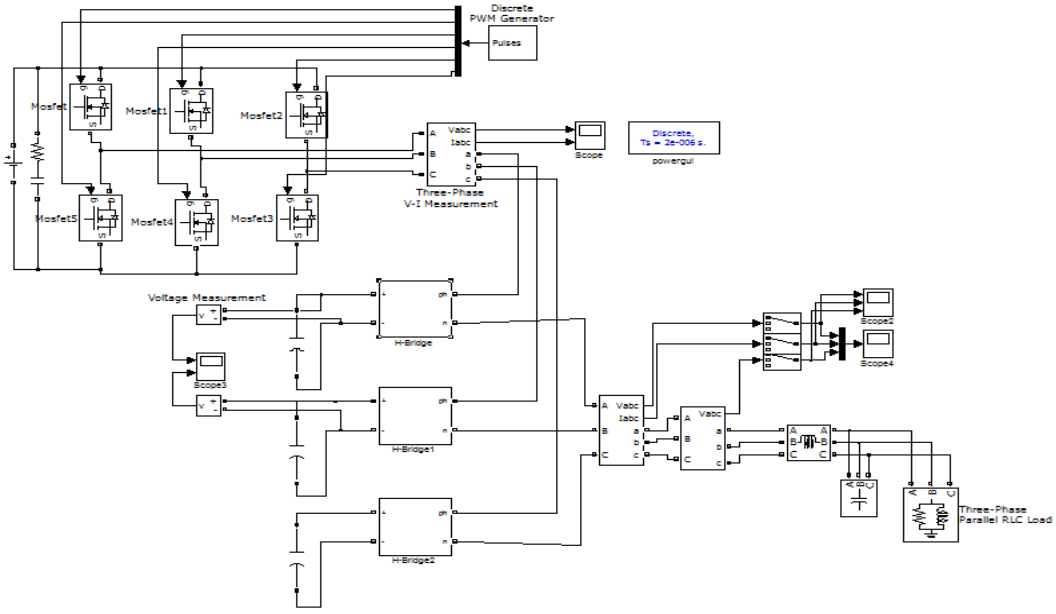

Fig 4.1 Simulink model of Three-phase 3-level Cascaded H-bridge Multi level inverter

The output waveforms for three level H-bridge type construction is shown in Fig 4.2. In this figure top part shows, phase to neural voltage and is 62Volts peak and middle part of figure is for current which is 40A peak and the bottom figure shows phase to phase voltage nearly 100 Volts.

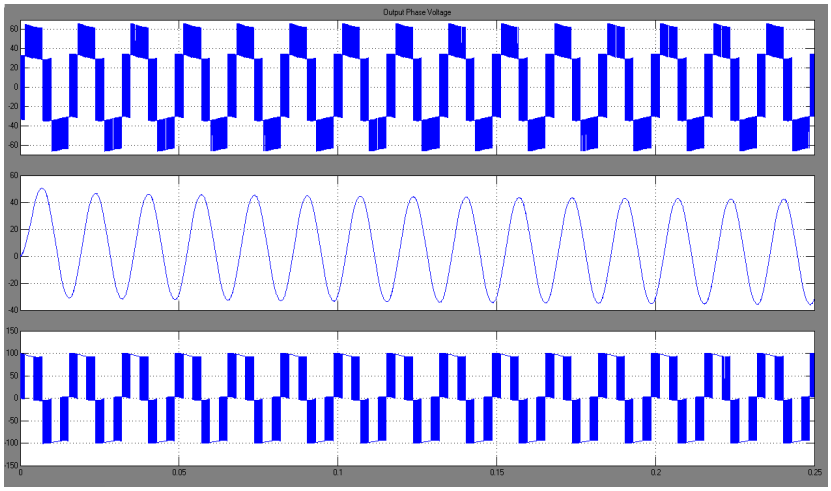

Fig 4.2 Output Phase voltages of 3-level CHB-MLI

B. Case 2: 5-level Cascaded H-bridge Multilevel Inverter

Figure 5.1 shows Matlab/Simulink model of five-level cascade h-bridge inverter based inverter. Subsystem of the inverter controller is shown in Figure 5.2 and 5.3. The modulated signal $V_{control}$ is compared with a phase shifted triangular signals in order to generate the switching signals. The carrier, modulating and command signals using phase shifted SPWM method are produced in this sub-system. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal. Figure 5.4 shows waveforms of output phase voltages for five level H-Bridge inverter.

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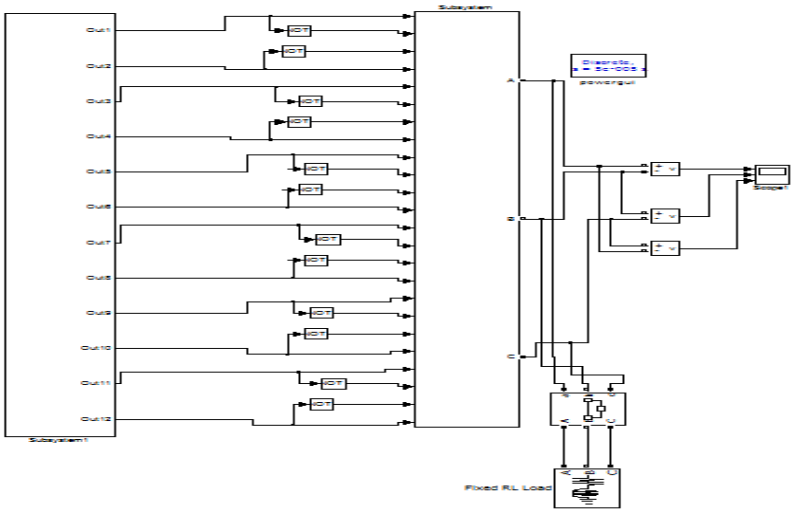

Fig 5.1 Simulink model of Three-phase five-level cascaded H-bridge MLI

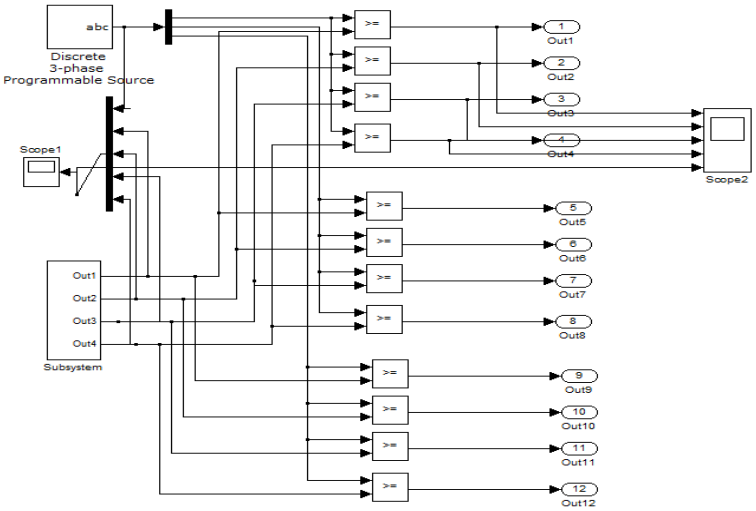

Fig 5.2 Design of modulator block of SPWM controlled 5-level inverter

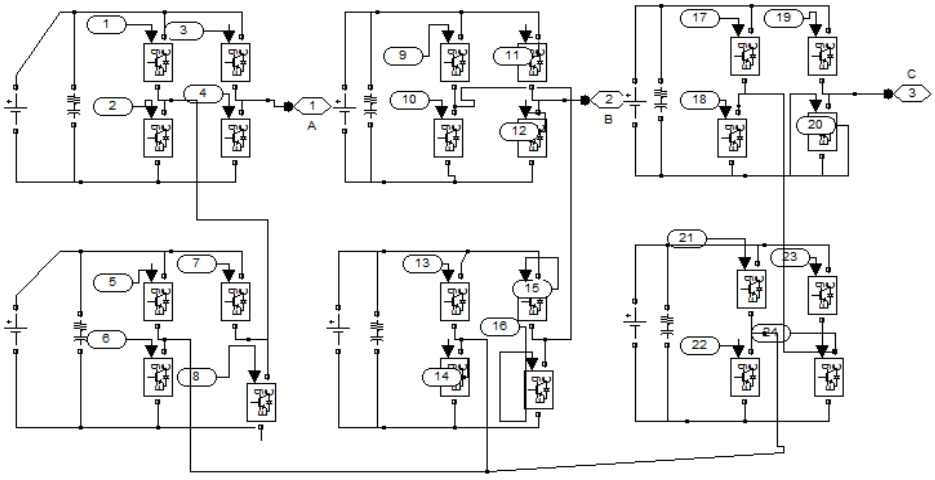

Fig 5.3 Sub system of Three-phase five-level cascaded H-bridge MLI

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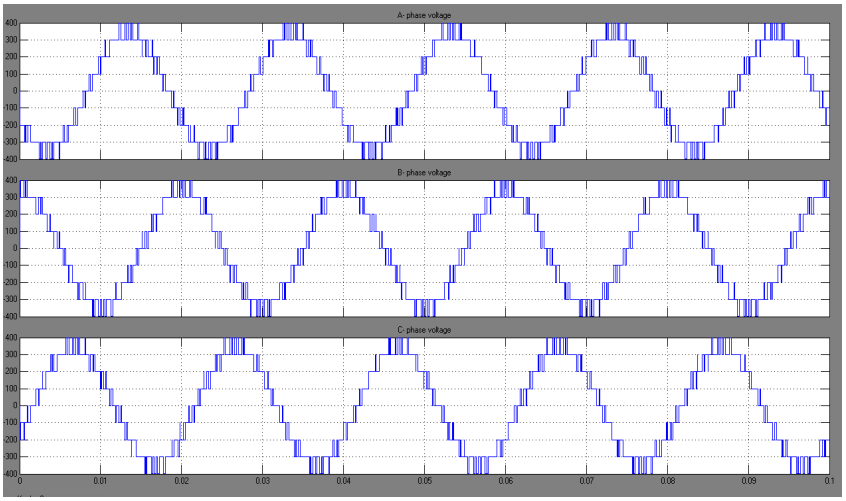

Fig 5.4 Output Phase voltages of 5-level CHB-MLI

C. Case 3: 13-level Cascaded H-bridge Multilevel Inverter

Figure 6.1 shows Matlab/Simulink model of thirteen-level cascade h-bridge inverter based inverter. The modulated signal $V_{control}$ is compared with a phase shifted triangular signals in order to generate the switching signals. The carrier, modulating and command signals using phase shifted SPWM method are produced in this sub-system. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal. Figure 6.2 and 6.3 shows waveforms of output phase- ground and phase to phase voltages for thirteen level H-Bridge inverter.

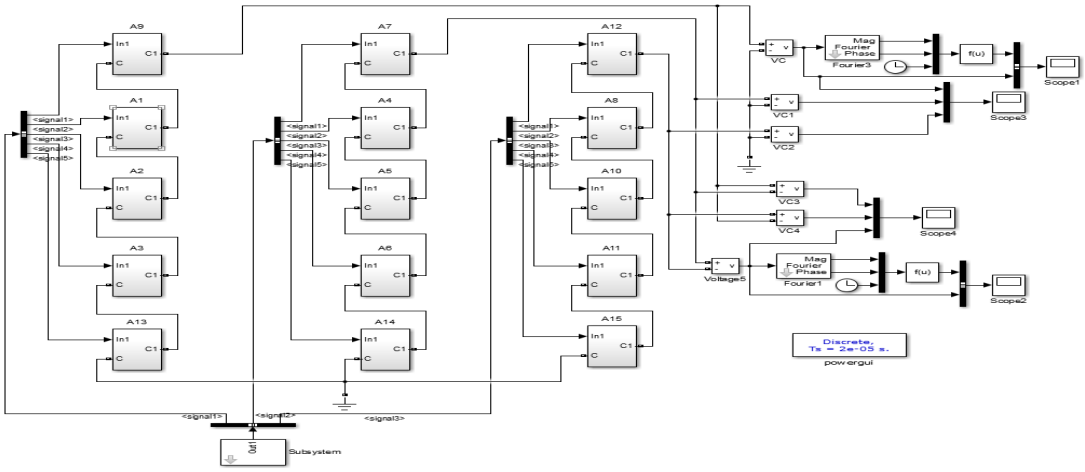

Fig 6.1 Simulink model of thirteen-phase thirteen-level cascaded H-bridge MLI

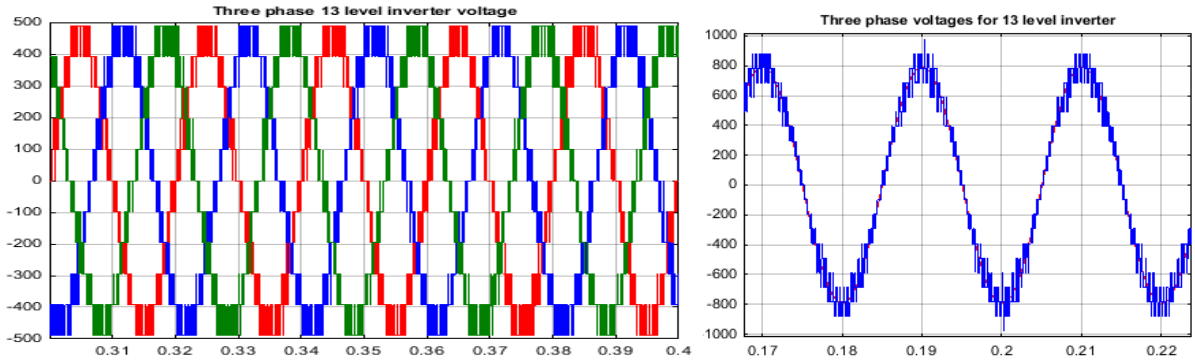

Fig 6.2 Output Phase-ground voltages and Fig 6.3 phase voltages of 13-level CHB-MLI

D. Case 4: 15-level Cascaded H-bridge Multilevel Inverter

In this case, Matlab/Simulink model of fifteen-level cascade h-bridge inverter based inverter is developed. The modulated signal $V_{control}$ is compared with a phase shifted triangular signals in order to generate the switching signals. The carrier, modulating and command signals using phase shifted SPWM method are produced in this sub-system. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal. Figure 7.1 and 7.2 shows waveforms of output phase- ground and phase to phase voltages for fifteen level H-Bridge inverter.

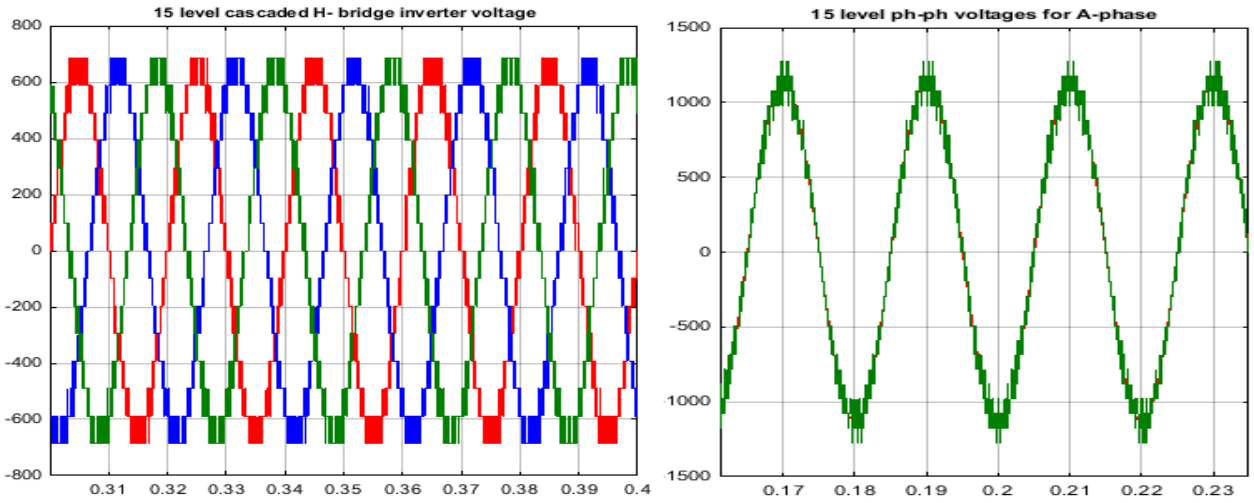

Fig 7.1 Output Phase-ground voltages and Fig 7.2 phase voltages of 15-level CHB-MLI

E. Case 5: 21-level Cascaded H-bridge Multilevel Inverter

In this case, Matlab/Simulink model of twentyone-level cascade h-bridge inverter based inverter is developed. The modulated signal $V_{control}$ is compared with a phase shifted triangular signals in order to generate the switching signals. The carrier, modulating and command signals using phase shifted SPWM method are produced in this sub-system. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal. Figure 8.1 shows waveforms of output phase- ground and phase to phase voltages for twentyone level H-Bridge inverter.

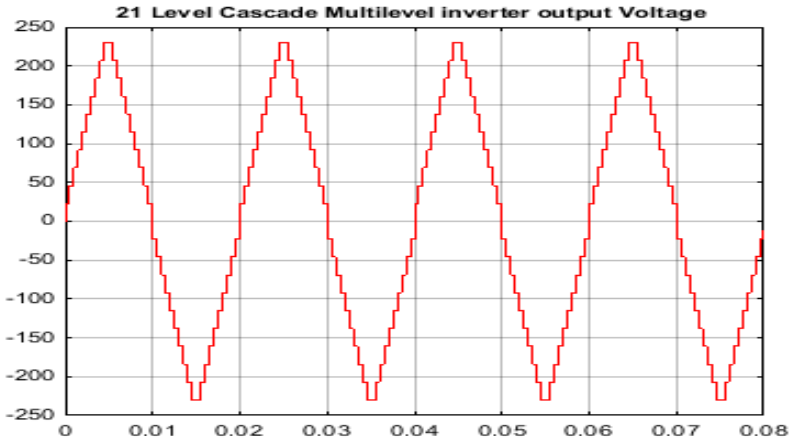

Fig 8.1 phase voltages of 21-level CHB-MLI

F. Case 6: 31-level Cascaded H-bridge Multilevel Inverter

Figure 9.1 shows Matlab/Simulink model of thirtyone-level cascade h-bridge inverter based inverter. The modulated signal $V_{control}$ is compared with a phase shifted triangular signals in order to generate the switching signals. The carrier, modulating and command signals using phase shifted SPWM method are produced in this sub-system. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal. Figure 9.2 and 9.3 shows waveforms of output phase- ground and currents for thirty-one level H-Bridge inverter.

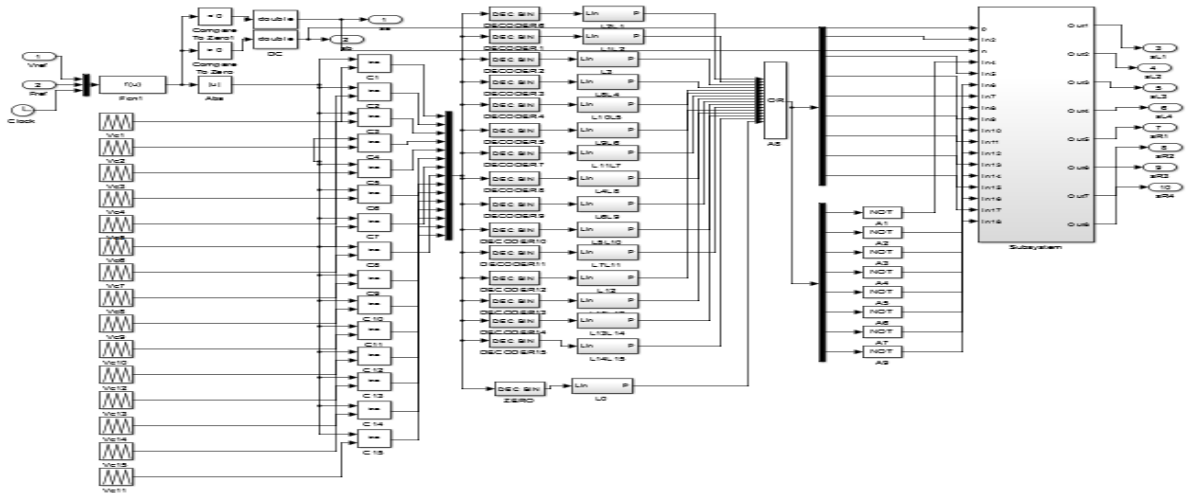

Fig 9.1 Simulink model of three-phase thirty-one level cascaded H-bridge MLI

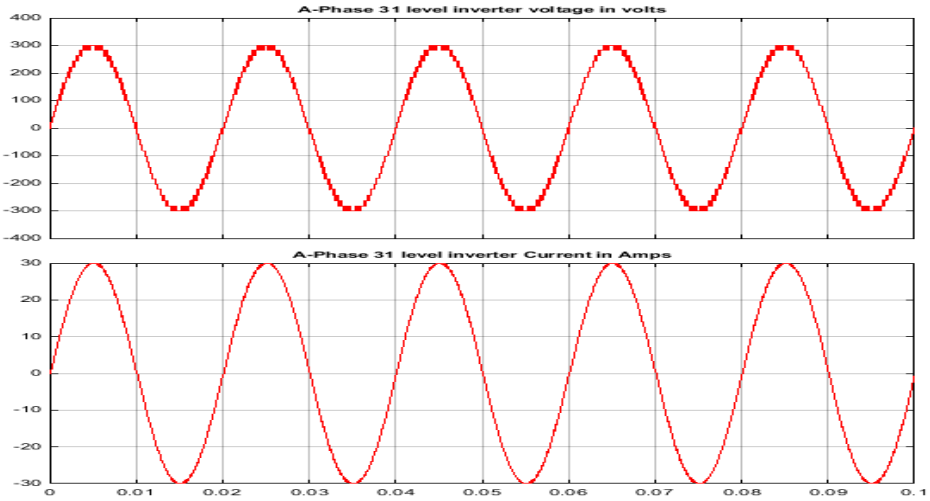

Fig 9.2 Output Phase-ground voltages and current of 31-level CHB-MLI

VI. RESULT AND DISCUSSION

Simulation results for three level in Figure 4.1-4.2, five level from Fig. 5.1 to 5.4, thirteen level in Fig. 6.1 and 6.2, fifteen level in Fig. 7.1 and 7.2, twenty-one level in Fig. 8.1 and thirty-one level inverters in Fig 9.1 and 9.2 are shown in respectively. And the total harmonic distortion for each inverter is shown in Table 2.

Table 2 Voltage Thd Of Three, Five, Thirteen, Fifteen, Twenty-One And Thirty-One Level Inverters

Multilevel Inverter	Three Level Inverter	Five Level Inverter	Thirteen Level Inverter	Fifteen Level Inverter	Twenty-one Level Inverter	Thirty-one Level Inverter
THD for voltage	27%	19.78%	11.29%	7.45%	4.58%	3.5%

VII. CONCLUSION

The simulation of three level, five level, thirteen, fifteen, twenty-one and thirty-one level inverters are realized in MATLAB SIMILINK where for switching of the ideal diode sine pulse width modulation (SPWM) is used for modulation purpose Phase opposition disposition (POD) carrier scheme is used. The total harmonic distortion for each level is calculated and compared. From the different levels of simulation it is clear that THD can be decreased by increasing number of levels.

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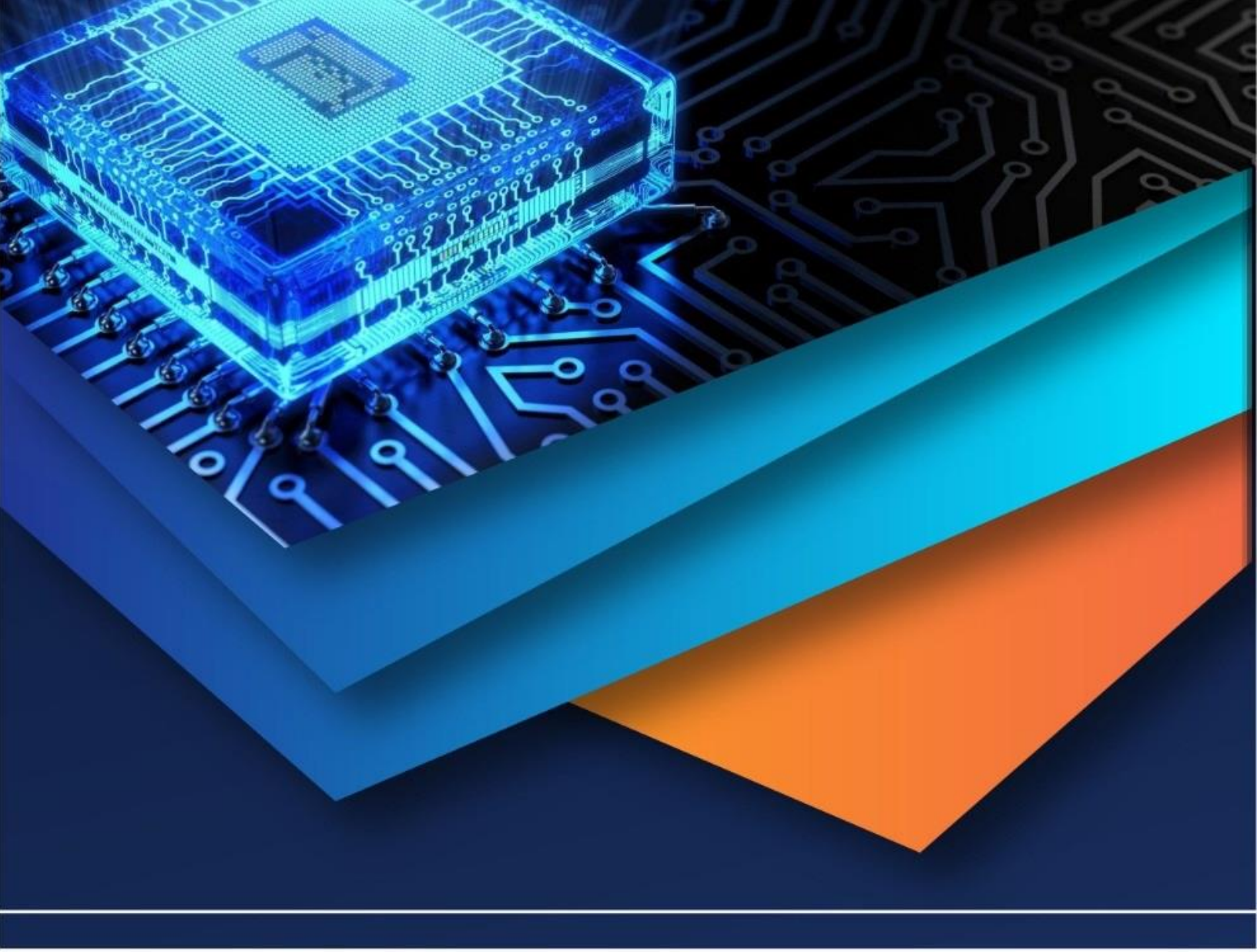

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