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Wideband Low Noise Amplifier Design at L band for Satellite Receiver

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Abstract: In this paper, the aim is to design, simulate and fabricate a wideband low noise amplifier circuit at L band with a high gain and low noise figure. The research process was conducted from the design, simulation and layout using Advance Design System (ADS) software to build the actual circuit. The design of the low noise amplifier uses diagram of two-stage cascade amplifier with different center frequency in order to create a good wideband performance and high gain. The low noise amplifier has been fabricated on a PCB board using pHEMT FET transistor amplifier with following specifications: Maximum overall gain of 33.19 dB, operating frequency from 950MHz to 2150MHz, noise figure is about 1.29 dB, the reverse isolation of -37.42 dB, the LNA using a 5 V supply voltage respectively and total current consumptions of 20 mA. This low noise amplifier is used for Satellite Receiver.

Keyword: Low noise amplifier, L band, noise figure, satellite receiver, ADS.

I. INTRODUCTION

Amplification is one of the most basic and prevalent microwave circuit functions in modern RF and microwave systems. In the first stage of the receiver, there is always Low Noise Amplifier (LNA) and this stage has an important rule in quality factor of the receiver. Because any noise injected by components in a system is amplified by later gain stages along with the signal, it is essential that the signal be amplified early in the receiver chain while adding as little noise as possible. The transistor LNA amplifiers are rugged, low cost, reliable and can easily be integrated in both hybrid and monolithic integrated circuit. Transistor amplifiers can be used in a wide range of applications requiring small size, low noise figure, broad bandwidth and low to medium power capacity. The goal of designer is to compromise many importance characteristics such as gain, Noise Figure (NF), stability, power consumption and complexity. The goal of this is to design an wideband LNA with the lowest noise figure, with wideband and gain as high as possible for the given FET. In order to obtain the demand on the system consisting of the gain, noise figure, bandwidth, we have to deal with the design of two-stage LNA. The first stage will optimize the noise figure, bandwidth and the second stage will increase an overall gain. The transistor amplifier used here to design is spf-2086 which was fabricated in pHEMT GaAs FET technology with low noise figure, high gain and operating frequencies up to 10 GHz.

II. TWO STAGE LNA DESIGN

A. Single Stage Amplifier

Typically, a single-stage transistor amplifier with matching networks at the input and output terminals of the transistor are shown in Fig.1, where a matching network is used both sides of the transistor to transform the input and output impedance Z_0 to the source and load impedance Z_S and Z_L. The most useful gain definition for amplifier design is the transducer power gain, which accounts on both source and load mismatch. Thus from [4], we can define separate effective gain factors for the input (Source) matching network, the transistor itself and the output (Load) matching network as follows:

$$G_S = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \qquad (1)$$

$$G_0 = |S_{21}|^2 \qquad (2)$$

$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad (3)$$

The overall transducer gain is $G_T = G_S.G_0.G_L$. The effective gains from G_S and G_L are due to the impedance matching of the transistor to the impedance Z_0.

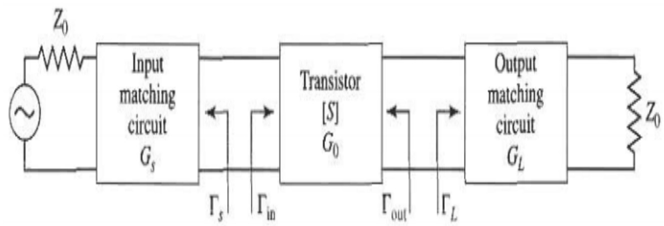

Fig 1: The typical diagram of amplifier circuit.

B. Design of Low Noise Amplifier

The configuration of the LNA in the paper is a two-stage cascade amplifier based on the design of single-stage one. The block diagram of two-stage cascade LNA illustrated in the Fig.2.

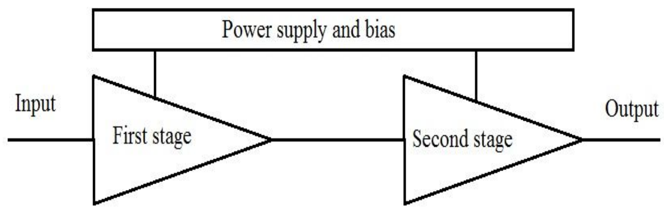

Fig 2: Diagram of two-stages cascade LNA

This two-stage amplifier has the same structure. However, they were provided the different bias voltage. In order to achieve bandwidth 1.2GHz, we suppose the design of center frequency in the first stage at 1.4 GHz and in the second stage at 1.7 GHz.

Design of the low noise amplifier competes with such factors as stability, gain, bandwidth and noise figure. For instance, a minimum noise performance at a maximum gain cannot be obtained. It is therefore, important to optimize characteristics to trade-offs between gain, stability, bandwidth and noise figure.

The first stage was designed to optimize the lowest noise figure. The noise figure of the amplifier at this frequency is calculated to be as follows [4]:

$$F = F_{\min} + \frac{4R_N}{Z_o}\left(\frac{|\Gamma_{opt} - \Gamma_s|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_S|^2)}\right) \quad (4)$$

From the S parameters and noise parameters at 1.4 GHz is provided by Stanford Microdevices we can find the parameters of noise figure as follows: Minimum noise figure F_{min}, Γ_{opt}, the noise resistance $R_N = 50*r_n$. In order to obtain the minimum noise figure, the reflection coefficient Γ_S look into the source is matched to Γ_{opt}. In addition, Γ_{in} is set to be the conjugate of Γ_S, the reflection coefficient looking into the load is shown below:

$$\Gamma_L^* = \frac{S_{22} - \Delta\Gamma_S}{1 - S_{11}\Gamma_S\Delta} \quad (5)$$

In the second stage, we will design for maximum gain. The overall transducer gain is $G_T = G_S.G_0.G_L$. Since G_0 is fixed for a given transistor, the overall gain of the amplifier will be controlled by the gains, G_S and G_L of the matching sections [4].

In order to transfer the maximum power from the input matching networks to the transistor will occur when $\Gamma_S = \Gamma^*_{in}$ and the maximum power transfer from the transistor to the output matching network will occur when $\Gamma_L = \Gamma^*_{out}$.

The value of Γ_S and Γ_L is after that used for the design of the input and output matching networks using smith chart. The matching networks can be designed by some methods such as using lumped components, stubs, quarter-wave transformer or using general transmission line. However, at L band, the design of the LNA using quarter-wave transformer is the best choice.

The completed LNA with two-stage was shown in Fig.3. The power supply for spf-2086 is 5V/20 mA and the voltage of biasing point is obtained at -0.7V.

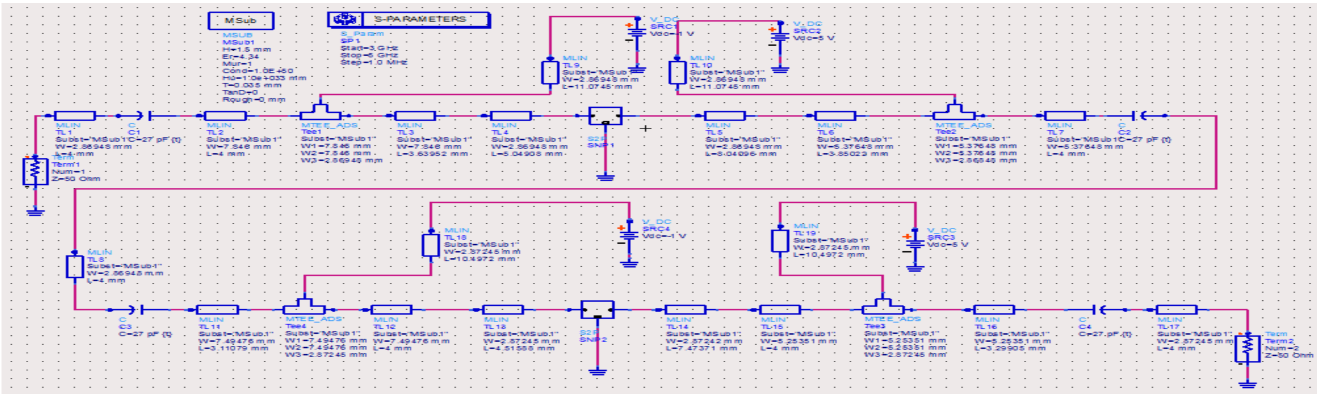

Fig 3: Schematic of the two-stages cascade LNA

III. SIMULATED AND EXPERIMENTAL RESULTS

The LNA circuit was fabricated in Laboratory with the aid of the ADS package and machine LPKF Promomat C40. The circuit was supplied Vds and Vgs through the DC pins at the bottom of the board. The drain current was measured to be about 20 mA. The result was shown in Fig.4.

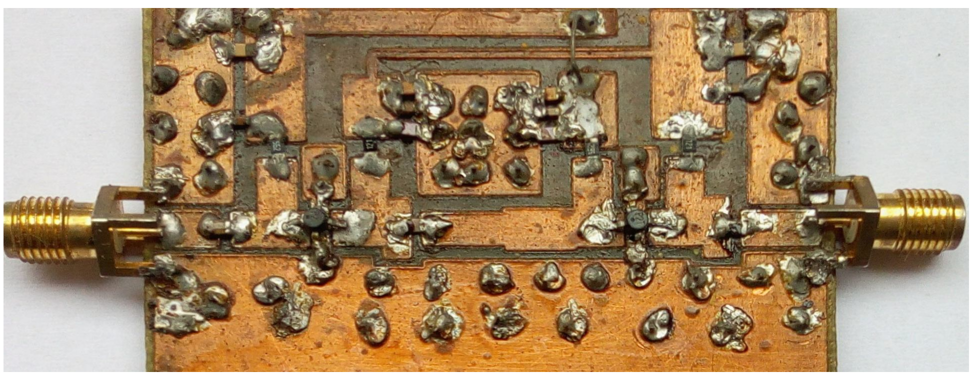

Fig 4: The fabricated LNA

The initial simulations to test the LNA performance were done with the s-parameter file of the transistor. The testing results visually are measured on the vector network analyzer 37369D - Anritsu technology up to 40 GHz and the Signal Analyzer FSQ.
The simulated and experimental results were shown in the bellow Figs.

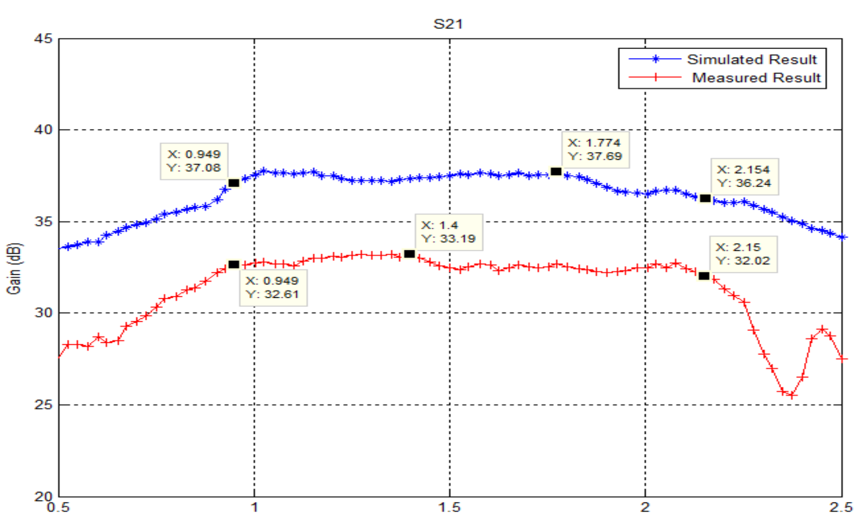

Fig 5: The gain of the LNA (S_{21}).

The simulated result above determines the maximum gain of 37.69 dB at 1.774 GHz while measured result S_{21} reaches at 33.19 dB at 1.4 GHz and circuit amplifies wide band from 0.95GHz to 2.15 GHz with gain is greater than 32.02 dB. The gain observes above is good agreement between the simulated and measured result.

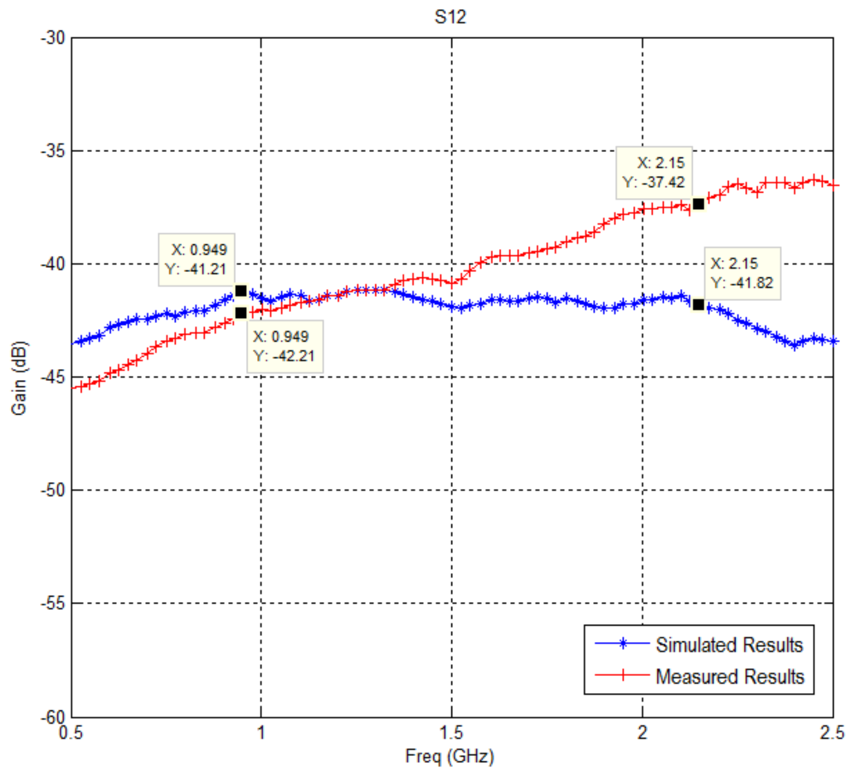

Fig 6: The reverse isolation (S_{12}) of the LNA.

The Fig.6 displays the value of reverse isolation (S_{12}) is very good in working band, and less than -37.42 dB. The measured results of reverse isolation is the same simulated results.

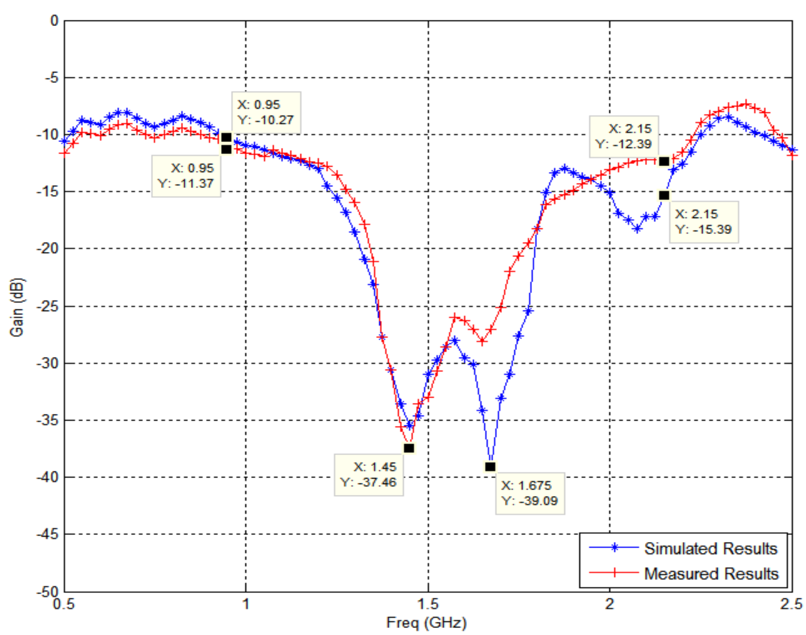

Fig 7: The S_{11} of the LNA

Looking into the results, both simulated and measured results show similar response. Whereas the measured S_{11} resonates at 1.45 GHz, compared to 1.675 GHz of the simulation. The value of the input impedance matching (S_{11}) is good at 0.95GHz to 2.15GHz.

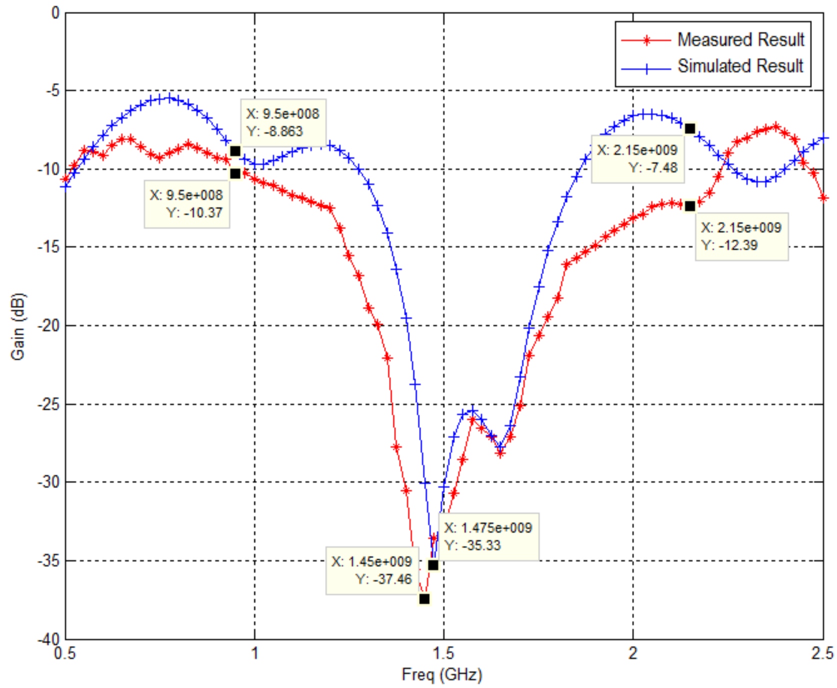

Fig 7: The S22 of the LNA

The measured S_{22} resonates at 1.45 GHz, compared to 1.475 GHz of the simulation. However, the measured results have been observed to be greater than simulation. The S_{22} is less than -10dB in working band. The output impedance matching is quite good and impedance matching range is very wide.

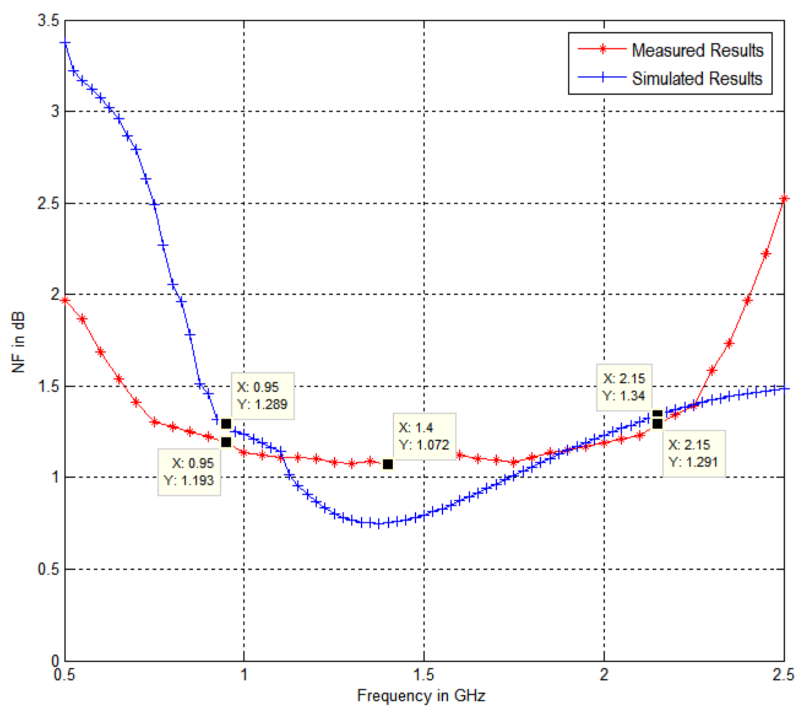

Fig 8: The noise figure of the amplifier

The Fig.8 indicates that the noise figure of the LNA reaches the minimum level 1.07 dB at 1.4 GHz and is less than 1.29 dB over all the designed frequency bands.

IV. CONCLUSION

A two-stage LNA with spf-2086 is designed and demonstrated with simulations in ADS package as well as tuning for the optimum gain, noise figure and bandwidth. The design was fabricated, measured and analyzed together with the simulated results. In summary, the measurement results of wideband low noise amplifier circuit were compared to references with following parameters:

Table 1: comparison between measurement results and references.

Parameters	This work	Ref. [2]	Ref. [3]
Frequency	0.9 - 2.15GHz	136 - 941 MHz	136 - 941 MHz
NF	1. 29 dB	1.02 dB	1.5 dB
S_{21}	32.02 dB	17.5 dB	12 dB
S_{12}	- 37.4 dB	-23 dB	-27 dB
S_{11}	- 12 dB	-10 dB	-35 dB
S_{22}	- 37.66 dB	-10 dB	-48 dB

The benefits of this LNA design are the stability of its performances throughout the wideband frequency range, high gain, low noise and smaller PCB fabrication. Overall, this LNA could be used for the RF front end application working at 0.95 – 2.15GHz.

V. ACKNOWLEDGMENT

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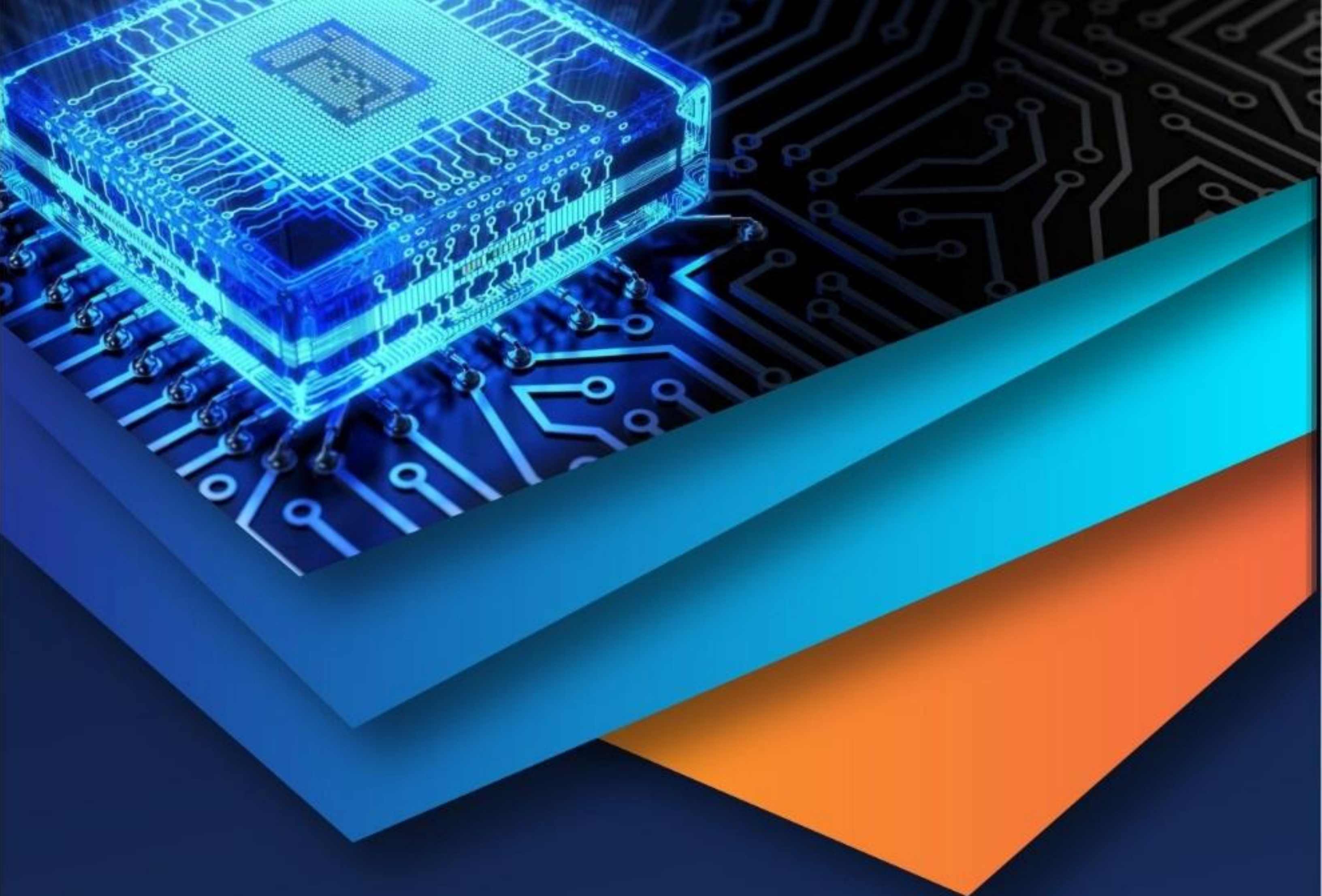

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