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16-Bit Carry Look-Ahead Adder: Design and Layout with Cadence Tools Top of Form

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Abstract: ***The development of highly organised architecture is the primary goal of the current communication world in order to achieve high speed computation with low power consumption. The Carry Look Ahead Adder is highly efficient due to its ability to reduce the propagation time of carry bits, resulting in time savings. The implementation of a 16-Bit Carry Look Ahead Adder using the Cadence tool is carried out in our project. Logical equations for carry generation (G) and carry propagation (P) are used to create the carry and sum for the 1-bit adder. Then, using the Virtuoso schematic editor, a single bit carry is developed. After that, a fresh cell view for the carry block is made and supplied as an input for adder implementations.***
Next, the bit rate is increased to 4 bits. Using this 4 bit adder, 8/16 bit adder is implemented using Cadence tool. It is necessary to have a basic understanding of IC design guidelines and fabrication procedures in order to produce the layout. Within the electronic VLSI design system, the layout will go through a Design Rule Check to find any breaches

I. INTRODUCTION

In advanced digital systems, many adder circuits have delay due to Carry Generation for each bit. It significantly affects how well digital systems operate as a whole [1]. We have chosen Carry Look Ahead Adder from the other adder structures that are available for addition operations, including Carry Select Adders, Carry Increment Adders, Carry Skip Adders, and others. This choice was made due to its potential to decrease the number of gates that a carry signal needs to traverse in order to propagate during the generation and calculation of propagation values, thereby resulting in a reduction in delay. Carry Look Ahead Adders are a convenient technique to quickly add numbers. Thisapproach avoids the need for a bottleneck to form as a result of the carry signal propagating step by step. The majority of embedded System processing modules as well as microprocessor systems have made extensive use of the Arithmetic Logic Unit [3]. Allprocessors with adders generally need to operate at a high speed. Consequently, increasing the speedof the carry chain is necessary to increase the speedof the adders [3]. Due to our lesser power requirements, we choose to utilize the carry look ahead adder.. When adding becomes faster in an arithmetic operation, all other arithmetic operations also get faster. In the majority of situations, we favour carrylook ahead adders since they minimise the carry propagation latency and provide excellent performance. The Carry Look Ahead Adder is a technique that can be employed to expedite the carry computations. Carry Look Ahead Adders are the quickest method for adding two binary values in order to minimise computation time.

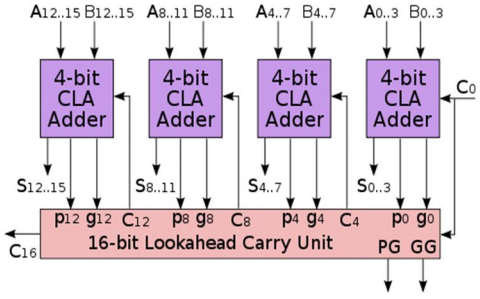

Fig1-16-Bit Carry Look-Ahead Adder Architecture

To facilitate the more straightforward integration, verification, and implementation of complicated circuits. The Cadence Virtuoso Platform is an instrument for creating fully customized integrated circuits, encompassing schematic input, extraction, and back-marginal notation. Cadence's simulator- independent environment lowered the learning curve. Advanced full custom polygon editing (L)is now available. The most extensive selection of process design kits (PDKs) for process nodes worldwide, supplied by top foundries worldwide, counterbalances the virtuoso platform. Circuits from basic 7nm process nodes to 0.6µm can be stimulated by it.

Integrated circuits are built using a variety of technologies, such as NMOS, PMOS, bipolar, and CMOS. The preference for CMOS technology stems from its lower power consumption, as power is solely utilized during the switching of NMOS and PMOS transistors from on to off states.

II. PROPOSED METHOD

In digital electronics, addition is a fundamental process. However, the carry signal propagates slowly through several digital components. Utilizing the Carry Look Ahead Adder can significantly decrease the propagation time of the carry bit.

Following that, we have analyzed the fundamental structure of the Carry Look Ahead Adder (CLA). The CLA relies on two primary signals, namely the Propagate Signal (P) and the Generate Signal (G).

Truth table

Mi	Ni	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

If Mi, Ni, and Cin have high values, the resulting sum will be high and a carry will be generated as well. Equation (1) shows the formula for the carry propagate signal Pi, and equation (2) expresses the generate signal Gi. The sum is shown in equation (3), and the execution of Ci+1 is indicated in equation (4).

$\boldsymbol{Pi} = M\boldsymbol{i} \oplus N\boldsymbol{i}$ (1)

$\boldsymbol{Gi} = M\boldsymbol{i} \,.N\boldsymbol{i}$ (2)

The output sum and carry can be expressed as-

$\boldsymbol{Si} = \boldsymbol{Pi} \oplus \boldsymbol{Ci}$ (3)

$\boldsymbol{Ci}+\mathbf{1} = \boldsymbol{Gi} + (\boldsymbol{Pi}.\boldsymbol{Ci})$ (4)

Where i = 0,1,2…..n-1.

For 4 bit CLA-

Using the provided equation, we have the ability to construct the circuit design. Subsequently, we can proceed to formulate the Boolean function for the carry output of every stage (in this scenario, there are four stages) and substitute it with a distinct value for each Ci..

The equations for the output carry of a 4-bit Carry Look-Ahead (CLA) can be applied using the previously mentioned formulas. The given output carry equations are provided below.

C1 = G0 + P0C0

C2 = G1 + P1C1 = G1 + P1(G0 + P0C0) = G1 + P1G0 + P1P0C0

C3 = G2 + P2C2 = G2 + P2G1 + P2P1G0 + P2P1P0C0

C4 = G3 + P3C3 = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1 P0C0.

The equations for propagating, generating, summing, and carrying signals will be repeated for a given number of bits, such as 8, 16, 32, and so on.

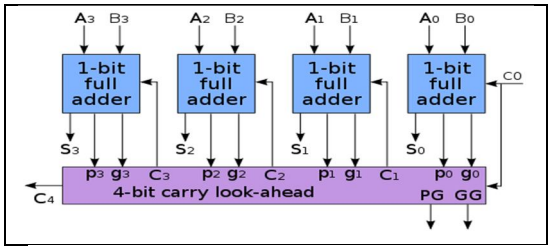

Fig 2- 4-Bit Carry Look-Ahead Adder Utilizing Full Adder Units

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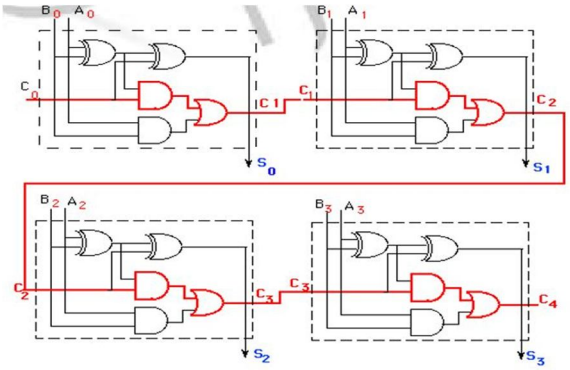

Fig 3-4-Bit Carry Look-Ahead Adder Constructed from Logic Gates

The CLA adder utilizing a 1-bit full adder is depicted in Figure 2 [5]. The full adder produces the carry propagate, carry generate, and the sum of the corresponding bits. These carry propagate and carry generate bits are then fed into the carry look ahead adder, and the final carry is generated by the CLA generator. Figure 3 illustrates the carry look ahead adder, which employs logic gates like the Exclusive OR gate, AND gate, and OR gate.

III. INTEGRATED CIRCUIT DEVELOPMENT

Transistors, wires, and bias are the three basic parts used to build integrated circuit layouts. Layout design is subject to design rules, which specify how different components should be arranged and interact with one another. In order to incorporate several functions onto a single chip, IC designers strive to reduce component sizes as much as feasible. Errors can occur throughout the fabrication process since wires and transistors are small components. Design guidelines are therefore created to reduce these mistakes. Creating design guidelines helps to raise to a suitable level the yield of precisely manufactured chips. Hence, it is crucial to take into account the design rule when designing the layout. The project's verification process will include DRC, LVS and ERC. These procedures play a significant role in IC layout and should not be underestimated.

A. Design Rule Check (DRC)

The chip's physical layout is examined to see if it conforms to the specified design rules using the Design Rule Check (DRC) verification technique. It confirms that all layers follow production guidelines, such as those regarding width and spacing. Following layout preparation, DRC is the first stage of verification. It assesses the design in the context of its intended application in addition to looking at design guidelines. Design dependability is improved with DRC by lowering the possibility of design flaws. As such, while potentially incomplete, it provides instantaneous analysis.

B. Layout Vs Schematic (LVS)

The process of Layout versus Schematic (LVS) is utilized to verify if an IC layout accurately matches the original schematic circuit of the design. All signals—inputs, outputs, and power signals—have their electrical connections examined during this procedure to make sure they match the corresponding devices accurately. As part of the LVS process, the dimensions of the devices are thoroughly examined. This includes verifying the width and length of the transistors, as well as assessing the sizes of the resistors and capacitors. Additionally, LVS identifies any additional components and indicators that may not have been depicted in the diagram. Initially, NCC uses a technique called local partitioning to find circuit incompatibilities. Next, NCC applies a second-generation layout validation tool called the Gemini algorithm.

C. Electric Rule Check (ERC)

When examining device connections or connectivity issues, ERC (Electrical Rule Check) is frequently used. It acts as an extra level of optional verification. ERC is used to identify any redundant, partially connected, or disconnected devices. It also checks for short circuits, floating nodes, and deactivated transistors.

The table above illustrates the basic principle of IC design, with all measurements given in lambda. It outlines the design guidelines for diffusion, poly, metal 1, metal 2, cut, and via. The alignment rule for cut or via surrounding and poly space to diffusion is 1λ, while for poly overlapping diffusion it is 2λ.

LAYER	WIDTH	SPACE
POLY	2	3
DIFF	3	3
METAL 1	3	3
METAL 2	3	4
N WELL	12	6
CUT	2	2
VIA	2	3

IV. LAYOUT DESIGNING

Physical Design of the CLA in the VLSI systemhas been done utilizing a variety of technologies. The author of this paper

1) Has provided a technique for creating an IClayout with 90nm technology. Where in the fully bespoke and semi-custom methods were both applied. Comparing the variations in area efficiency and power dissipation between semi-custom and full-custom techniques was the key to evaluating CLA performance. The outcome demonstrates that, in contrast to the fully custom way, the semi-custom method results in a small area and slow power consumption.

2) Using cadence GPDK and 90nm technology, the circuit was analyzed. The transient analysis is used to interpret the circuit's power consumption values. The results show that using the short pulse successfully turned on the logic block for the required short amount of time, which minimized wasteful use. Constant Delay (CD) logic was employed in this paper

3) To lower the power delay product and dissipation. H-Spice was used for the simulation, while Cosmo Scope Z 2007.03 was used to check the latency. Better PDP is produced by the CD logic, which focuses mostly on critical path delay improvement.

4) The efficiency of CLA was evaluated by comparing the propagation delay, power dissipation, and the resulting product. The Tanner EDA tool was used to simulate the circuit while taking into account various feature sizes (150, 200, and 250 nm). The 8-bit pseudo-NMOS CLA implementation required the most average power, according to the paper's data, whereas the 4-bit normal CMOS CLA implementation required the least average power. Using Xilinx as a synthesis tool, this paper

5) This research, utilizing Xilinx as the synthesis software, concentrates on the utilization of Verilog code for the design and simulation of 4/8/16 bit CLA circuits. The findings indicate that the adder with carry look-ahead exhibits the most favorable area-delay product.

6) Power dissipation and PDP results were compared to determine the performance. Tanner environment with 90nm and 180nm technology was used for simulation. Moreover, carry skip adderhas the least PDP. The alternative log-n stage design that the author provides in this study achieves almost ideal performance in terms of maximum connector wire length, area-time efficiency, and regularity.

7) The CLA's structure becomes noticeably regular when input and output are limited, making it easier to add two n-bit values in a time of zero.

V. METHODOLOGY

We will work using program called Electric Cad. And make use of its potent tools. And willemploy wave viewer and schematic recording using LT Spice IV simulation software. The gates in CLA are AND, XOR, and OR. We can construct, carry, generate, and propagate signals using gates. The propagate and create signal schematic diagram is displayed in Fig. 4.It will be used during the entire CLA process. Itcan be 4, 8, 16, 32, or many other bits. Figure 5 displays the Circuit Diagram of a 1-bit partial full adder, while Figure 7 showcases the Circuit Diagram layout of a 4-bit CLA. We will Perform a DRC check at each level of layoutdesign in order to find any errors.

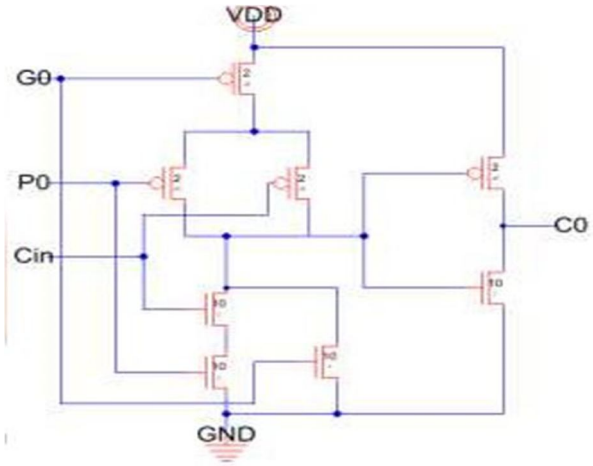

Fig-4 Circuit Diagram Representation of Carry Propagation and Generation Signals"

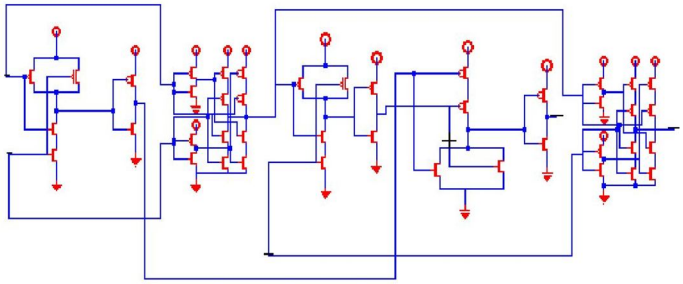

Fig -5 Diagram: Full Adder Circuit.

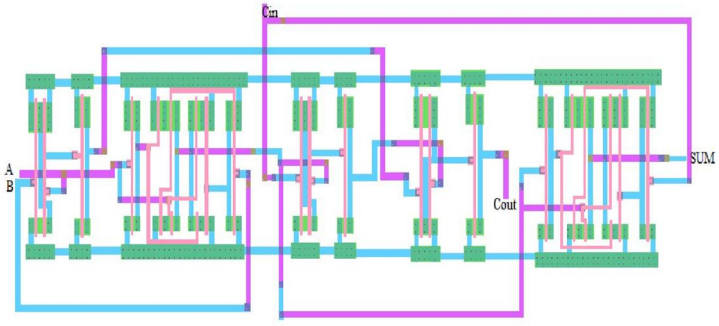

Fig-6 "Full Adder Layout Design"

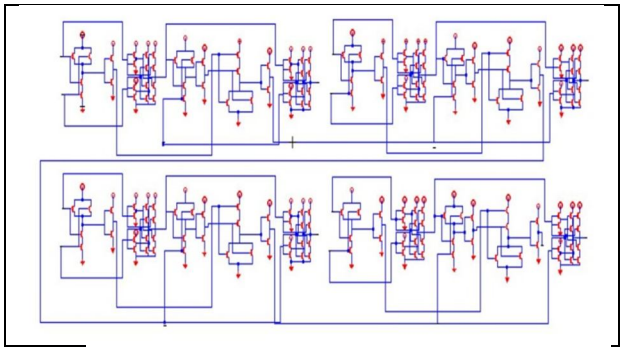

Fig-7- Diagram: 4-Bit Carry Look-Ahead Adder Circuit

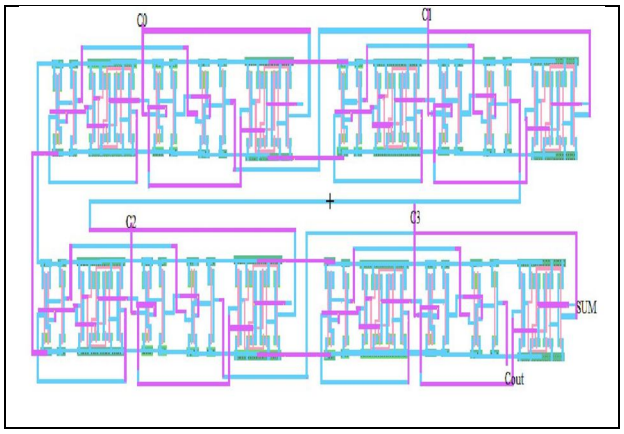

Fig-8- 4-Bit Carry Look-Ahead Adder: Layout Design

VI. CONCLUSION

After receiving the output from the layout design, we will examine the CLA's transient andfrequency response using the results of the simulation. Additionally, a user-friendly tool for designing complex circuit architectures is provided via the open-source Electric VLSI platform. With the use of this program, we may also be able to handle more complicated circuits and use the IRSIM simulator to determine their transient response. Reduction in delay, power consumption, and memory usage has been achieved. Carry look ahead adders play a crucial role in reducing the carry propagation time of the adder in comparison to different logic designs.
Now using the 4 bit CLA schematic we have to design 8/16 bit CLA and then design the layout of that 8/16 bit CLA.

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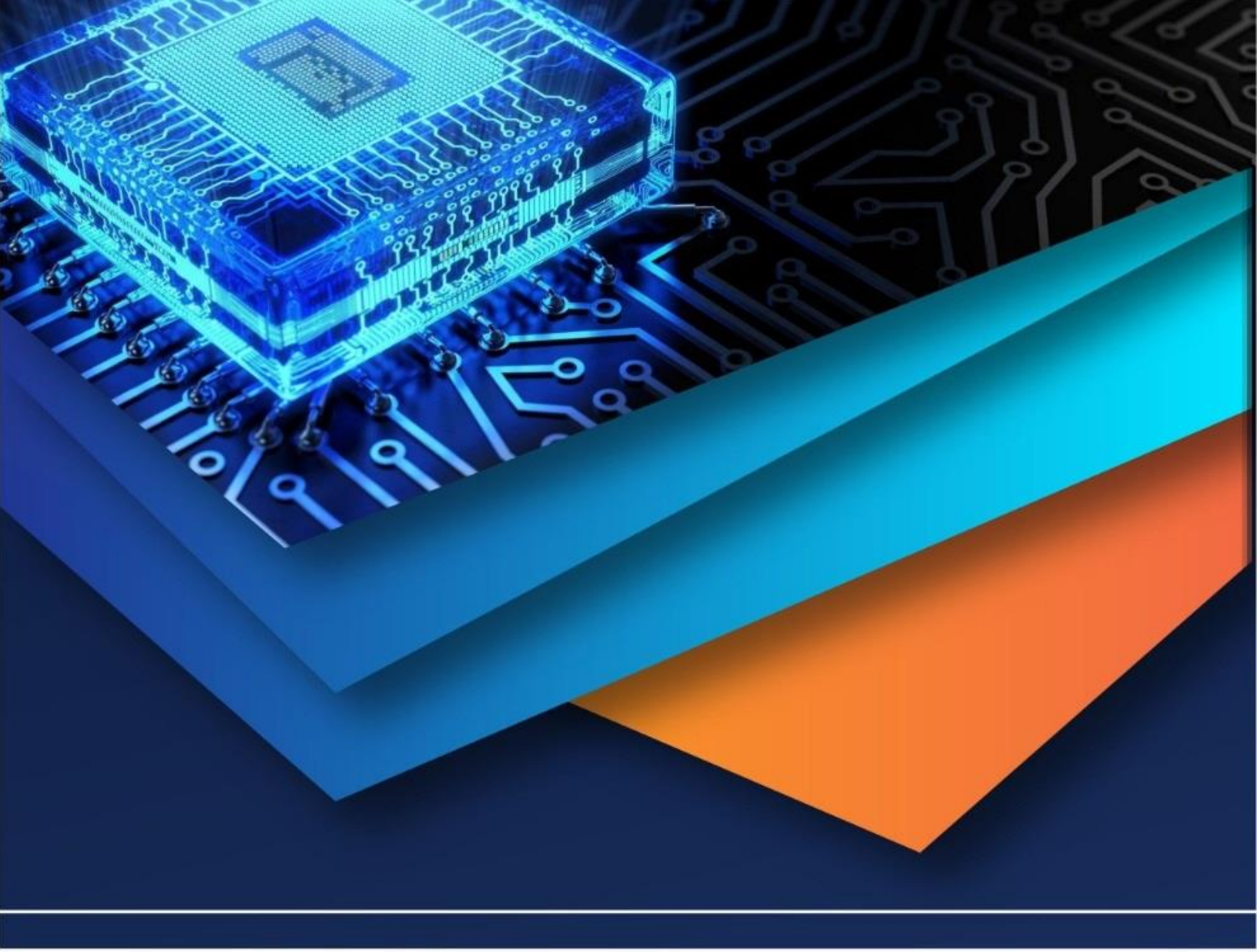

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