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Design and Implementation of 32 Bit Linear Feedback Shift Register using FPGA

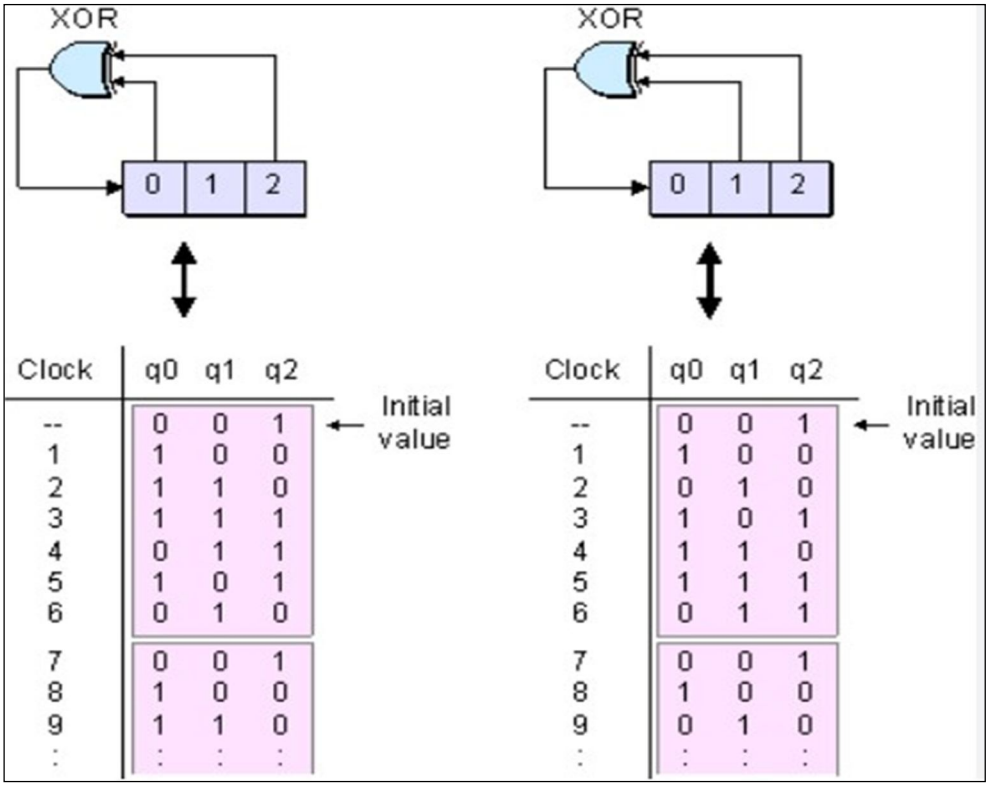
Sajal Tripathi[1], Sharad Gupta[2], Shivanshu Pratap Singh[3], Kamal Bhatia[4]
Department of Electronics & Communication Engineering ABES Engineering College Ghaziabad, India

Abstract: ***Shift register is a common device for generating signals and sequences. Usually register is the combination of flipflops.The shift register is of two types which are: linear and nonlinear. Various sequences including pseudorandom codes are generated by linear and nonlinear feedback shift registers, respectively. Linear feedback shift register (LFSR) is composed of dynamic or static master-slave flip-flop. Its characteristics are usually characterized by a characteristic polynomial. The two-input XOR gate is used to calculate the characteristic polynomial of the maximum or near maximum length of the feedback function without rectifying the register.***

Keywords: LFSR, Flipflop, XOR gate, seed, linear and non linear Shift Register.

I. INTRODUCTION

The initial value assigned to the register is called the "seed", because the operation of the linear feedback shift register is deterministic, so the data stream generated by the register is completely determined by the state of the register at that time or before. Moreover, because the state of the register is limited, it will eventually be a repeated cycle. However, with primitive polynomials, linear feedback shift registers can generate sequences that appear random and have very long cycle periods. The shift register has a simple structure and a fast running speed. The theory of shift registers has also become the basis of modern stream cipher systems. A sequential shift register with combinational feedback circuitry surrounding it, the linear feedback shift register pseudo-randomly cycles through a series of binary values. A selection of points in the register chain provides feedback on the shift register of the LFSR, and these points are either XORed or XNORed to provide a point back into the register. In essence, the LFSR repeatedly cycles through pseudorandom value sequences.



II. IMPLEMENTATION OF LFSR ON FPGA TECHNIQUE

1) LFSR ON FPGA IMPLEMENTATION USING XILINX:

: Although LFSRs are easily constructed and have many applications, designers regrettably frequently overlook them. A basic shift register is used to create one of the more popular types of LFSR. We use XILINX spartan 3e FPGA board (xc3s500e)

The initial values of the two LFSRs are the same, but when clock pulses are supplied, their sequences quickly diverge because of the differing taps. An LFSR may occasionally wind up cycling in a loop with a finite set of values. Nonetheless, because they cycle through every possible value (except from all bits being 0) before going back to their starting values, the two LFSRs seen in Fig. 2 are considered to be of maximal length.

A maximal-length LFSR with "n" register bits will only sequence through (2^n – 1) values, but a binary field with "n" bits can assume 2^n unique values. This is due to the fact that LFSRs with XOR feedback routes will not run through a value in which every bit is zero.

2) 32 BIT LFSR IMPLEMENTATION USING XILINX ISE 14.7 SOFTWARE

Firstly we implemented 8 bit LFSR and simulate it. After getting the simulation results successfully we also determine its IO planning design, chip floor planning design using PLAN AHEAD 14.7 software which is inbuilt feature of XILINX ISE 14.7

Similarly, we implement 16 bit LFSR using VHDL/Verilog and find its all important parameters.

But our main task is to implement and simulate 32 bit LFSR. For this purpose we use VHDL programming with some modifications. Here we are going to show some important parameters and design considerations.

Below are the some important features which we have determine like : simulation, RTL schematic, technological schematic, chip floor planning, IO planning

Although we know that linear feedback shift register(LFSR) is bound to produce psuedo random numbers when the taps are arranged in some specific form.

III. FEATURES OF THE IMPLEMENTATION

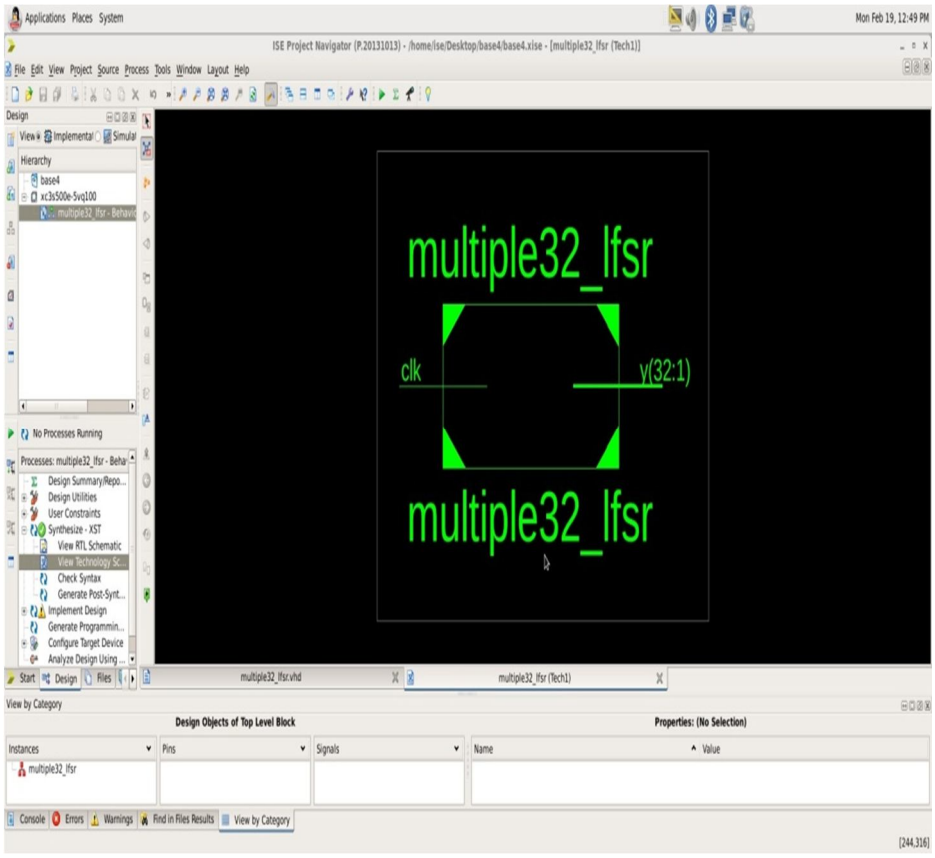


Fig 3. RTL schematic 1 of 32 bit LFSR

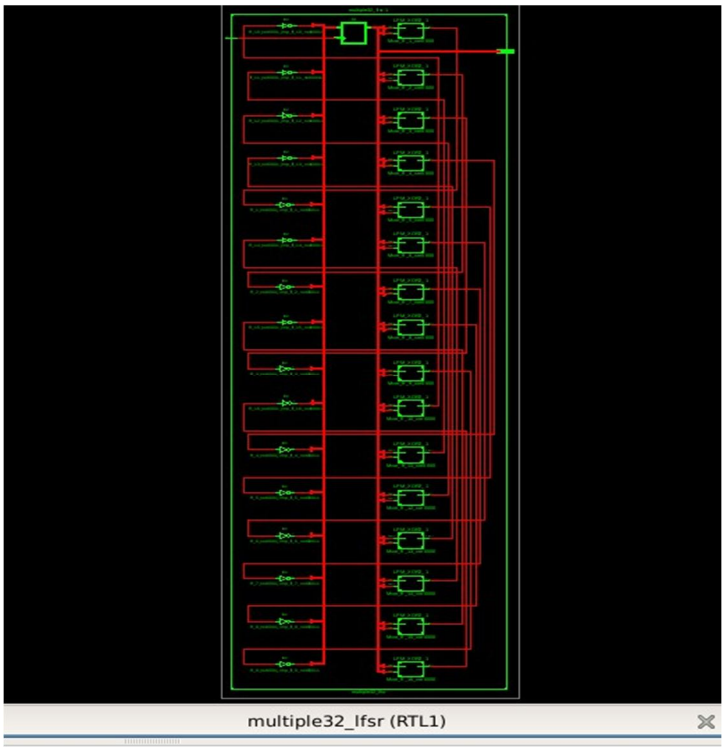


Fig 4. RTL schematic 2 of LFSR using XILINX ISE 14.7

A Linear Feedback Shift Register (LFSR) is a digital circuit that generates pseudo-random sequences using linear feedback
This RTL schematic represents the basic structure of a 32-bit LFSR. The specific connections and feedback polynomial used would determine the sequence generated by the LFSR.

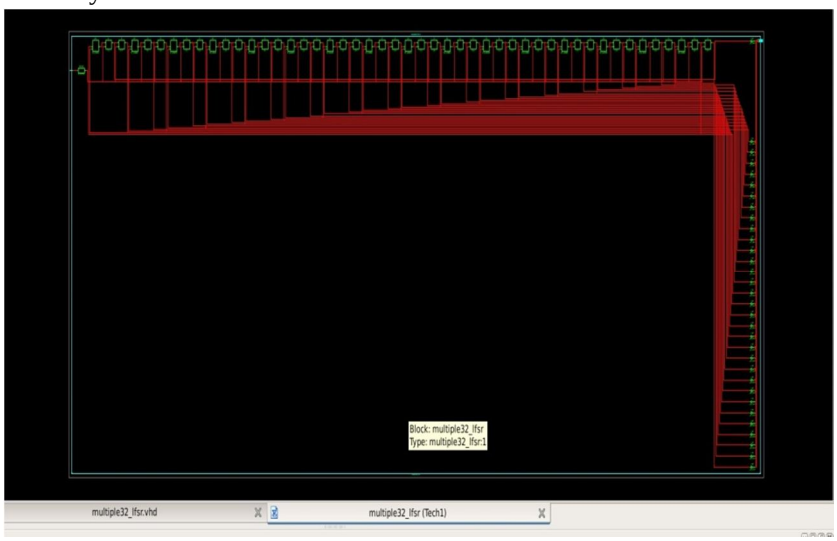


Fig 5. technological schematic using XILINX ISE 14.7

Creating a technological schematic for a 32-bit Linear Feedback Shift Register (LFSR) using Xilinx ISE 14.7 involves designing the circuit using schematic entry tools provided by ISE.
Through this schematic entry process, designers define the interconnections and functionality of the LFSR circuit, including input and output pins, feedback mechanisms, clocking schemes, and reset logic. The schematic serves as a graphical representation of the desired behavior of the LFSR, facilitating design exploration, documentation, and collaboration among team members.

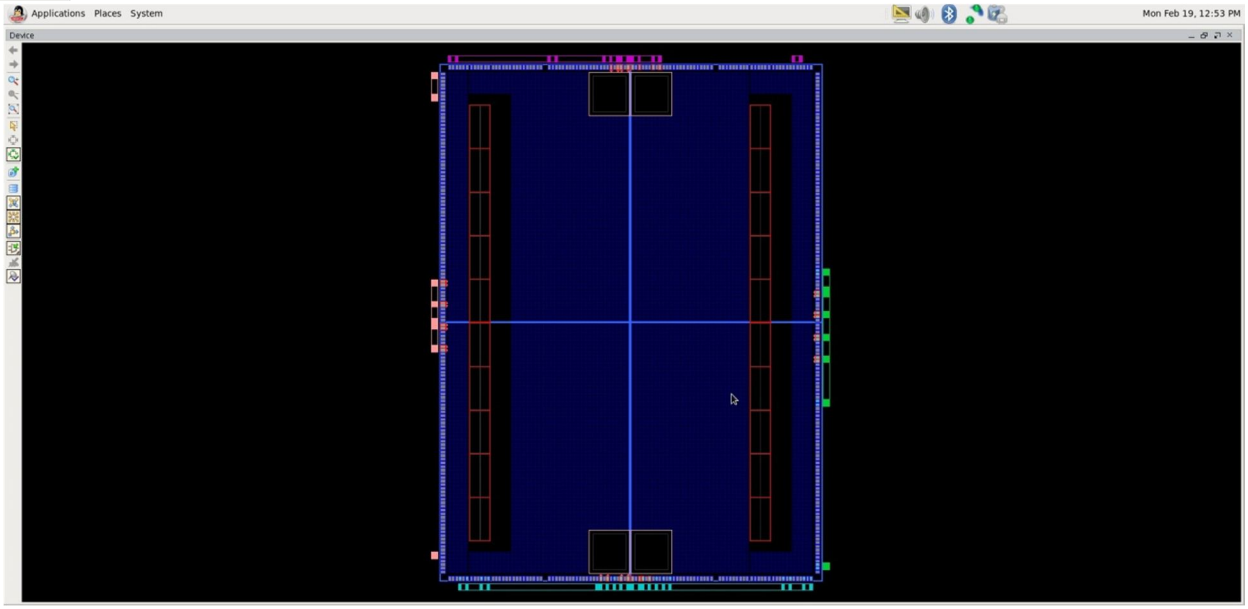


Fig 5. Device planning design of 32 bit LFSR(chip design using Plan Ahead 14.7)

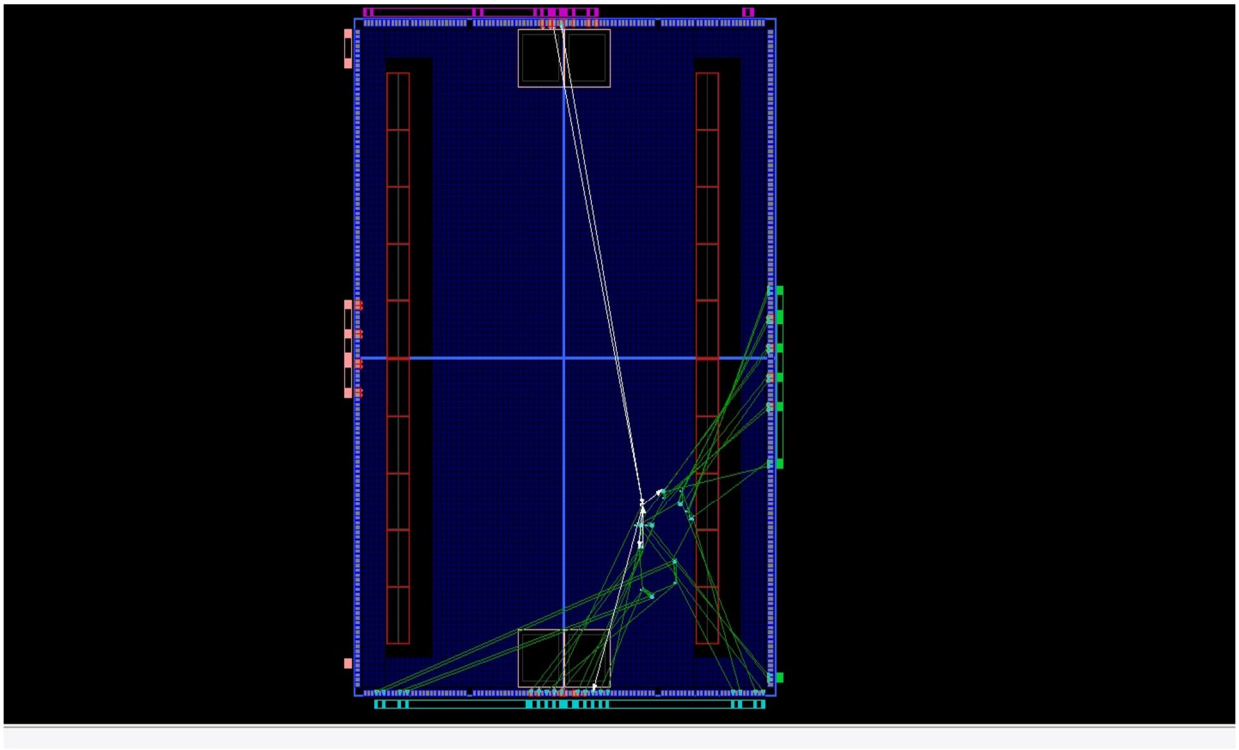


Fig 6. floor planning design of 32 bit LFSR using Plan Ahead 14.7

Floor planning a 32-bit Linear Feedback Shift Register (LFSR) using PlanAhead 14.7 involves organizing the logic elements and routing resources efficiently within the FPGA device.

In conclusion, floor planning a 32-bit Linear Feedback Shift Register (LFSR) using PlanAhead 14.7 is a crucial step in FPGA design. It involves organizing the logic elements and routing resources efficiently within the FPGA device to optimize performance and resource utilization. By carefully partitioning the FPGA device, placing logic elements strategically, and routing connections effectively, designers can ensure that the LFSR operates reliably and meets timing requirements.

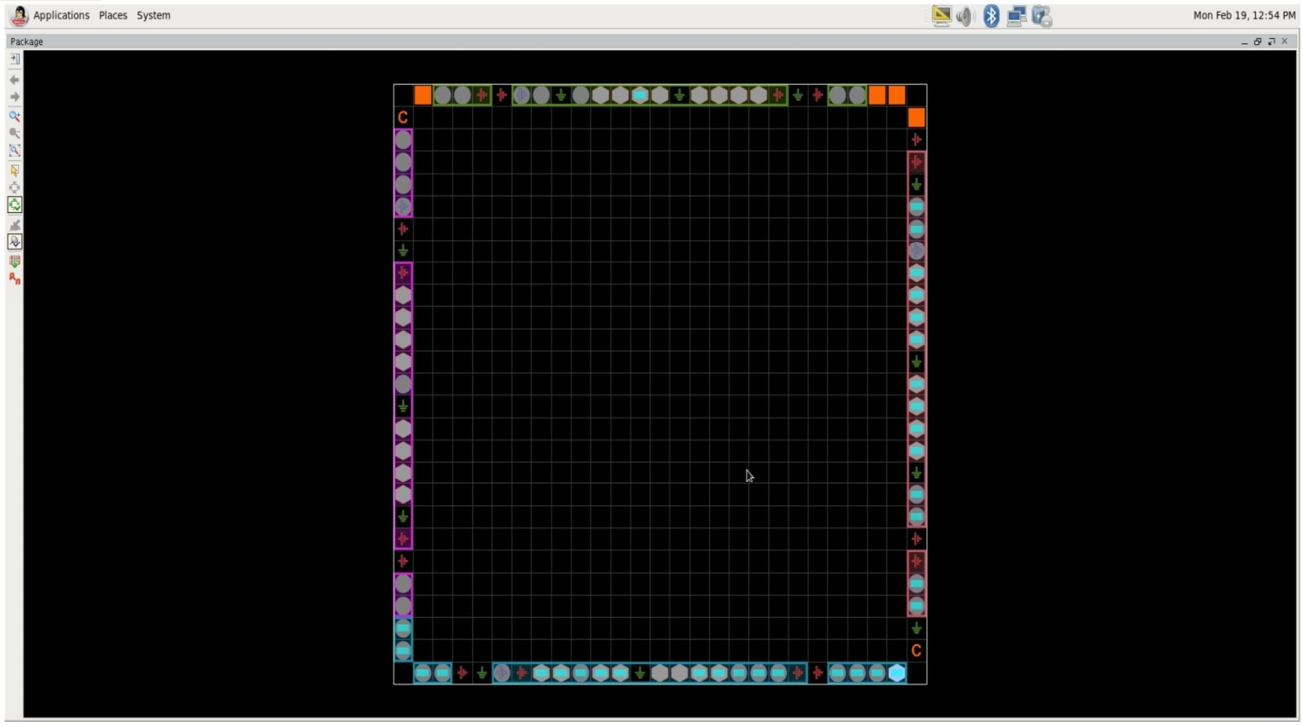


Fig 7. IO planning of 32 bit LFSR using XILINX Plan Ahead 14.7

IO (Input/Output) planning for a 32-bit Linear Feedback Shift Register (LFSR) using Xilinx PlanAhead 14.7 involves defining the physical connections between the FPGA device and external components.

In conclusion, IO planning for a 32-bit Linear Feedback Shift Register (LFSR) using Xilinx PlanAhead 14.7 is a critical aspect of FPGA design. It revolves around defining the physical connections between the FPGA device and external components, ensuring reliable communication and proper functionality of the LFSR within the larger system.

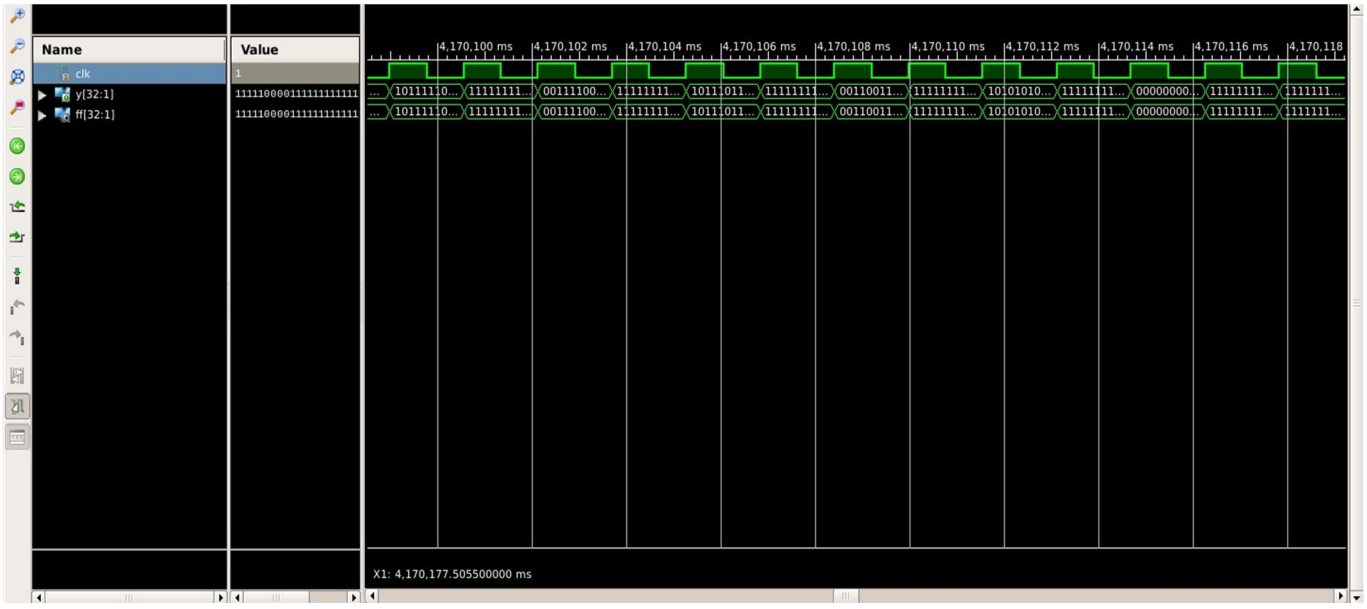


Fig 8. Simulation of 32 bit LFSR on XILINX ISE 14.7

To simulate a 32-bit Linear Feedback Shift Register (LFSR) using Xilinx ISE 14.7, you can use VHDL to describe the behavior of the LFSR and then use the ISim simulator included with Xilinx ISE for functional verification.

IV. CONCLUSION

As we bring our exploration of LFSR to a close, the integration of schematic diagrams, implemented using XILINX ISE 14.7 software, adds a tangible dimension to our comprehensive review. Beyond theoretical discussions, the graphical representations of the respective LFSR

1) *Visualizing Complexity:* The schematic diagrams, meticulously crafted using XILINX ISE 14.7 allow us to visualise the intricate details of each LFSR implementation. They go beyond the abstractions of theory, offering a tangible representation of the electronical and knowledge of shift registers configurations, its types and arrangements, and wave diagrams that define the functionality of these shift registers. Such visualisations are invaluable for engineers and researchers seeking to grasp the complexities of circuitry in a more advanced manner.
2) *A Dynamic Framework for Future Work:* The utilisation of XILINX capture in our study serves not only as a means of representation but also as a dynamic framework for future work. The adaptability of XILINX make it conducive to further experimentation and refinement of LFSR design.
3) *Collaborative Potential:* In the spirit of collaboration, the integration of XILINX ISE 14.7 generated schematic diagrams opens avenues for shared exploration. Engineers and researchers across the globe can leverage the provided visualisations,

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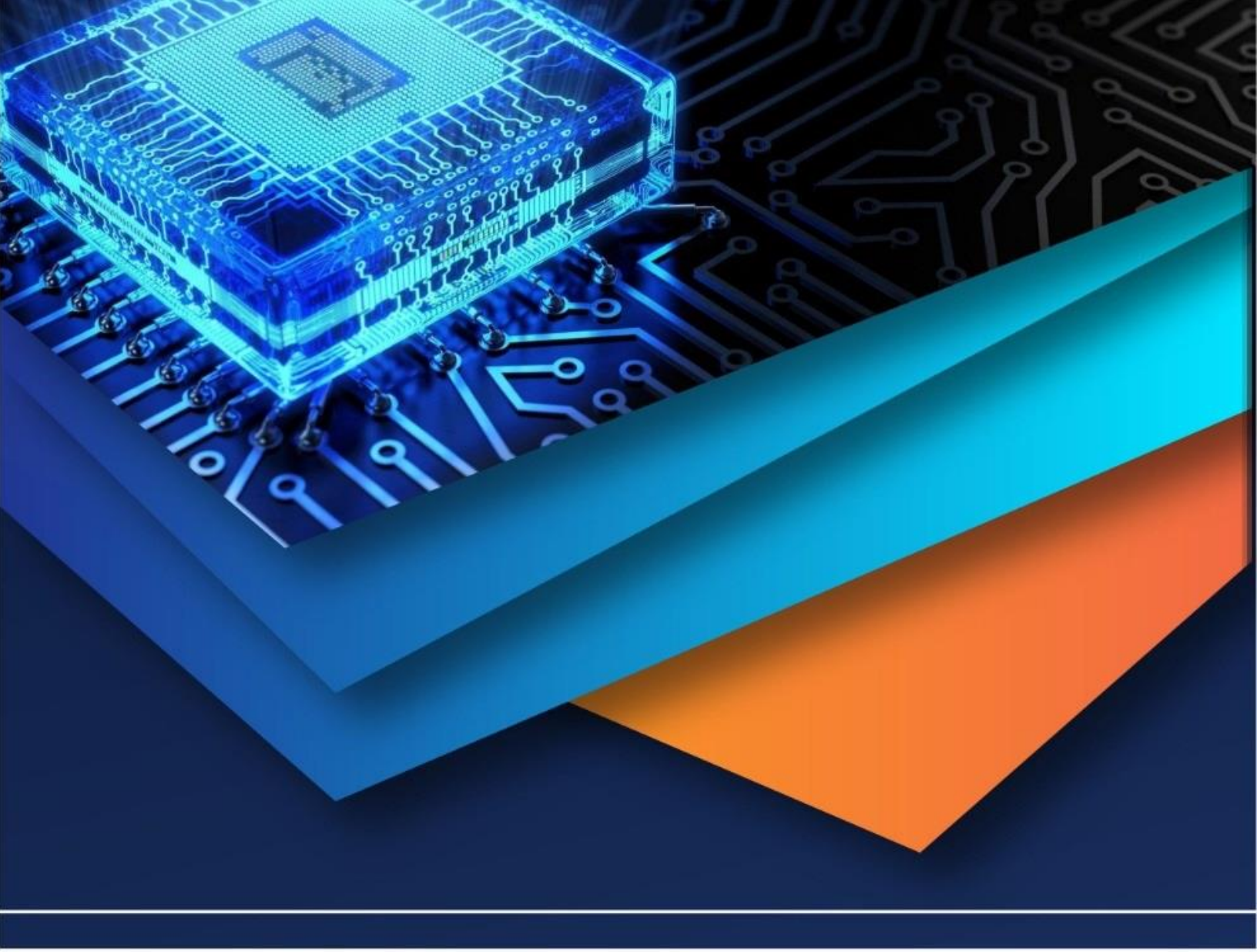

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