iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 11 **Issue:** IV **Month of publication:** April 2023

DOI: https://doi.org/10.22214/ijraset.2023.50158

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 11 Issue IV Apr 2023- Available at www.ijraset.com

A Low Power 10T SRAM Cell with Extended Static Noise Margins is Used to Implement an 8 by 8 SRAM Array in 16nm CMOS

T. Venkata Lakshmi[1], T. Edukondalu[2], S. Rahul[3], R. S. P. L Suvarna[4], T. Rohit Chaitanya[5]
[1]*Associate Professor, Department of Electronics and Communication Engineering, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru*
[2, 3, 4, 5]*Department of Electronics and Communication Engineering, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru*

Abstract: ***Thus, it must have an ultra-low power design. Low power techniques must be used to obtain SRAM cells. First, all current high performance VLSI circuits must be designed with the 10T SRAM cell, which must also be checked for write and data storage capabilities. Large amounts of data need to be stored and accessed as quickly as possible in today's world. Static random access memory (SRAM) is a type of memory that is frequently utilised in consumer devices. The necessary circuits for designing the read operation for the 88 SRAM array are the 3 to 8 Decoder, Precharge circuit, Write Driver, and Sense amplifier. commence the application of low power approaches to the SRAM cell after that. Here, the SRAM Cell is designed using two low power methods.***
Multi Threshold CMOS (MTCMOS) and Variable Threshold CMOS are examples of low power approaches (VTCMOS). The simulation results and graphic graphs show which low power method is best for lowering the dynamic power consumption of 10T SRAM cells. Using TANNER Eda V16.0, a low power 8X8 SRAM array was designed.
Keywords: Low power, Multi Threshold CMOS Technology (MTCMOS), Variable Threshold CMOS Technique, Static Random Access Memory Array (VTCMOS).

I. INTRODUCTION

More data storage capacities are constantly in demand as technology develops. This has pushed the development of fabrication technology and memory towards more condensed design principles and higher data storage densities. Information can be stored and accessed using a variety of memory. You can choose between a read-only memory, which is typically used in microcontrollers, and a read-write memory, which is typically used in microprocessors, depending on your needs. SRAM is more faster than DRAM, even though it takes up more space. It can also be made quickly. In contrast to static RAM, dynamic RAM requires refreshment at regular intervals. Thus, while having a high transistor density, SRAMs have relatively low standby power. SRAM cells are very immune to noise thanks to their greater noise margins. The CPU cache memories, small on-chip memories, FIFOs, and other buffers are where SRAM is most commonly used. Here, an 8x8 SRAM array chip is designed, and the area and latency of the complete device are analysed.

II. LITERATURE REVIEW

The primary consideration for power optimisations is the quantity of transistors employed in the circuit. Although though the SRAM circuit only needs four transistors to be designed, the additional resistive loads are required, which lowers the circuit's reliability. The load-less 4T SRAM cell's writing stability is poor [1].
The 5T SRAM cell is made to increase writing stability [2]. This circuit has a lot of leakage power because of the feedback link. By using a look ahead bias that regulates the threshold voltage dynamically, the instability of the write operation can be avoided. The 7 transistors are used in this circuit [3].
The self-controllable voltage circuit is used to lower the leakage current. Nonetheless, it has difficult data retention and transistor sizing [4]. The self-controllable voltage circuit cannot compete with the efficiency of the MTCMOS method. The 12T SRAM circuit uses the Multi Threshold CMOS (MTCMOS) technology [5]. The circuit complexity in this paper is high. The memristor is used to maximise power. Being an analogue component, the memristor has a dependable leakage power. The introduction of memristor increases the circuit's overall area [6].

III. DESIGN OF 10T SRAM CELL

A 10T (LP10T) SRAM cell with a high level of read and write stability and capability. A Schmitt-trigger inverter with a double-length pull-up transistor and a regular inverter with a stacking transistor make up the robust cross-coupled construction of the proposed LP10T SRAM cell. The read-disturbance is eliminated as a result of this and the read path being set apart from real internal storage nodes. Additionally, it uses a write-assist mechanism and executes its write operation in pseudo differential form using a write bit line and control signal. To estimate the proposed LP10T SRAM cell's performance, it is compared with some state-of-the-art SRAM cells using TANNER EDA in 16-nm CMOS predictive technology model at 0.7 V supply voltage under harsh manufacturing process, voltage, and temperature variations cell it indicates working nature of the cross coupled inverters the word line is maintained at 0.7v constantly, QA is compliment to bit line (BL) and QB is compliment to bitline bar (BLB) as shown in the Fig.

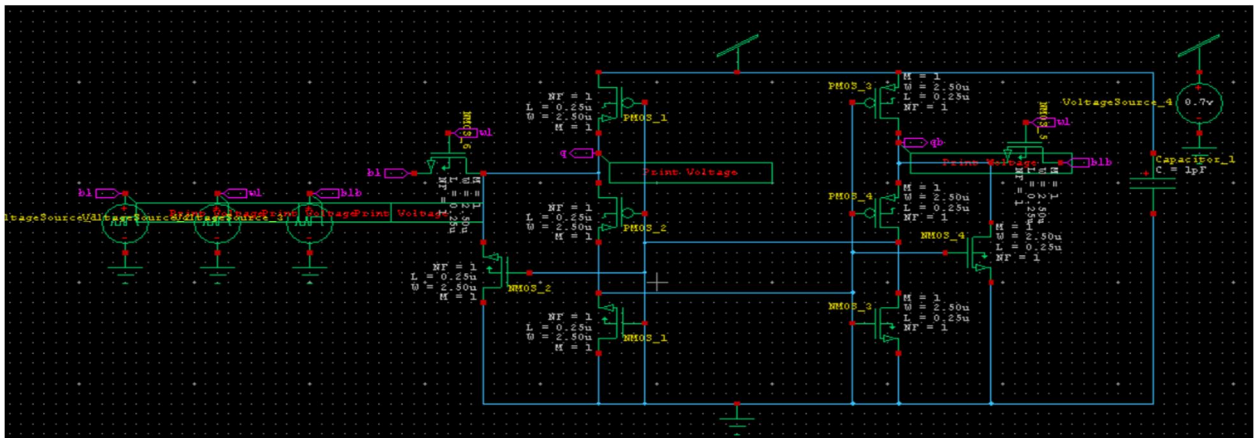


Fig: Schematic of 10T SRAM Cell

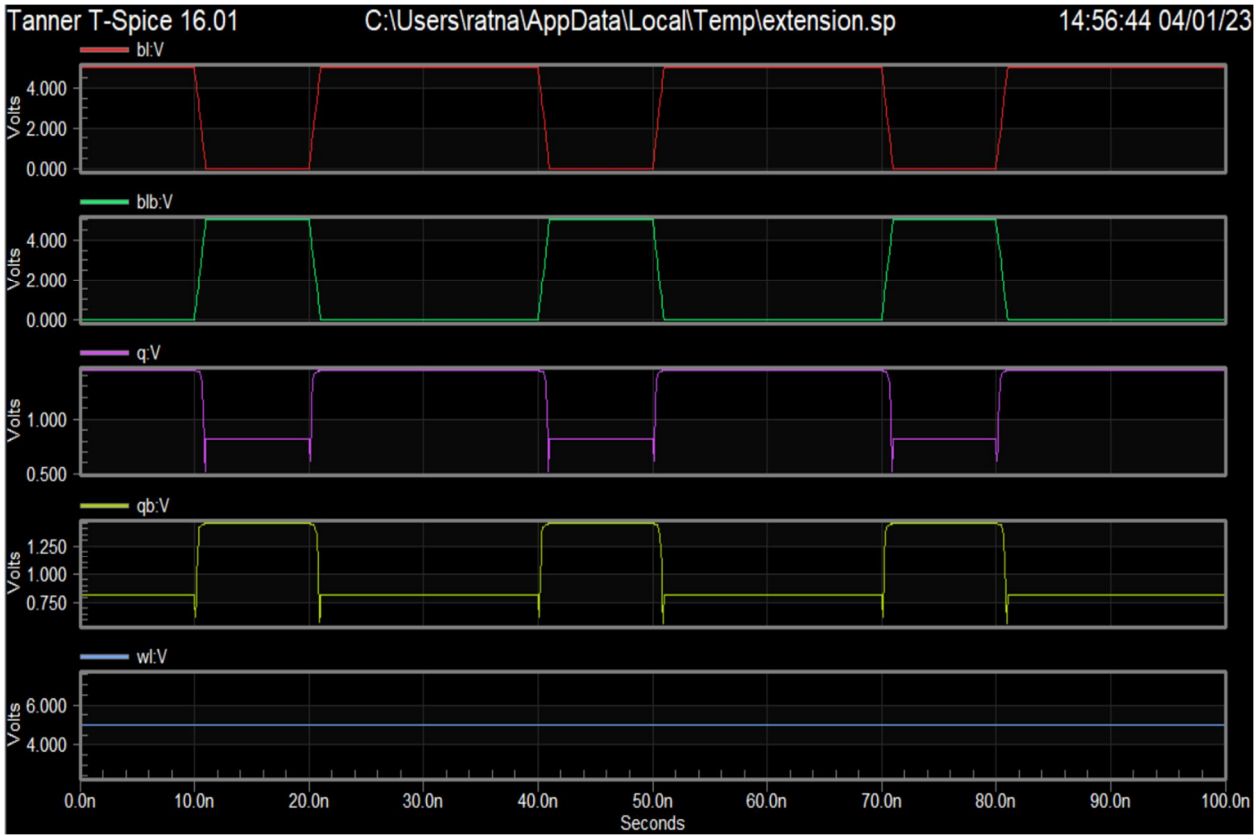


Fig: Transient response of 10T SRAM Cell

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 11 Issue IV Apr 2023- Available at www.ijraset.com

IV. BLOCK DIAGRAM OF GENERIC SRAM ARRAY

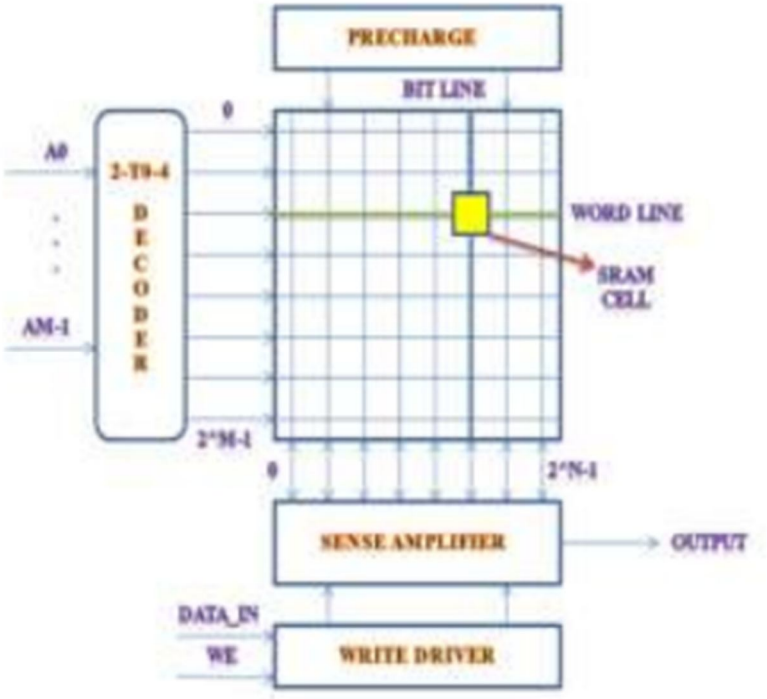


Fig: block diagram generic SRAM Array

Designing an SRAM array Initially, the SRAM Array's design subcircuits are fundamental circuits that are very important to the design of the SRAM Array. These are the SRAM cell, Write Driver, Sense Amplifier, Pre-charge Circuit, and 3 to 8 Decoder.

V. DESIGN OF 3 TO 8 DECODER

The decoder is an electrical circuit that activates the output that corresponds to the input binary number after accepting the set of inputs that form a binary number. "n" inputs and "2n" output lines make up a decoder. The 3-to-8 decoder functions in accordance with the Truth table, which is depicted in Table 1. • The eight outputs are D0, D1, D2, D3, D4, D5, D6, and D7, while the three-bit inputs are A0, A1, and A2. • The output Di is only true if the input is the binary number i. • For instance, output D0 is true and outputs D1, D2, D3, D4, D5, D6, and D7 are all false if the inputs A0, A1, and A2 are all equal to 1. • With this circuit, a binary number is "decoded" into a "one-of-eight" code.

A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Table 1. Truth Table of 3 to 8 Decoder

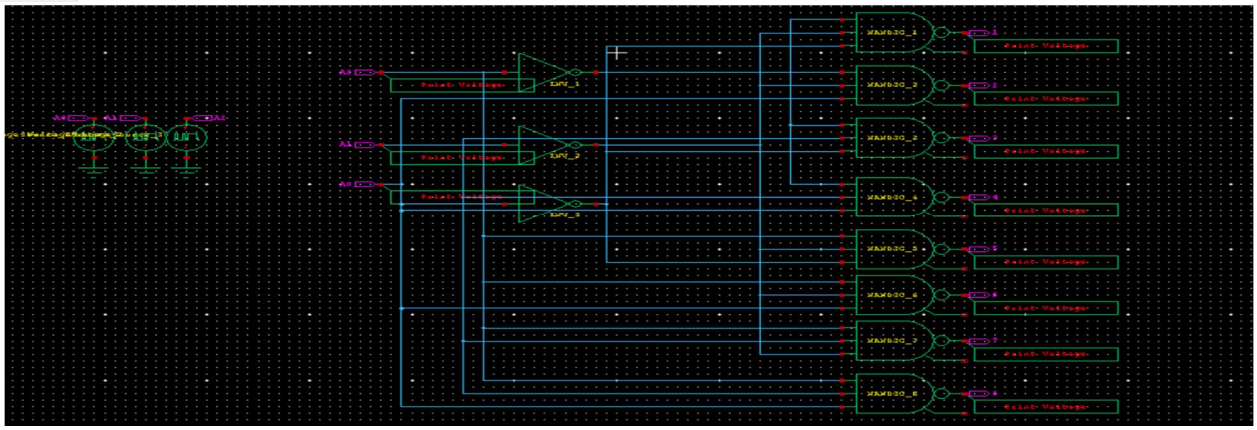


Fig : Schematic of 3 to 8 Decoder

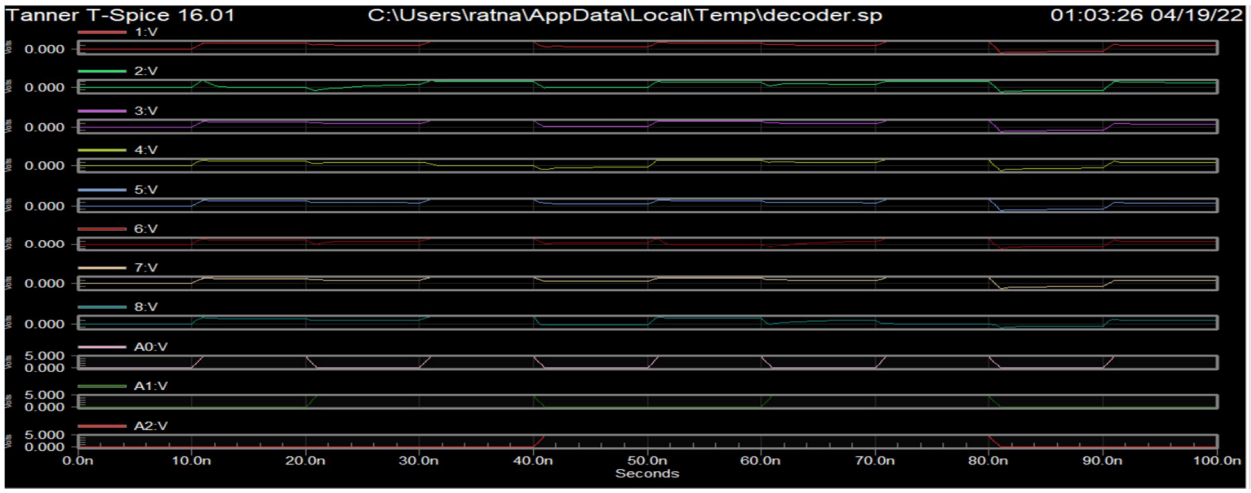


Fig: Transient response of 3 to8 Decoder

VI. DESIGN PRE-CHARGE CIRCUIT

One essential element that is continuously used in SRAM cells is the pre-charge circuit. Charge the bit and bitline-bar to the power supply Vdd=1.8v is what the pre charge does. Aside from during read and write operations, the pre charge circuits permit the bit lines to always be charged high.

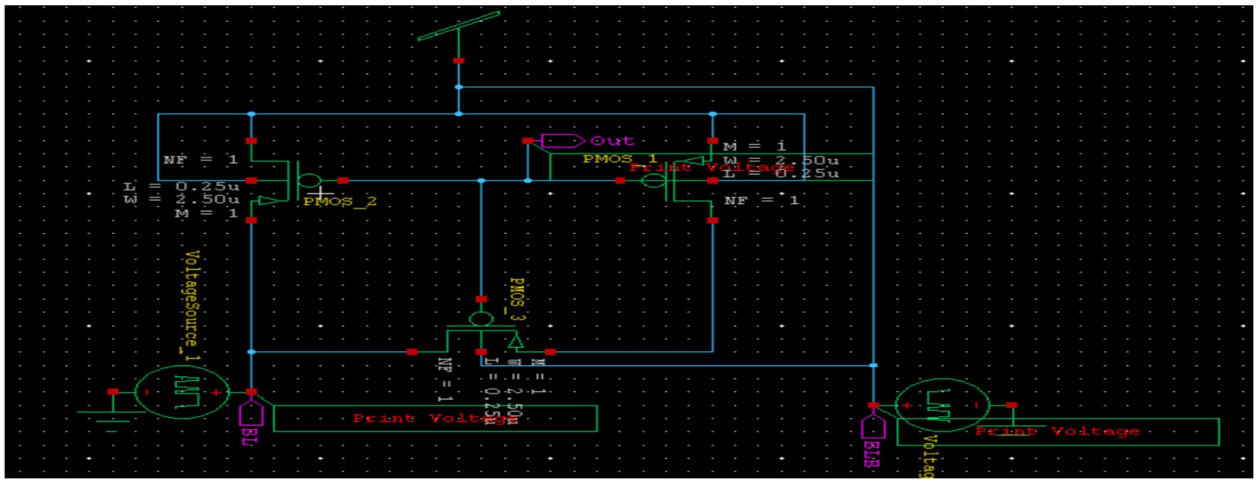


Fig: Schematic of Pre-charge circuit

In a high voltage DC application, pre-charging the power lines is a preliminary mode that reduces the inrush current during the power-up process. The differential signals can be amplified to a practical logic level thanks to the pre-charge that maintains bit lines at positive voltage.

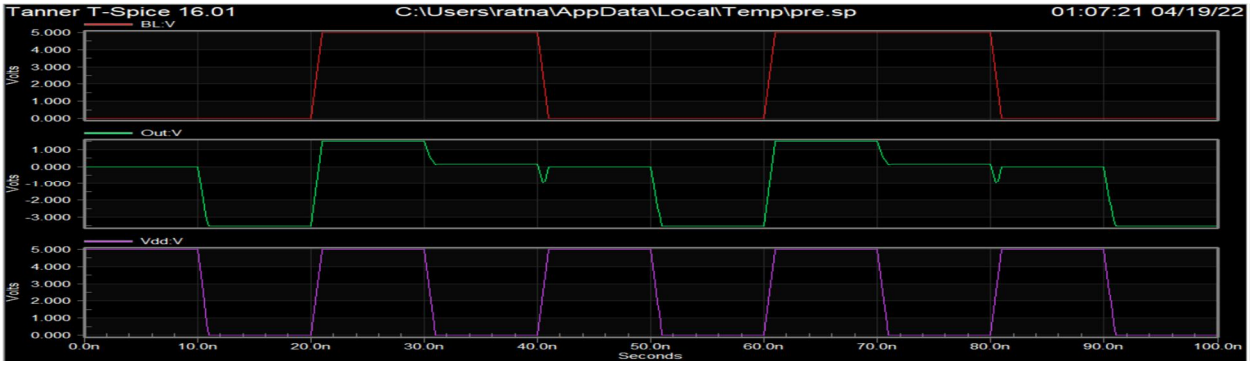


Fig : Transient response of Precharge circuit

VII. DESIGN OF WRITE DRIVER CIRCUIT

One of the key elements in the construction of the SRAM array is the write driver circuit. The write driver's responsibility is to maintain the bit line and bitline-ground bar's potential for the task at hand. The maximum supply voltage of Vdd is applied to the bit line and bitline-bar prior to this. It will be charged by using a pre-charge circuit, and then it will be discharged. The two NMOS junction points, namely 0 and 1, are given the two logics. Bit lines that are closer to the 0 logic are discharged first, and then their logic is reversed. The bit line and bitline-bar are therefore released to the ground. Bit line and bit line bar discharge occurs during this type of activity. in order to achieve zero voltage difference between the bit line, bit line bar, and ground. should make it simple for the memory cell to retrieve additional data.

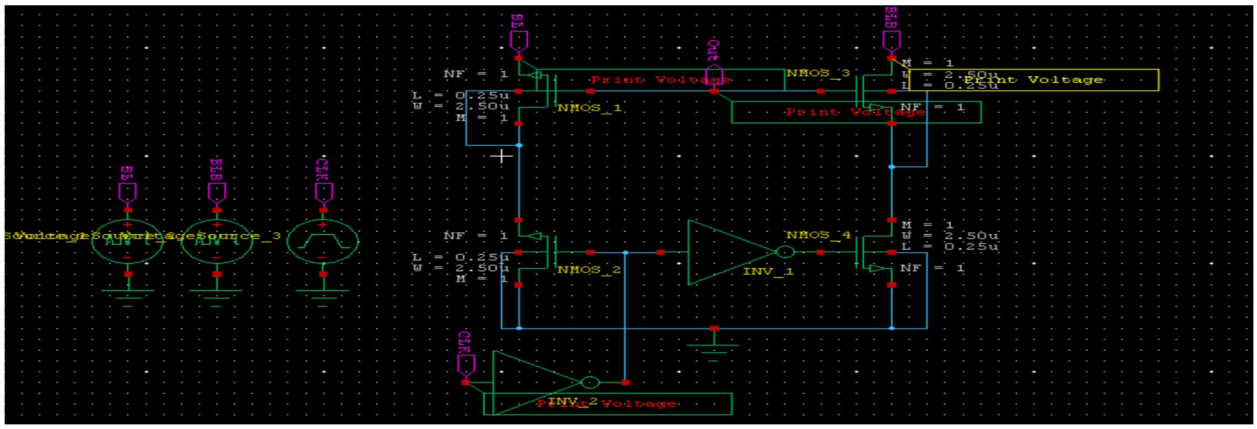


Fig: Schematic of Write driver

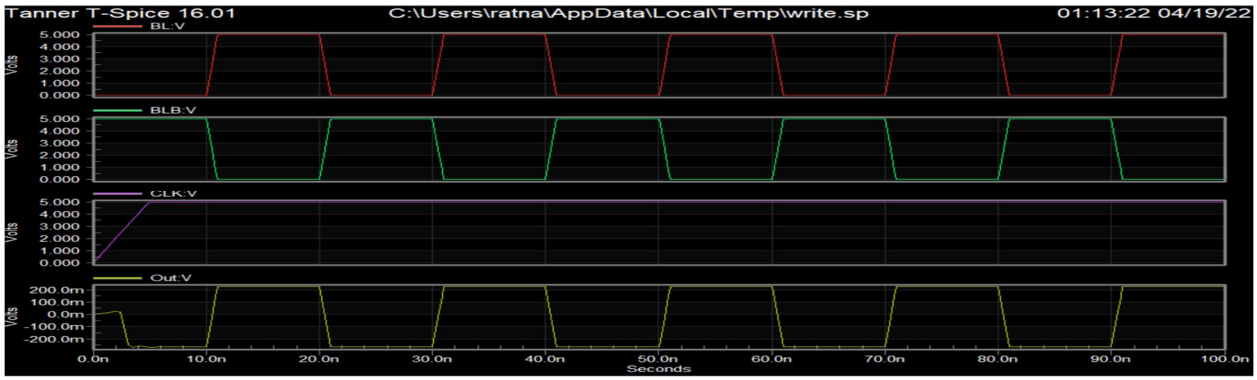


Fig: Transient response of Write Driver

VIII. DESIGN OF SENSE AMPLIFIER

In the design of the SRAM memory, the sense amplifiers are crucial. The sensing amplifier's responsibility is to detect the bit line and bitline-bar for accurate observation action. The SRAM memory cell's read and write speeds are accelerated. Getting memory design to operate with low power consumption is another task. The sense amplifiers' major function during operation is to amplify the voltage differential that is created on the bit line and bit line bar. While each segment contains one sense amplifier for a single output, we are aware that during SRAM operation, memory refresh for subsequent processes was not necessary. As a result, the sensing amplifier in the designing circuit can be used appropriately. These are some of a sense amplifier's different parameters.

Profit A =Vout/Vin

Sensitivity S is the least pronounced signal in Vin. Time of ascent t-rise, time of decline t-fall, -10% to 90%.

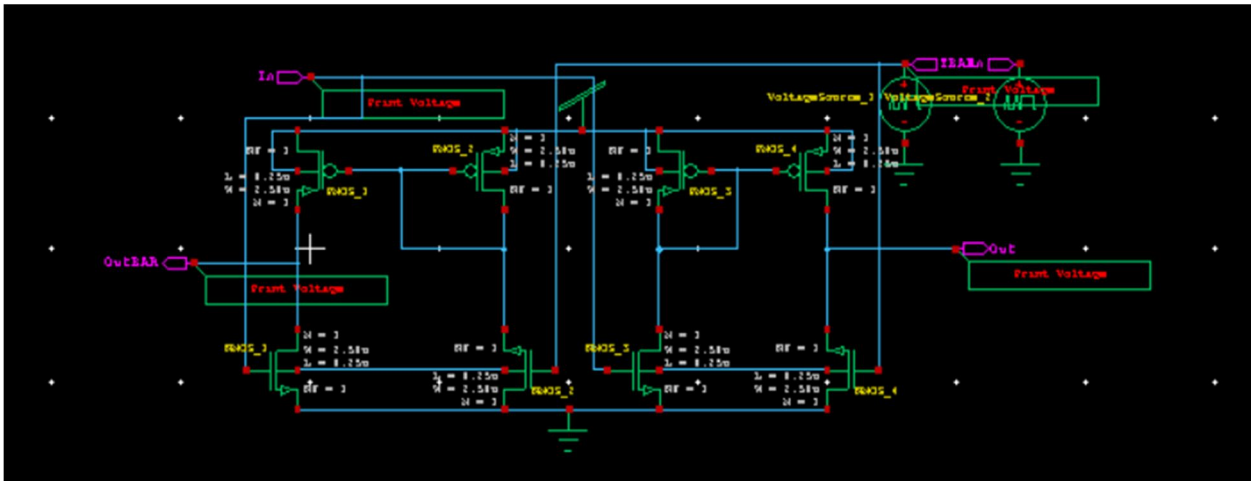


Fig: Schematic of Sense Amplifier

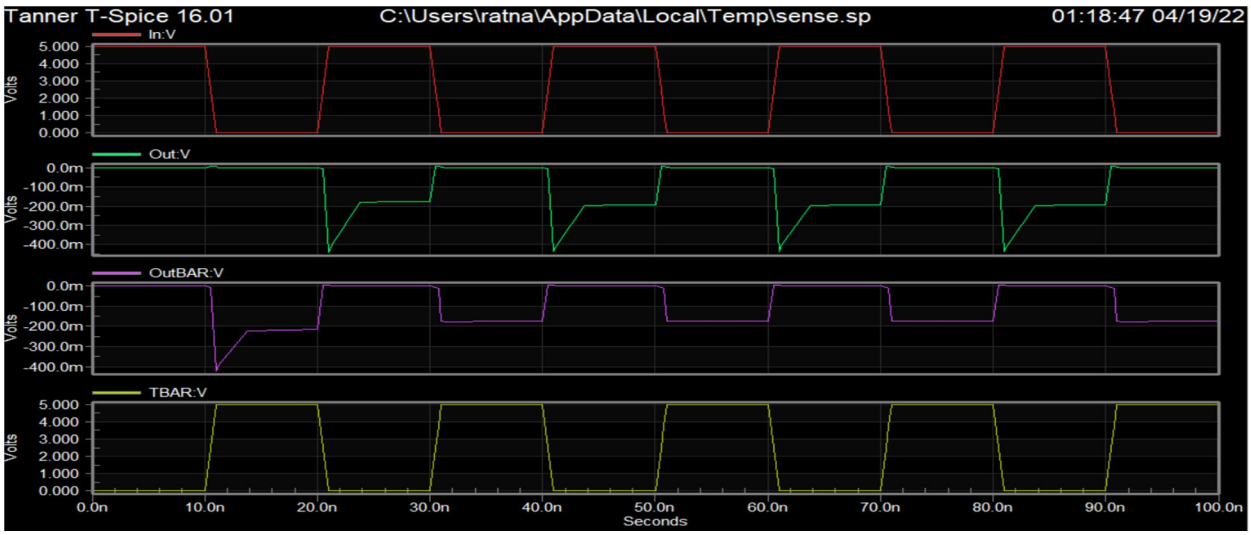


Fig: Transient response of sense amplifier

IX. DESIGN OF 8×8 SRAM ARRAY

As a result, Fig. 20 depicts the transient response for write operations 0 and 1. The WL7 and WL0 are activated here during the read operation as well in order to carry out the necessary activities. Write 1 operation occurs at QA0 and write 0 operation occurs at QB0 when the WL7 is high at a location where the WL0 is low. Hence, the procedures to write 0 and write 1 are confirmed.

As a result of the transient reaction as demonstrated by the results above, during read operations when both inputs become low, data is maintained at the constant value. When WL7 changes from high to low and WL0 changes from low to high while sense enable is on, the read operation of the memory cell is validated.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 11 Issue IV Apr 2023- Available at www.ijraset.com

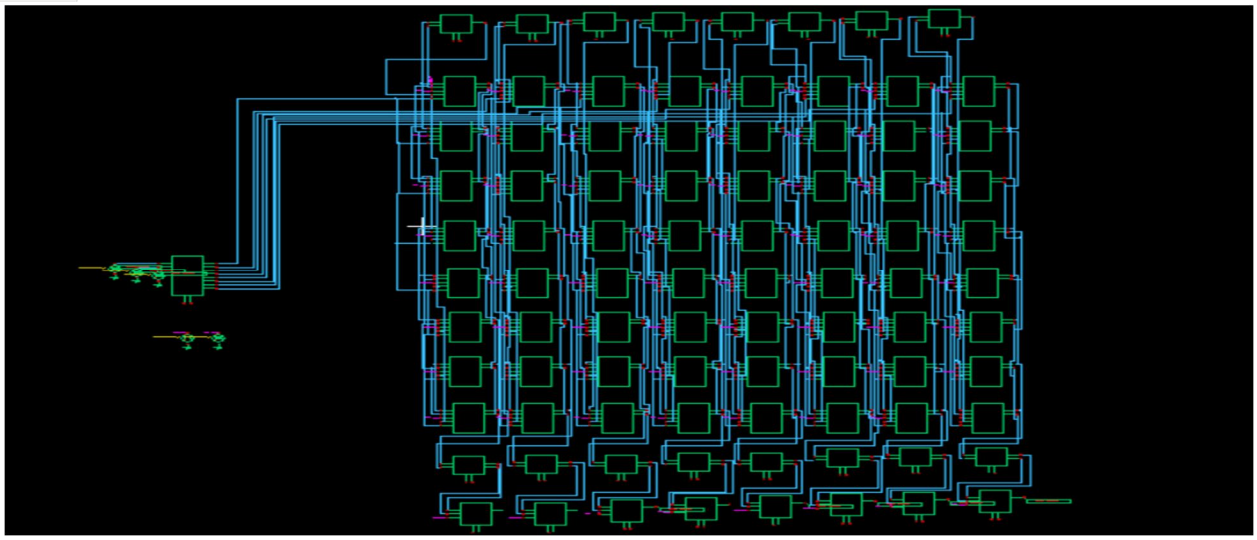


Fig: Schematic of 8×8 SRAM Array

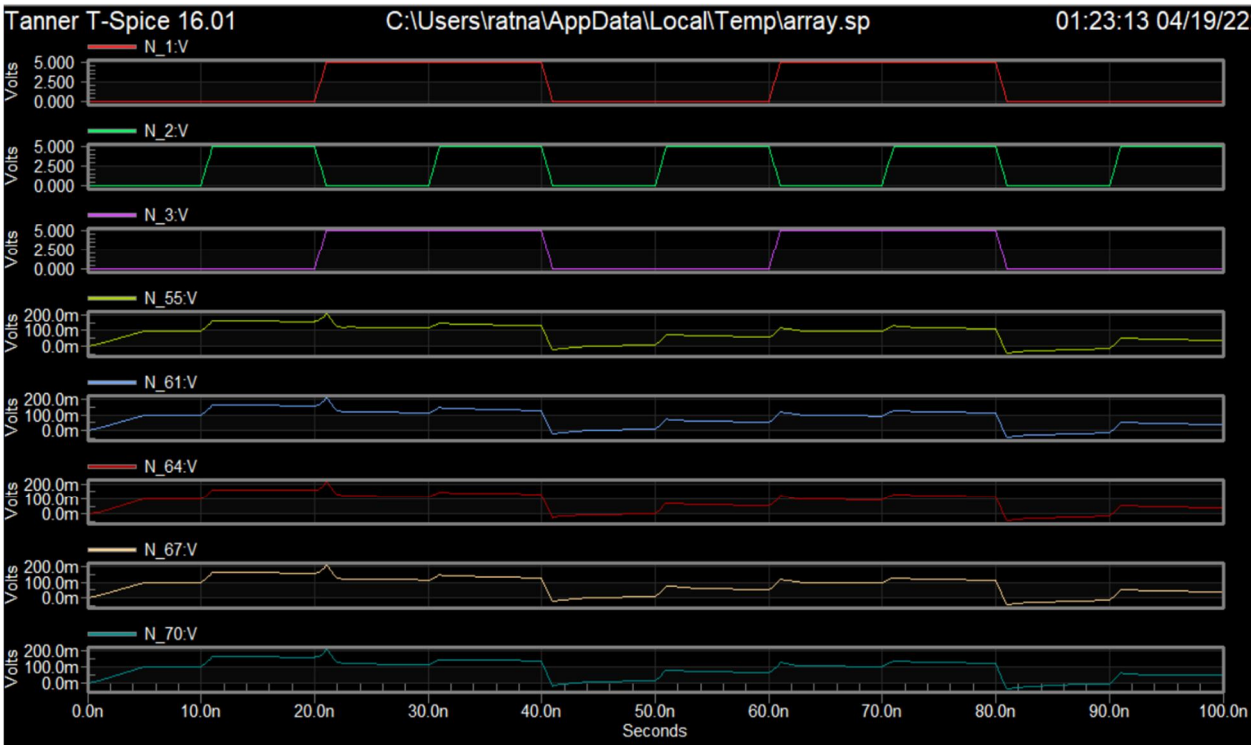


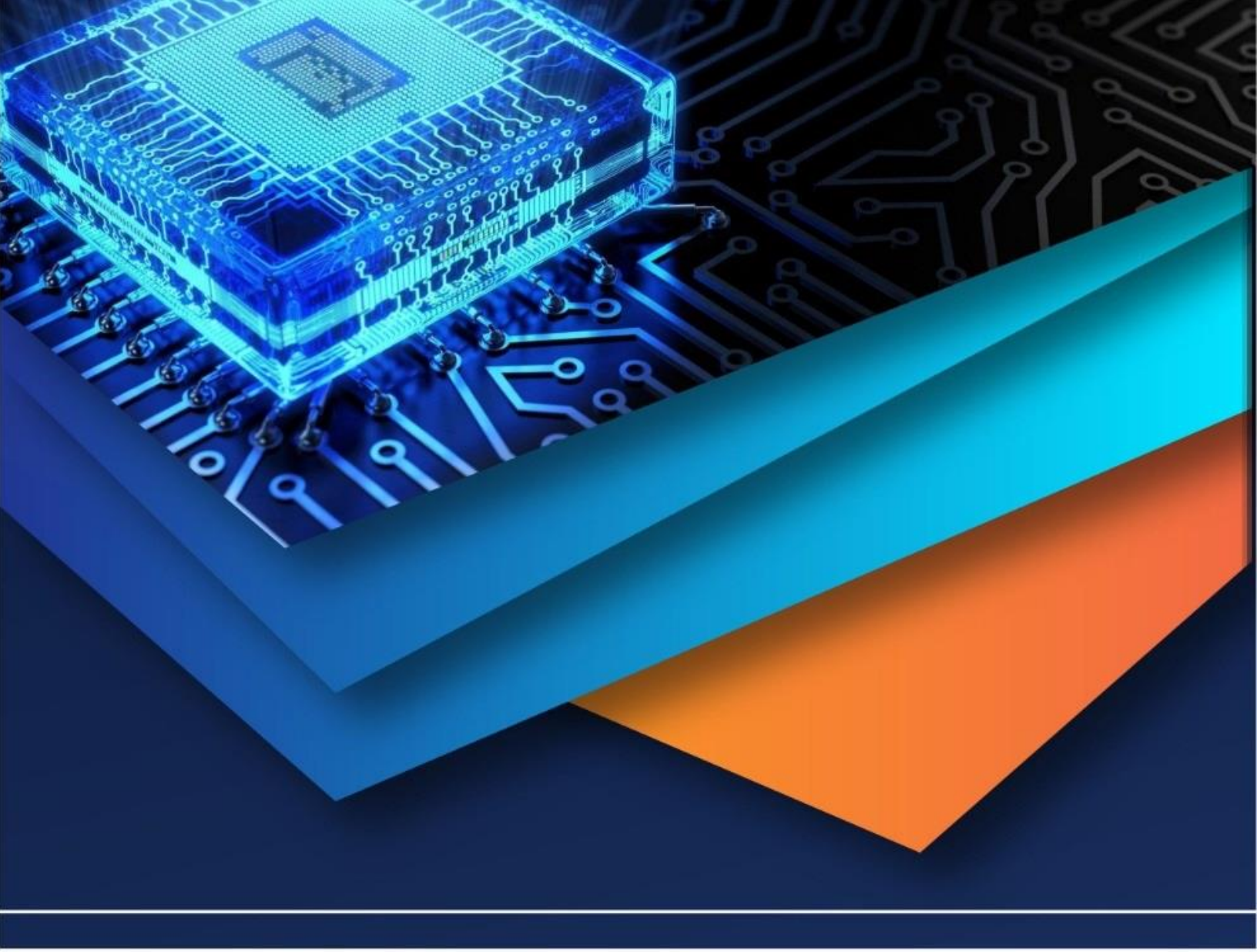
Fig: Transient response of 8*8 sram cell

X. CONCLUSION

64 bits are intended to be stored in a low power 8X8 SRAM array. A SRAM array is made up of peripheral parts, including a 3 to 8 decoder, a precharge circuit, a write driver circuit, and a sensing amplifier. Noise reduction uses a sense amplifier of the differential kind. For an 8*8 SRAM array, a supply voltage of 1.8V and a pulse input signal with a peak-to-peak voltage of 0.7.V (rail rail) and 0.7 V for SRAM cells are both acceptable. Analysis has been done on the transient reactions for read and write operations in logic-1 and logic-0. The MTCMOS Technology produced greater outcomes when low power techniques were compared to the other two techniques. In this technique, the power consumption is reduced from the standard 10T SRAM cell to 57%. In Tanner eda, SRAM array, SRAM cells, and auxiliary components are designed.

REFERENCES

[1] Robert Giterman, MaozVicentowski, Itamar Levi, YoavWeizman, OsnatKeren and Alexander Fish., "Leakage Power Attack-Resilient Symmetrical 8T SRAM Cell," IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS", no.5, May. 2018.
[2] E. Seevinck et al., "Static-Noise Margin Analysis of MOS SRAMCells," IEEE J.Solid-State Circuits, vol.SC-22, no.5 pp.748-754, Oct. 1987.
[3] Benton H. Calhaun, Anantha P. Chandrakasan "Static Noise MarginVariation for Sub-threshold SRAM in 65 nm CMOS", IEEE Journalof SolidState Circuits,, pp.1673-1679. vol.41,July 2006.
[4] Benton H. Calhoun Anantha P. andrakasan, "Analyzing StaticNoise Margin for Sub-thresholdSRAM in65nmCMOS",ESSCIRC,2005.
[5] S. Tavva et al. "Variation Tolerant 9T SRAM Cell Design"GLSVLSI"10,pp.55- 60,may 16, 2010.
[6] Arandilla,C.D.C et al."Static Noise Margin of 6T SRAM Cell in 90-nm CMOS" IEEE 13th International Conference on computer modeling and Simulation, pp.534- 539,March 30,2011.
[7] K. S. Yeo, W. L. Goh, Z. H. Kong, Q. X. Zhang, andW. G Yeo, "Highperformance low-power currentsense amplifier using a cross-coupled currentmirrorconfiguration," IEE Proc. G Circuits, Devices, andSystems, Vol. 149, No. 56, pp. 308-314, Oct. 2002.
[8] Singh S K, Singh S V, Kausik B K, Chauhan C and Tripathi T 2014 Characteriztion& improvement of SNM in deep submicron SRAM design International Conference on Signal Processing and Integrated Networkspp 538-542.
[9] Christiensen D.C. Arandilla, Anastacia B. Alvarez and Christian Raymund K. Roque 2011 Static noise margin of 6T SRAM cell in 90-nm CMOS International Conference on Modelling and Simulationpp 534-539.
[10] VanamaKundan, GunnuthulaRithwik and Prasad Govind 2014 Design of low power stable SRAM cell International Conference on Circuit, Power and Computing Technologies pp 1263-1267.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY