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A Novel Spin Based Logic Circuitry Synthesis Using SS Gate

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Abstract: ***Because of its perceived advantages, reversible logic has attracted a lot of study attention. It introduces commendable characteristics like low power consumption, minimized garbage output, and least propagation delay. Reversible logic integrated circuits (ICs) have been produced utilizing traditional CMOS topology in a number of published research endeavors up to this point. However, because CMOS technology is already experiencing a common scaling down issue, researchers are now focusing on post-CMOS devices for the manufacturing of reversible integrated circuits in the future. This particular research project is focused on related research projects that feature reversible IC design based on Spintronic. The authors first implemented spin-oriented conventional reversible logic gates and evaluated their effectiveness in terms of generated garbage values, power consumption, device integrity, and size. Later, in order to understand the benefits of the suggested Single Spin Logic based SS gate, the authors come across an SS gate that is singular in its kind and stick to its spin realization.***
Index Terms: Reversible Logic; SS Gate; Single Spin Logic; Garbage Value; Low Power Consumption.

I. INTRODUCTION

Embryonically, Reversible Logic [12] geared exclusive curiosity in terms of Low Dimensional Structures (LDS). The promising esteems of reversible circuitry corroborates the notion of loss less information processing [17, 22, 29, 30-31], low power consumption, low power dissipation, high speed computing and least garbage value generation. Counting on these integrities Researchers strove Feynman, Double Feynman, Toffoli, Fredkin, Peres gates [15] and so on. To pace up with robust [18] technologies Researchers concurrently initialized several subsets such as multiplier [3] using Peres gate, adder [14] using DKG gate, binary to gray converter [10] using Feynman gate, ALU [33] using Feynman, Peres and Fredkin gate and so on. The goodliness of reversible topology [16] was soon benchmarked with its traditional counterpart. One imperative precondition is the elimination of garbage value. This in particular reduces the heat dissipation and power consumption. The quantum cost is an annexed feature of reversible logic which is largely pondered over. Categorically reversible logic circuitry is now enormously scaled to foster future ready computational ICs [19-21, 23-28], RAM, ROM, ASICs and FPGAs. Nonetheless the reversible circuits are comprised of CMOS composite materials and being indebted to intrinsic limitations of CMOS technology, the MOSFET reversible circuitry suffers the pitfall of scaling limitations. But contemporary research articles exhibit countless strives to ratify the scaling limitations of CMOS [5].

Spintronics is one such post CMOS versatile technology that discourse the obscurities of CMOS scaling. It preserves both intrinsic spin of electron and its conjoined magnetic momentum keeping aside the elementary charge of an electron. It indeed exercise maneuvering electron in metal, semiconductors and in heterostructures. Thus spin positioned information processing incorporates a stipulated technology to inject, store, control and manipulate information with the span of spin degree of freedom. Several spin based device proposal fortified spin based circuit realizations and logicalizations including Single Spin Logic (SSL) [32]. These elements mark the dawn of spintronics era.

The authors here realized reversible logic circuitry under the daybreak of SSL and subsequently ventured into a new paradigm of SSL reversible circuitry. Erstwhile the authors have reported such SSL reversible circuitry. In furtherance to such pain sticking endeavor here the authors put forward few noteworthy SSL reversible logicalizations and subsequently tender SSL SS gate and confer its modus operandi.

Accordingly, the authors adhere to SSL SS gate based Half adder and Full adder and outline the attributes of the modeled combinational circuits in terms of garbage value, power consumption, device integrity, robustness, heat dissipation and eventually the ‘no requirement’ of interconnections.

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II. THE ORTHOGONALITY OF SPIN REVERSIBLE LOGICALIZATION

The intrinsic spin of an electron steadfast two spin set i.e. spin up '↑' and spin down '↓'. This two existing non-degenerate orthogonal spin state are ultimately parallel and anti-parallel to the magnetic field and mutually they encode classical bit '1' and '0'. The closest adjoining spin exchange information endowing a three phase clock is fed in unidirectional to the signal flow from input to output. This favors spintronics from conventional physical charge based devices and profoundly dissipates low or no heat even at higher processing speed. The spin degree of freedom in associations to spin interaction is customized for encoding qubit in quantum logic gates. This covalent structure enthuse SSL which detects and controls spin degree of freedom exchange amid ferromagnetic metallic or ferromagnetic semiconductor hetero-structures. Robustly SSL expanded plentifully to be seized in a quantum dot and substantial research has been reported so far to marshal spin in a low magnetic field. SSL based NAND gates (Agarwal et.al), Full Adder (S. Shukla et.al.), Multiplexer (T.K. Bhattacharyya) are designed beforehand [7]. To attain akin pinnacles authors here implement SSL know-how in BJN Gate [9], TR Gate [4], R Gate [2], MUX Gate [13], New Gate [1], NFT Gate [11] and SS Gate [6].

III. ARTICULATION OF SSL IN REVERSIBLE LOGIC DOMAIN

Spin composed electronic research quantized information processing in nano devices. Prior to this work the authors have proposed SSL based Reversible logic circuits as demonstrated in [8]. Authors here chronologically report the novel architectures of SSL synthesized other few notable Reversible Logic Gates (RLG) in which green arrow indicates the input and blue arrow provides the output.

A. BJN Gate

Fig. 1 is the SSL realization of 3×3 BJN gate with three inputs (A, B, C) and three outputs given by $P=A$, $Q=B$, $R= (A+B) \oplus C$, respectively. It's quantum cost is 5 and the Garbage Value is limited to zero.

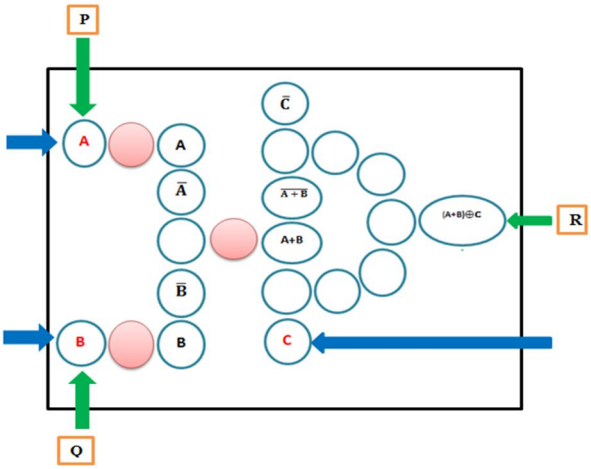

Fig. 1. SSL based BJN gate.

B. TR Gate

Fig. 2. is another 3×3 SSL based TR Gate having inputs A,B,C and its corresponding outputs are $P= A$, $Q=A\oplus B$, $R=AB\oplus C$. It has Quantum Cost 6 and the garbage value is limited to zero.

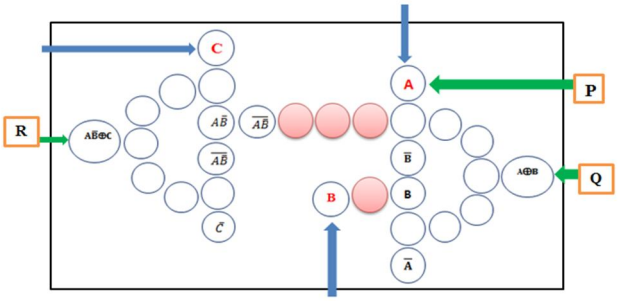

Fig. 2. SSL based TR gate.

C. R Gate

Apart SSL-BJN and SSL-TR gate, R gate is a crucial 3×3 reversible gate and its SSL realization is shown in Fig. 3. This gate is generally commissioned to invert a signal and also to duplicate a signal. The inputs are (A, B, C) and outputs are $P=A\oplus B$, $Q=A$, $R = AB \oplus C$ Similar to prior gates the R gate does not possess any garbage value.

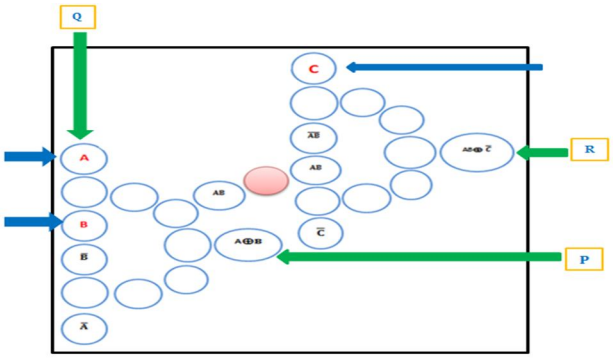

Fig. 3. SSL based R gate.

D. MUX Gate

Fig. 4 shows 3×3 MUX Gate having inputs (A, B & C). The outputs are expressed by $P=A, Q = A \oplus B \oplus C$, $R = \bar{A}C + AB$ in SSL domain and its Quantum Cost is 4. It produces merely 2 garbage values.

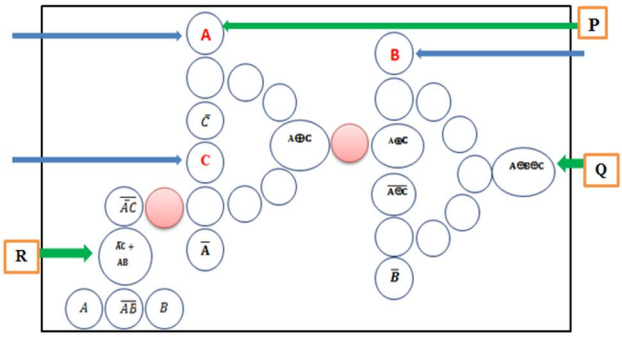

Fig. 4. SSL based R gate.

E. New Gate

The New gate is a 3×3 Gate shown in Fig. 5. The inputs are (A, B, C) and outputs are $P=A, Q = AB \oplus C$, $R = \bar{A}\bar{C} \oplus \bar{B}$. The fragility of this gate is that its Quantum Cost is still unknown. Its garbage value is limited to one.

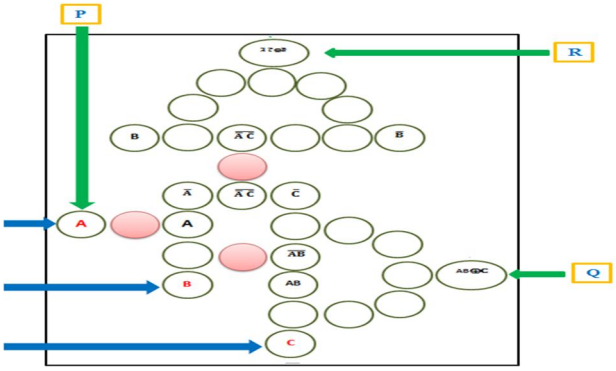

Fig. 5. SSL based New gate.

F. NFT Gate

Noval Fault Tolerant or NFT reversible gate is a 3×3 reversible gate shown in Fig. 6. The inputs are given by (A, B, C) and outputs are taken as $P = A \oplus B$, $Q = \bar{B}C + A\bar{C}$, $R = BC + A\bar{C}$. Its Quantum Cost is 5 and the garbage value is two.

The credentiality of such RLGs are largely co-related to fundamental of spin. In order to disseminate the garbage value enough care is taken upon in realizing the SSL RLG circuits. Eventually the authors with the cost for highest accuracy in reversibility proposed SS gate and its nobilities are low quantum cost, production of less garbage value, high processing and other few merits. Basically the authors resonate an amicable model that is to be incorporate in future ICs [34].

IV. SS SPIN GATE REALIZATION

This is a new reversible gate named after first letter of the authors' name. This is a 3×3 reversible gate. Primarily the authors conclave a stochastic approach and substantiate the model with its CMOS counterpart.

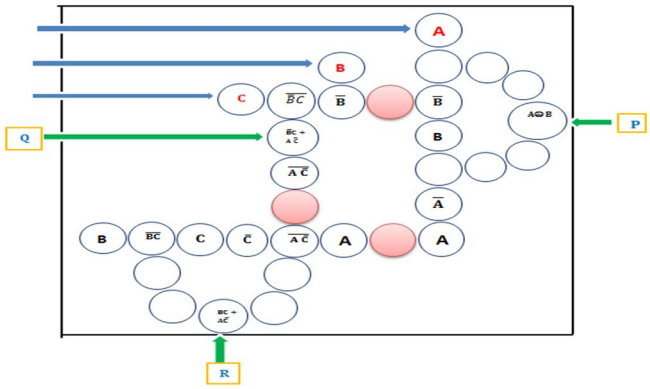

Fig. 6. SSL based NFT gate.

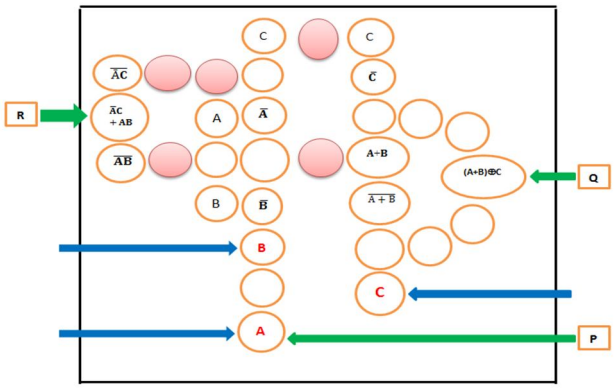

Fig. 7. SS gate in SSL domain.

The SSL realization of SS model is shown in Fig. 7. It has inputs A, B, C and outputs $P = A$, $Q = A \oplus B \oplus C$, $R = \bar{A}C + AB$.

Now to validate SS gate the Half adder, Half subtractor and 1-bit comparator are devised and then after introspection of the attributes of the designed Half adder, Half subtractor and 1-bit comparator are compared with their conventional counterpart. The main advantage of this gate is it can work as a half subtractor if one of the input is turned to zero as shown in Fig. 8. Here the garbage value is maximized to 'one' only as JMS gate itself upholds all the requisite criterion itself of the Half subtractor marked by red arrow.

V. CONCLUSION

The authors earlier analytically studied the approximation of SSL in the reversible vicinity. This particular research endeavor is a frame work to deliberate the notion of SSL in variety of reversible circuitry and above all the proposed SS gate is realized using SSL to perpetuate the heterogeneity of spin degree of freedom. The linearity of such model is bestowed upon the physiognomies of spin structure in ferromagnetic metal as well as in ferromagnetic semiconductor.

The inheritance of such circuits is vested upon the users' proficiency in improvising spin in the nano region. Moreover, the comparative analysis postulate all benevolence of spin technology uninterruptedly and uncompromisingly.

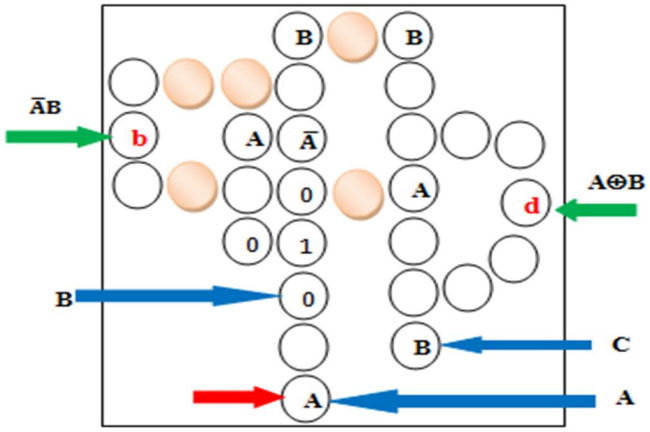

Fig. 8. SS gate based SSL Half Subtractor.

Thus the authors adhere to such reversible logic invention using spin topology and anticipate to maximize its incorporation for future elegant solution of the dead end of CMOS. Lastly the authors acknowledge this specific research maneuver as a fascinating but challenging series of action.

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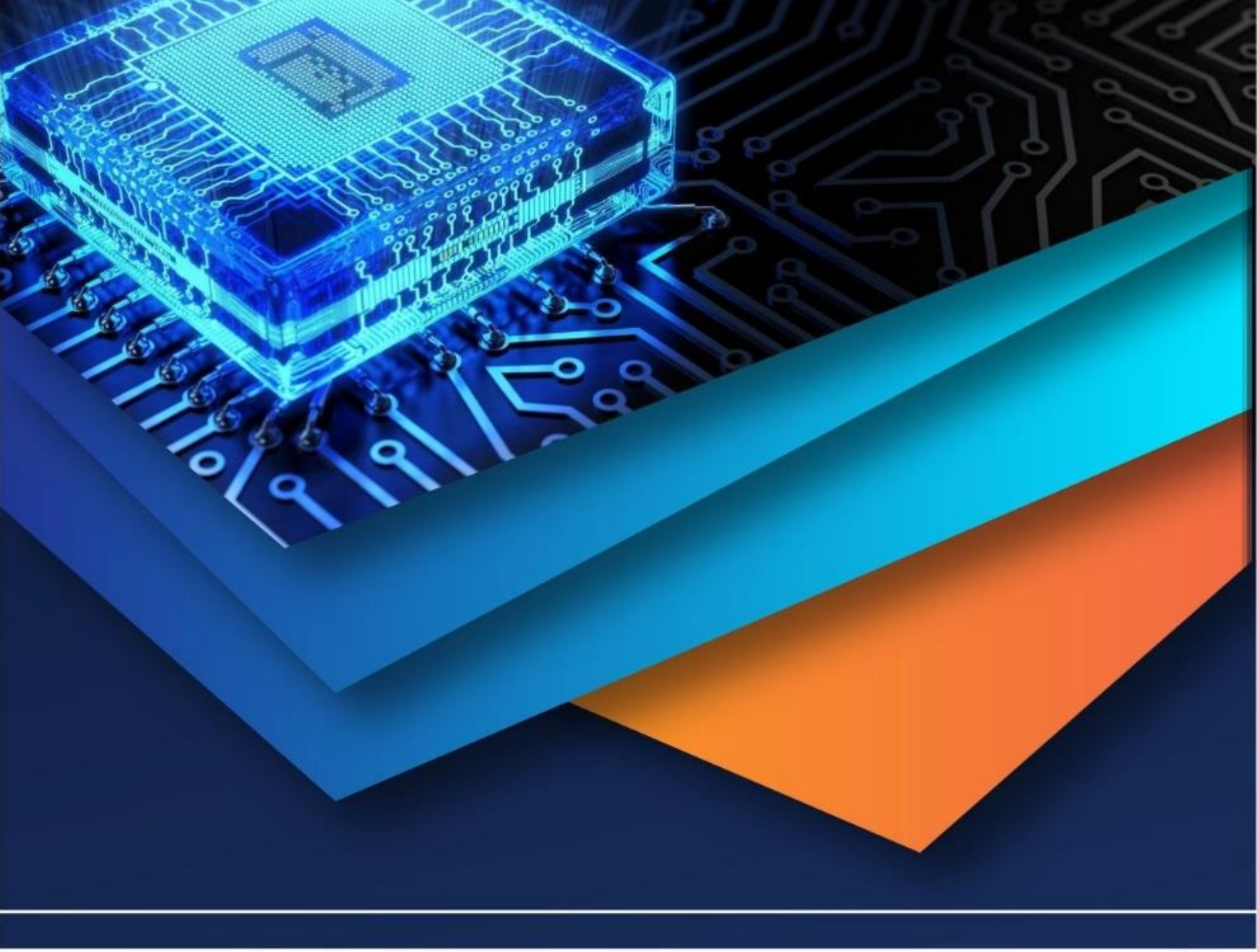

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