iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 10 **Issue:** III **Month of publication:** March 2022

DOI: https://doi.org/10.22214/ijraset.2022.40523

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue III Mar 2022- Available at www.ijraset.com

Adders implemented on VLSI for high-speed ALU

Meeth Jain[1], KB Ramesh[2]
[1, 2]*Electronics and Instrumentation, RV College of Engineering*

Abstract: ***This study focuses on the development of high-speed adder circuits utilising the Hardware Description Language (HDL) within the Xilinx ISE 9.2i platform, as well as their implementation on Field Programmable Gate Arrays (FPGAs) to analyse planning parameters. The main building component of the Arithmetic Logic Unit (ALU) is the adder, and hence the performance of the Control Processing Unit is determined by it (CPU). The ALU and the register file are the two primary components of processors. The carry-chain extra operation could be one of the important channels within an ALU. In this paper, we've simulated and synthesised a variety of adders in order to find the most efficient one.***
Keywords: Adders, ALU, CPU, High speed adders, delay

I. INTRODUCTION

The digital computer LU is a branch of logic design with the goal of developing appropriate algorithms in order to achieve the most efficient use of the available hardware. Only a relatively small and precise set of Boolean operations and arithmetic can be performed by the hardware.
Operations are based on a hierachy of operations that are developed utilising algorithms against the hardware. Because, ultimately, speed, power, and LU utilisation are the most commonly cited measures of an algorithm's efficiency.

A. What is an Adder

In digital electronics, adder is a digital circuit that performs addition of two numbers. many computers and other kinds of processors, adders are used not only in the ALU(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and many more.
Consider two binary variables x and y. The binary sum is denoted by x + y, such that
0+0=0 0+1=1 1+0=1 1+1=10. Here, the result in the last case is a binary 10 (i.e., 2 in base 10). The sum of two numbers can be out of the range of the digits in binary set. This, of course, is the origin of the concept of a carry out. In the binary sum 1+1, the result 10 is viewed as a 0 with a 1 shifted to the left to give a "carryout is 1".

1) *Half Adder*: A Half Adder (HA) is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits. The Boolean equation and Truth table of half adder: S = A XOR B ; C = A AND B

Fig. 1 Half Adder Circuit

Table I
Truth Table of Half Adder Circuit

Input		Output	
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue III Mar 2022- Available at www.ijraset.com

2) *Full Adder*: A Full Adder (FA) is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, which are both binary digits. A FA adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and Ci here A, B are the operands, and Ci is a bit carried in. The circuit produces a two-bit output sum typically represented by the signals Co(Carry) and S(Sum). The Boolean equation and truth table: S = A XOR B XOR Ci ; Co = (A AND B) OR (B AND Ci) OR (Ci AND A)

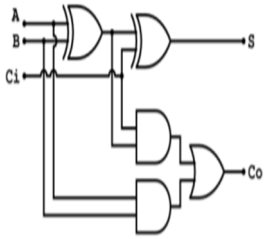


Fig. 2 Full Adder Circuit

Table II
Truth Table of Full Adder Circuit

A	B	C_{in}	C_{out}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

B. Complex Adders

The reference to eve of adding single bits, let"s extend it to adding binary words. In general, adding two n-bit words yields an n-bit sum and a carry-out bit Cn. The carry is carried from lower bit adder to higher bit adder. Based on carry transfer from LSB to MSB, the adders are classified.

1) *Ripple Carry Adder:* "It is possible to create a logical circuit using multiple full adders to add N-bit numbers." Each full adder inputs a carry Cin which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder (RCA) in, since each carry bit "ripples" to the next full adder.

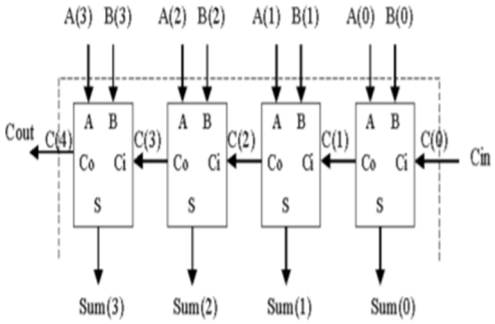


Fig. 3 Ripple Carry Adder Circuit

2) *Carry-Look Ahead Ladder:* "Carry-Look ahead Adder is designed to overcome the latency introduced by the repelling effect of the carry bits in RCA." The improves speed by reducing the amount of time required to determine carry bits. Carry lookahead logic uses the concepts of generating (G) and propagating(P)c

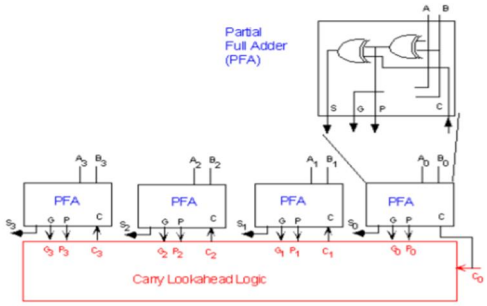


Fig. 4 Carry Look-Ahead Adder Circuit

Table III
Truth Table of Carry Look-Ahead Adder Circuit

A	B	Ci	C i +1	Condition
0	0	0	0	No carry generate
0	0	1	0	
0	1	0	0	
0	1	1	1	No carry propagate
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry generate
1	1	1	1	

II. PROPOSED METHODOLOGY

A. The Alternate Approaches for Designing of High-Speed Adders(HSA) are Discussed:

1) *Carry Skip Adder*: The carry-skip adder is meant to speed up a long adder by adding the propagation of carry bit round a portion of the whole adder. The concept is illustrated in the context of a four-bit adder. The carry-in bit is designated as I and the adder itself generates a carry-out bit of i+4. Two logic gates make up the carry skipping circuitry. The ND gate recognises the carry-in bit and compares it to the group propagate signals.P(i,i+3) = Pi+3. Pi+2.Pi+1.P

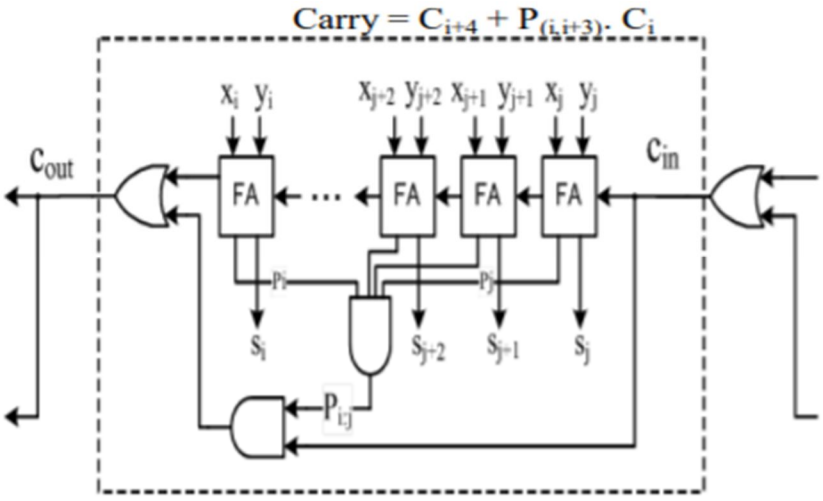


Fig. 5 Carry Skip Adder Circuit

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue III Mar 2022- Available at www.ijraset.com

2) *Carry Select Adders*: Carry Select Adders (CSA) use multiple narrow adders to create fast wide adders. Consider the addition of two n bit numbers with a = an-1…..a0 and b = bn-1…..b0. At the bit level the adder delay increases from the least significant 0th position upward, with the (n-1)th requiringthe most complex logic. A carry select adder breaks the addition problem into smaller groups. A carry-select adder provides two separate adders for the upper words, one for each possibility. A multiplexer (MUX) is then used to select the valid result.

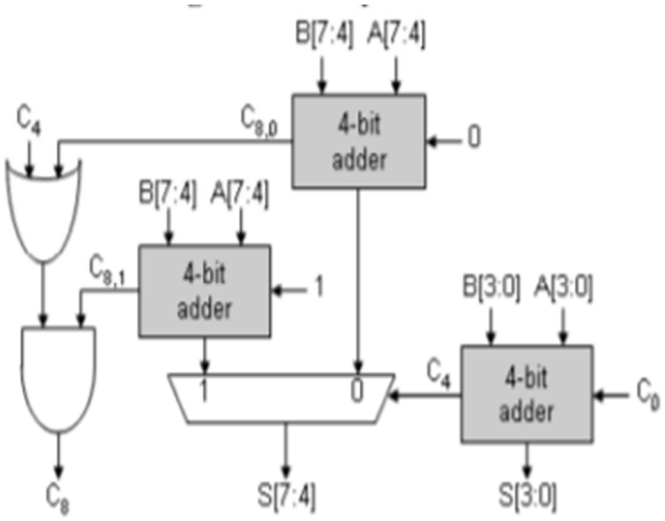


Fig. 6 Carry Select Adder Circuit

3) *Carry Save Adder*: Carry – save adder is based on the idea that a complete adder really has three inputs and produces two outputs, as shown. While it is most commonly used to associate the third input with a carry in, it might also be used as a "regular" value. The complete adder is utilised as a 3:2 reduction network, where it starts with bits from 3-bit words, adds them, and then outputs a 2-bit wide output. Using n separate adders, an n-bit carry save adder may be constructed. The word carry-save comes from the fact that we save the carry out words instead of using them right away to calculate the final sum. When we need to add more than two numbers, carry-save adders come in handy. Because the design is generated automatically avoids the delay in the carry-out bits.

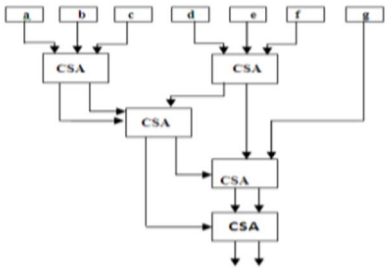


Fig. 7 Carry Save Adder Circuit

III. RESULT AND DISCUSSION

The design of high speed adders is necessary to increase the computation speed of ALU and it supports to the design of high speed processor. In this research, the hardware implementation of various adders has been done to analyze the speed and area. And the following data has been interpreted

16-bit adders: "The total time delay for ripple carry adder, carry-look ahead adder, carry-skip adder and carry-select adder was approximately 21.6 ns, 21.6 ns, 16.6 ns, 23.1 ns respectively."

8-bit adders: "The total time delay for ripple carry adder, carry-look ahead adder, carry-skip adder and carry-select adder was approximately 13.2 ns, 13.2 ns, 11.5 ns, 15.9 ns respectively."

IV. CONCLUSION

The research article describes about the hardware implementation of high speed adders. In this paper, the various adders like full adder, ripple carry adder, carry-look ahead adder, carry-skip adder and carry –select adder have been simulated and synthesized. Finally, the captured parameters like speed and area are compared for 8 –bit and 16-bit adders. This paper concludes that the carry-skip adder is the most efficient adder in speed and area consumption.

REFERENCES

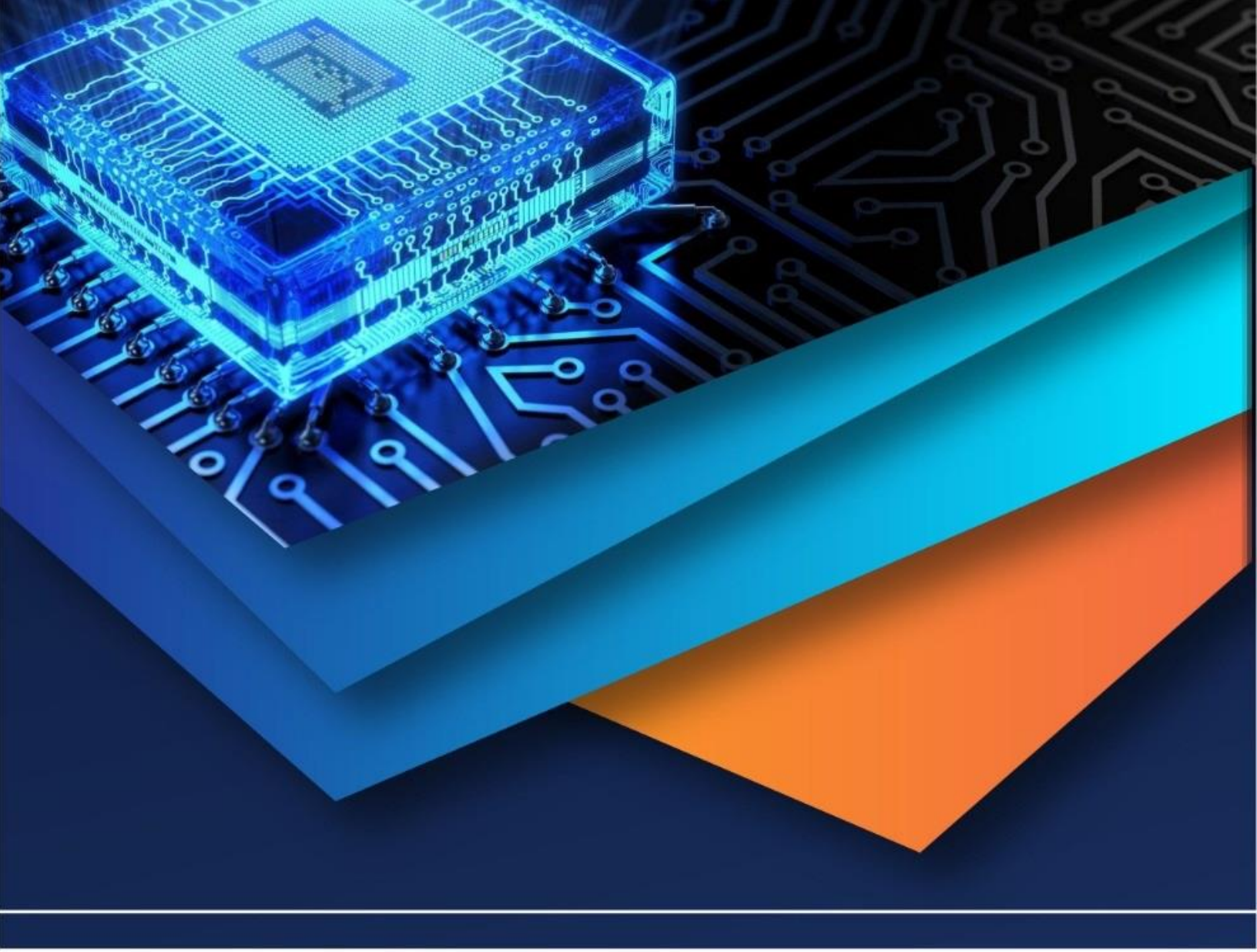
[1] Simson and D. S, "Design and Implementation of High Speed Hybrid Carry Select Adder," 2021 International Conference on Advances in Electrical, Computing, Communication and Sustainable Technologies (ICAECT), 2021, pp. 1-6, doi: 10.1109/ICAECT49130.2021.9392452.

[2] Y. d. Ykuntam, K. Pavani and K. Saladi, "Design and analysis of High speed wallace tree multiplier using parallel prefix adders for VLSI circuit designs," 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT), 2020, pp. 1-6, doi: 10.1109/ICCCNT49239.2020.9225404.

[3] B. Harish, K. Sivani and M. S. S. Rukmini, "Design and Performance Comparison among Various types of Adder Topologies," 2019 3rd International Conference on Computing Methodologies and Communication (ICCMC), 2019, pp. 725-730, doi: 10.1109/ICCMC.2019.8819779.

[4] Ananthakrishnan, A. Ajit, A. P.V., K. Haridas, N. M. Nambiar and D. S., "FPGA Based Performance Comparison of Different Basic Adder Topologies with Parallel Processing Adder," 2019 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA), 2019, pp. 87-92, doi: 10.1109/ICECA.2019.8821925.

[5] K. A. K. Maurya, Y. R. Lakshmanna, K. B. Sindhuri and N. U. Kumar, "Design and implementation of 32-bit adders using various full adders," 2017 Innovations in Power and Advanced Computing Technologies (i-PACT), 2017, pp. 1-6, doi: 10.1109/IPACT.2017.8245176.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY