iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 12 **Issue:** II **Month of publication:** February 2024

DOI: https://doi.org/10.22214/ijraset.2024.58338

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue II Feb 2024- Available at www.ijraset.com

Analysis of Two Stage CMOS Operational Amplifier in 90nm CMOS Technology

K. Guru Sai Kavya[1], G. Nagasowmya[2], G. Ankitha[3], K. Bharathi[4], K. Reshma[5], M. Sharmila[6]
Department of ECE, Sri Venkateswara College of Engineering, Tirupati, Andhra Pradesh, India

Abstract: ***Operational amplifier circuits are used in computation, instrumentation and other applications. Precision op-amps previously used in instrumentation are now-a-days being used in industrial and automotive applications. Hence, there always exists a need for better precision op-amps. It should operate under a wide temperature range. Nowadays, due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip, Complementary Metal-Oxide Semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system. Two-stage Op-Amp is one of the most commonly used Op-Amp architectures. In this work an operational amplifier based on CMOS is presented whose input depends on its bias currents which is 20µA and designed using 180nm and 90nm technologies. In sub-threshold region due to unique behavior of the MOS transistors not only allows a designer to work at low voltages and it also allows operating at low input bias currents. Most CMOS Op-Amps are designed for specific on-chip applications and are only required to drive capacitive loads of a few pf. In this proposed work, design of a two stage fully differential CMOS operational amplifier is presented and simulations are carried out in 180nm and 90nm technologies for various parameters. The simulation is to be carried out using Cadence Virtuoso Tool.***

I. INRODUCTION

The trend towards low voltage low power silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. Op-amps are built with different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high-speed amplifications or filtering [1]-[3]. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits [4].

Op-amps are linear devices that are ideal for DC amplification and are used often in signal conditioning, filtering or other mathematical operations (add, subtract, integration and differentiation) [5].

The operational amplifier is arguably the most useful single device in analog electronic circuitry. With only a handful of external components, it can be made to perform a wide variety of analog signal processing tasks. It is also quite affordable, most general-purpose amplifiers selling for under a dollar apiece. Modern designs have been engineered with durability in mind as well: several "op-amps" are manufactured that can sustain direct short-circuits on their outputs without damage [6]-[9].

The Op Amp (Operational Amplifier) is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function. The gain produced by the op amp is higher than the gain produced by normal amplifiers. Thus, it is a high gain amplifier. The basic symbol of Op-Amp is shown in Figure1.1.1. The op amp symbol has two input terminals, one is positive terminal and other is negative terminal, voltage supplies to op amp as +VCC, –VCC and one output terminal.

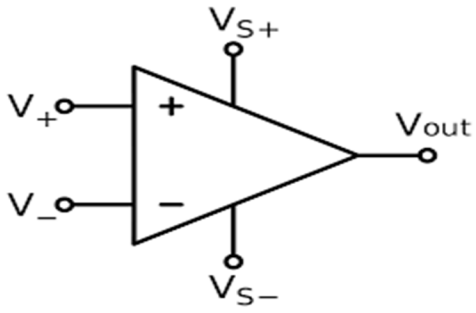


Fig .1 : Operational Amplifier

One key to the usefulness of these little circuits is in the engineering principle of feedback, particularly negative feedback, which constitutes the foundation of almost all automatic control processes [10]-[12]. The principles presented in this section, extend well beyond the immediate scope of electronics. It is well worth the electronics student's time to learn these principles and learn them well [13]. Digital comparators are divided into Total (Full) comparators and Equality comparators. Full comparators recognize three possible conditions for two n-bit binary numbers A and B, while equality comparators only indicate equality when both inputs are equal. This circuit is referred to as a *voltage follower*, and it behaves like this:

$$V_{in}=V_{out}\ V_{in}=V_{out}$$

On face, this isn't super useful. Why would I pay a few extra cents for an op-amp when it looks like a wire would do the same job between two components? The answer is simple once you know a few simple things about op-amps. When you start to break down a circuit with op-amps, two basic principles should be at the forefront of your mind:

1) The op-amp's input terminals, V+ and V-, draw no current.
2) The voltage of V+ and V- are always equal. This property is sometimes called the *virtual short approximation.*

Looking at the first rule, we can see that our voltage follower circuit is not drawing any current at the input terminal connected to V+. This is really just a way of saying that V+ has a really high impedance - in fact, since we're talking about ideal opamps, we tend to just say that it has infinite input impedance. In practice, this has some pretty neat implications: if V+ isn't drawing any current, then it means that we could connect Vin to any node in any circuit and measure it *without modifying the original circuit*. We wouldn't have to go through the tedious rigamarole of solving a bunch of new equations for node voltages and mesh currents, because we wouldn't be disturbing either of them by adding a voltage follower [14].

Instead of taking a direct measurement at Vin in our hypothetical circuit, we'd measure instead at Vout. This is the second rule of op-amps in effect - the voltages of V+ and V- are always considered to be equal. Since we've connected V- and the op-amp's output, we can extend this a step further, and say that Vout = V- = V+ due to the virtual short approximation [15] -[16].

As their name suggests, opamps are amplifiers. They can amplify signals by a certain ratio of input to output. This ratio is commonly referred to as the gain of an operational amplifier. In a perfect world, an opamp's gain would be infinite - so high that it could amplify any signal level to any other signal level. This isn't the case in the real world, but we'll consider it a fact while we analyze the next circuit: an inverting amplifier.

II. EXISTING SYSTEM

This paper presents a novel design for a two stage CMOS operational amplifier. The increasing demand for high-performance digital systems necessitates the development of comparators that can operate at elevated speeds while maintaining a compact footprint. Our proposed design achieves this by leveraging a scalable architecture tailored for CMOS Amplifier digital comparison. Through careful optimization of circuit components and efficient signal propagation, the comparator achieves remarkable speed without compromising on area efficiency.

The architecture employs advanced circuit techniques to minimize propagation delays, enabling rapid and reliable CMOS 180nm and 90nm Technology Amplifiers. Additionally, the design incorporates scalable elements, making it adaptable to various bit-width requirements. The utilization of low-power design principles enhances energy efficiency, further contributing to the overall effectiveness of Amplifiers.

Simulation results demonstrate superior performance in terms of speed and area utilization compared to existing designs. The proposed 90nm Operational Amplifier holds promise for applications in high-speed digital signal processing, Slew Rate, and other areas demanding Bandwidth and efficient digital comparisons. This work addresses the critical need for advanced Amplifiers in modern digital systems, offering a scalable solution for Operational Amplifier with a focus on both speed and area efficiency.

A CMOS two stage operational amplifier has been presented Priyanka, T., Aravind, H. S., & Hg, Y. (2017)[1], which operates at 1.8 V power supply at 0.18 micron (i.e., 180 nm) technology and whose input is depended on Bias Current. The op-amp provides a gain of 63dB and a bandwidth of 140 kHz for a load of 1 pF. This op-amp has a Common Mode gain of -25 dB, an output slew rate of 32 V /µs, and a output voltage swing. The power consumption for the op-amp is 300µW.

The high-performance two-stage operation amplifier have such advantages: a high gain, a wide output voltage amplitude, and a high common mode rejection ratio. The process of the design of CMOS op-amp proposed by, Y. Swami and S. Rai[3] ,First, adjust W and L to change the DC operation points, ensure all MOS working at saturation region, and meet the demand of the DC bias current. Then set proper input voltage (common mode input and differential mode output) to do AC simulation and transient simulation to check the gain and the phase margin of the op-amp.

Design and implementation of a two stage fully differential, RC Miller compensated CMOS operational amplifier is presented by B. Li[5], High gain enables this circuit to operate efficiently in a closed loop feedback system, whereas high bandwidth makes it suitable for high speed applications. The design is also able to address any fluctuation in supply or dc input voltages and stabilizes the operation by nullifying the effects due to perturbations. Implementation has been done in 0.18 um technology using libraries with the help of tools from Mentor Graphics and Cadence. The power dissipation for 3.3V supply voltage at 27 degrees C temperature under other nominal conditions is 2.29mW. Excellent output differential swing of 5.9V and good liner range of operation are some of the additional features of design.

III. PROPOSED SYSTEM

The proposed two stage complementary metal oxide semiconductor operational amplifier is simulated in 180nm process technology and its schematic diagram is shown in Fig. 2

Fig .2 : Design of Two-Stage CMOS Op-amp using 180nm technology

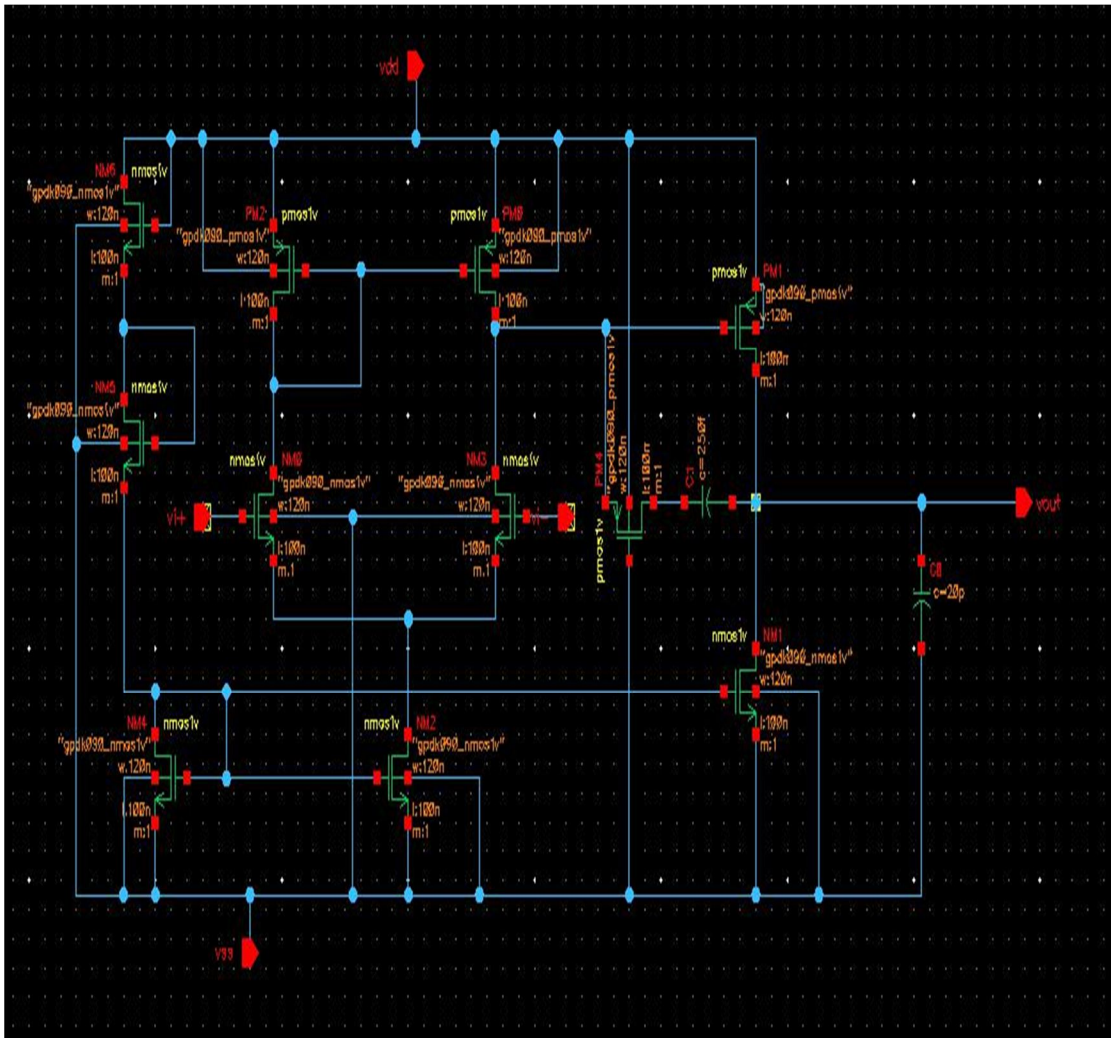


Fig.2: Schematic of two-stage CMOS operational amplifier.

IV. SIMULATION RESULTS

The important specifications considered in this design are as follows: gain-75 decibels, Phase Margin greater than or equal to 50 degrees, Slew Rate ≥ 20V/μs, Power Dissipation ≤ 2.8mW, Common Mode Rejection Ratio (CMRR) ≥ 70decibels, Output Swing ≥ ±1.5V, Offset voltage ≤ ±100mV, Gain Bandwidth product ≥ 500MHz and power supply voltage=1.8V. The transistors are assumed to be operated in saturation region. DC analysis simulation with respect to temperature variation is plotted in Fig. 3.

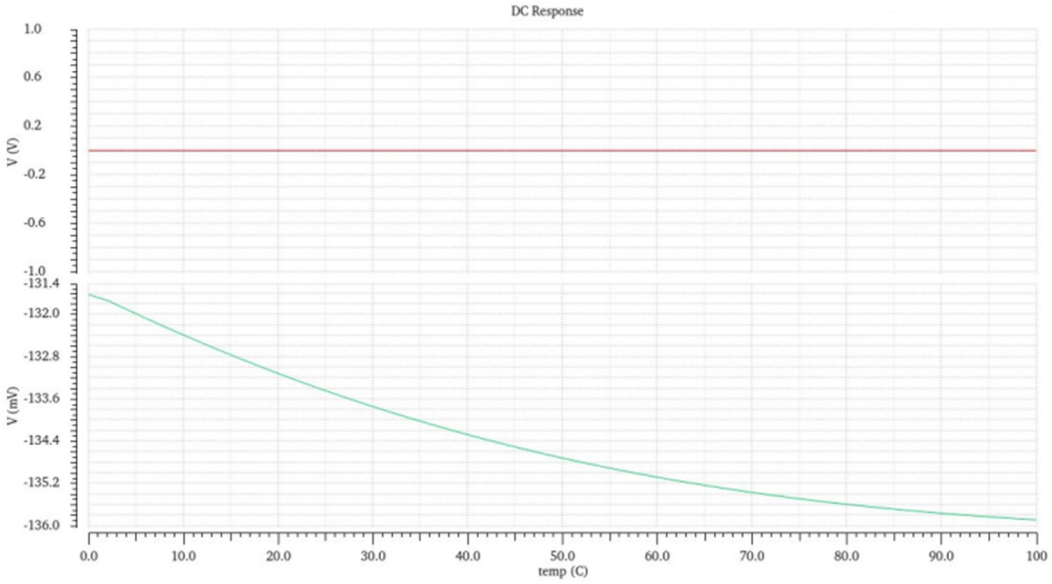


Fig. 3: DC response analysis

Transient response simulation is performed to calculate the peak to peak operating voltages and currents. A pulse width of one microsecond with a time-period of three microseconds is applied at the input terminals. Fig. 4 presents the transient analysis response.

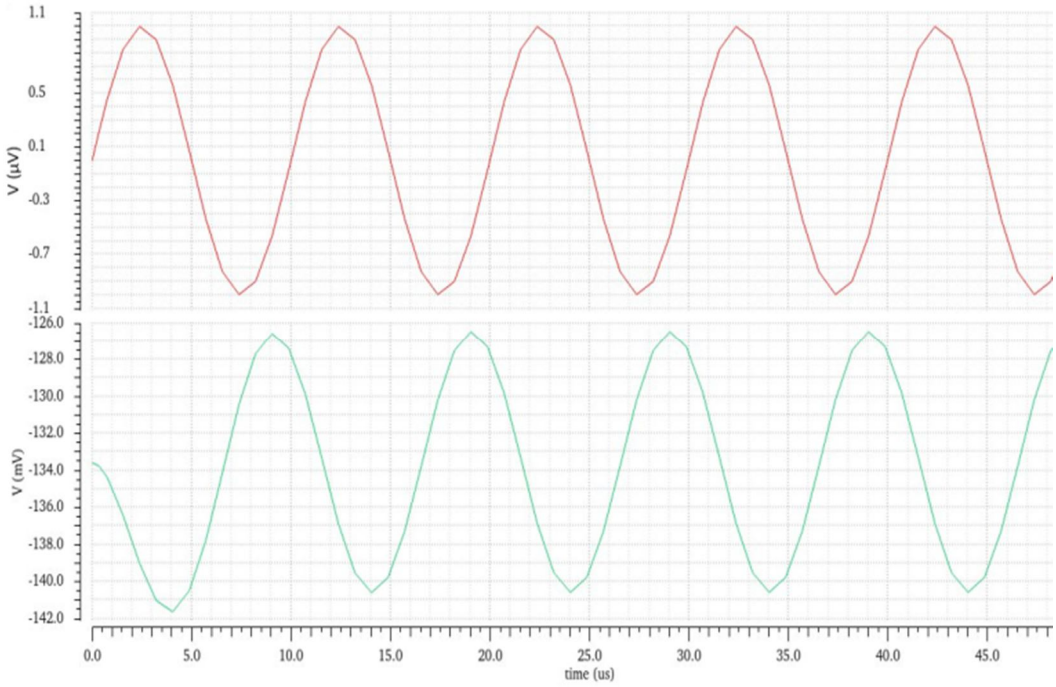


Fig. 4: Transient analysis responses

AC response analysis containing both magnitude and phase responses are performed to calculate DC gain, Phase margin and unity gain bandwidth. To carry out these calculations, an input signal of 1 microvolt of opposite phase is registered at the input side of the two-stage op-amp. The Bode plot containing both magnitude plot and phase plot versus frequency is presented in Fig. 5. A Gain of 76dB, Phase margin of 68°, and a Gain bandwidth product of 860MHz are observed from the simulated graphs.

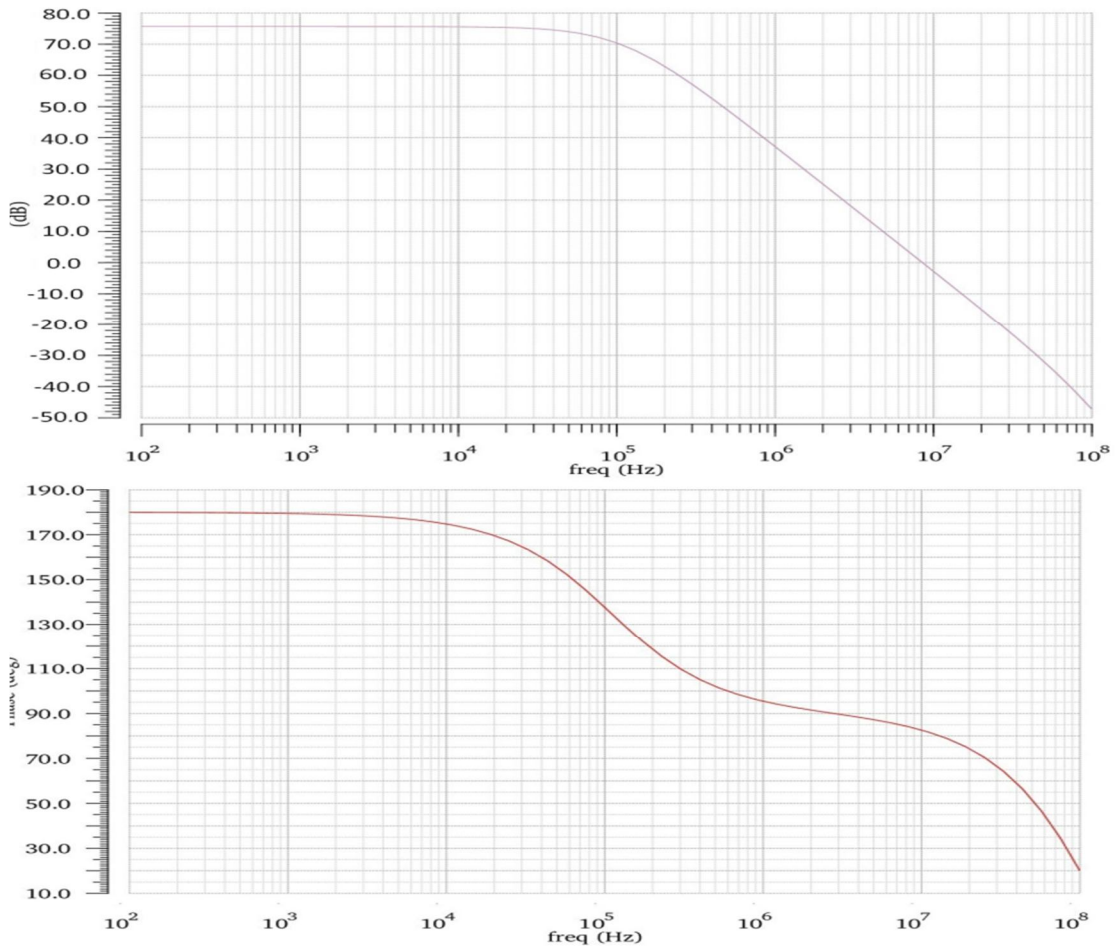


Fig.5: Magnitude plot and Phase plot

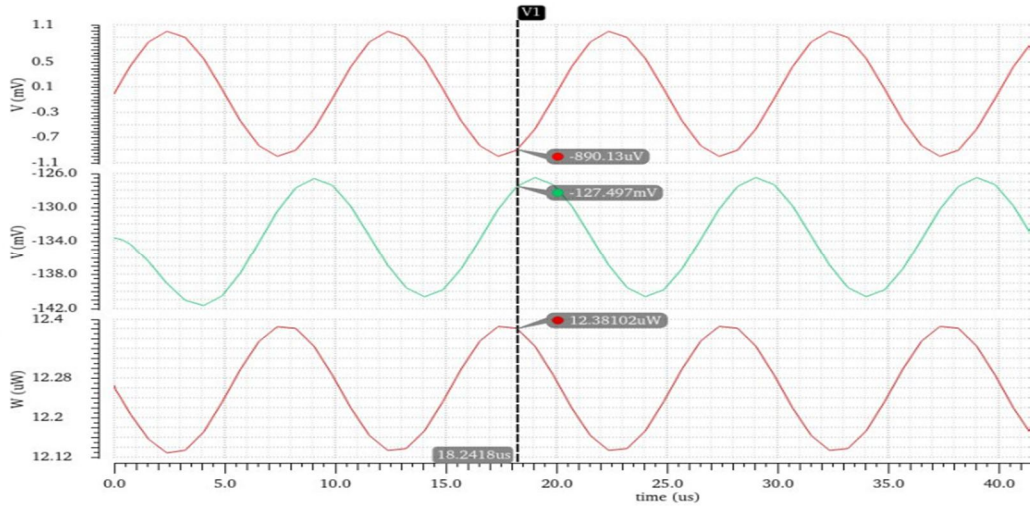


Fig.6: Simulated power response

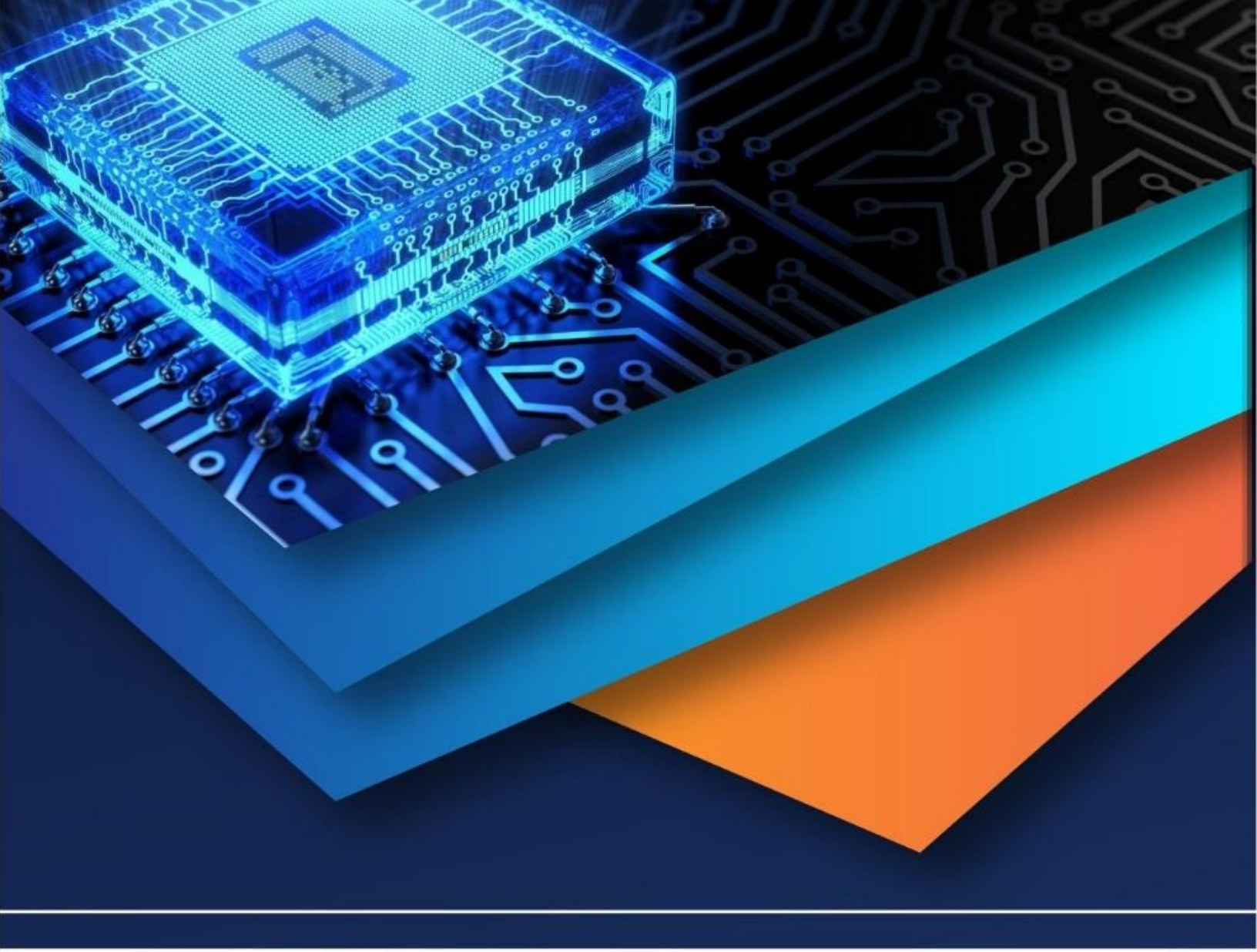
The output power calculations of the two-stage operational amplifier are presented in Fig.6. From the simulated results power dissipated at the peak output is calculated as 45.22 microwatts. Fig. 8 shows the response related to output noise and input noise in microvolt/ sqrt(Hz).

V. CONCLUSION

In this design, we have satisfied all the parameters in the requirement and specially we achieved high gain values, slew rate and wide unity gain phase margin. By comparison we found that the simulation result is a little different from out theoretical design due to some omitting during our calculation. but after all, our calculation has represent the real situation and offered great help in the design of the device. All the simulations have been carried out using cadence in 90nm CMOS process. The complete rail-to-rail output voltage swing is achieved by operating the current sourcing transistors in deep triode region. The important parameters related to CMOS two-stage operational amplifier such as direct current gain, phase margin, settling time, power dissipation, CMRR, unity gain-bandwidth and slew rate have been calculated in 90nm CMOS technology using cadence virtuoso tool and it is verified with the theoretical values. The unity gain bandwidth of the proposed two stage CMOS operational amplifier is enhanced by varying the widths of the operating transistors.

REFERENCES

[1] Priyanka, T., Aravind, H. S., & Hg, Y. (2017). Design Of Two Stage CMOS Operational Amplifier in 180nm Technology. International Research Journal of Engineering and Technology (IRJET), 4(7), 3306–3310.
[2] Yadav, V., Saxena, N., & Rajput, A. (2017). Design and Implementation of an Efficient CMOS Operational Amplifier. International Journal of Engineering Trends and Technology, 43(1), 53–57.
[3] Y. Swami and S. Rai, “Design of a CMOS Two-stage Fully Differential Operation Amplifier,” Circuits Syst., vol. 7, no. 13, pp. 4248–4279, 2016.
[4] A. M. Murshed, K. L. Krishna, M. A. Saif and K. Anuradha, "A 10-bit high speed pipelined ADC," 2018 2nd International Conference on Inventive Systems and Control (ICISC), Coimbatore, India, 2018, pp. 1253-1258
[5] B. Li, “A High DC Gain Op-Amp for Sample and Hold Circuits,” Proc. 2nd Int. Conf. Computer Science Electron. Eng. (ICCSEE 2013), vol. 9, no. Iccsee, pp. 1781–1784, 2013.
[6] A. J. Kumar, K. L. Krishna, K. A. Viswateja, K. Gopi, S. M. Rao and B. Mamatha, "A High Gain Low Power Operational Amplifier using Class AB Output Stage," 2019 3rd International Conference on Computing Methodologies and Communication (ICCMC), Erode, India, 2019, pp. 409-413,
[7] I. Aoki et. al, “Design and analysis of two stage CMOS operational amplifier using 0.13 µm technology”, JSSC, Vol. 43, No. 12, Dec. 2008, pp. 2747-2758.
[8] K. Swetha, K. L. Krishna, K. Likhitha, K. Lahari, K. Gopi and S. M. Rao, "Analysis and Simulation of Single Tail and Double Tail Circuits," 2019 4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT), Mysuru, India, 2019, pp. 269-273.
[9] P.R Gray and R.G Mayer, “ Analysis and Design of Analog Integrated Circuits”. New York: Wiley, 2001.
[10] K. Bult and G.J.G.M. Geelen, “ A fast-settling CMOS opamp for SC circuits with90-dB DC gain,” I EEE Journal of Solid-State Circuits, vol. 25, No 6, pp. 1379-1384, Dec. 1990.
[11] P.E. Allen and D.R. Holberg, “CMOS Analog Circuit Design” Oxford University Press, 2nd edition.
[12] B. Razavi, “Design of Analog CMOS Integrated Circuits,” Tata McGraw-Hill, 2002.
[13] Ankit Sharma, Parminder Singh Jassal. “Design Of A Ultra Low Power, High Precision CMOS Opamp Based Comparator For Biomedical Applications”, International Journal of Engineering Research and Applications (IJERA) , Vol. 2, Issue 3, May-Jun 2012, pp.2487-2492.
[14] Suparshya Babu Sukhavasi1, Susrutha Babu Sukhavasi1, Dr. Habibullah khan2, S R Sastry Kalavakolanu3, Vijaya Bhaskar Madivada3, Lakshmi Narayana Thalluri3, “Design of a Low Power Operational Amplifier by Compensating the Input Stage”, International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2, Mar-Apr 2012, pp.1283-1287.
[15] A.S Sedra and K. C. Smith, “Microelectronics Circuits Theory and Applications”, Fifth Edition. Oxford University Press, 2009.
[16] G. Palmisano and G. Palumbo “A very efficient CMOS low voltage output stage” , IEEE Electronic Letters 31(21). pp 1830-1831, 1995
[17] P.R Gray and R.G Mayer, “Analysis and Design of Analog Integrated Circuits”. New York: Wiley, 2001.
[18] Y. Thulasi, K. L. Krishna, D. Srinivasulu Reddy, V. Hemanthi, T. B. Reddy and T. Lalithapriya, "An Improved Miller Compensated Two Stage CMOS Operational Amplifier," 2023 Second International Conference on Electronics and Renewable Systems (ICEARS), Tuticorin, India, 2023, pp. 332-336.
[19] G. J. Kumar, K. L. Krishna, D. S. Reddy, G. L. Niharika, G. Asha and G. Neha, "Design and Implementation of an Efficient CMOS Operational Amplifier," 2022 First International Conference on Electrical, Electronics, Information and Communication Technologies (ICEEICT), Trichy, India, 2022, pp. 1-6,



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY