iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 10 **Issue:** VI **Month of publication:** June 2022

DOI: https://doi.org/10.22214/ijraset.2022.44299

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue VI June 2022- Available at www.ijraset.com

Design of CMOS Circuit Based on NAND Function at 150nm Channel Length for Low-Power and High-Speed IC Fabrication

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Abstract: ***In this paper the low-power and high-speed design approach of one Complementary Metal Oxide Semiconductor (CMOS) circuit based on NAND function has been reported. The CMOS design methodology has been followed to construct the circuit. The design has been carried out at 150 nm channel length of Metal Oxide Semiconductor (MOS) transistor. Average power consumption and gate delay of the circuit has been measured. Power-delay product (PDP) of the circuit has been calculated for optimized operation. The simulation of the circuit has been carried out with the help of Tanner SPICE (T-SPICE) software.***

Keywords: NAND Function; CMOS; Low-Power; High-Speed; PDP

I. INTRODUCTION

CMOS design technique is the simplest methodology [1-4] for integrated circuit design. In this method two blocks are used. The block which is connected between power supply voltage and output is known as pull-up network (PUN) and the block which is connected between the output node and ground is known as the pull-down network (PDN) [5-6]. Whenever, PUN is on then logic "1" is transferred to the output node and during this time some power is dissipated across PUN [3-4]. On the other hand, whenever PDN is on, logic "0" is transferred to the output node and some power is dissipated in across the PDN. This type of power dissipation is known as switching or dynamic power dissipation [7-10]. In addition to the switching power, short circuit power and leakage power dissipation are also observed in CMOS circuit [1-4]. Therefore, average power consumption is the summation of switching power, short circuit power and leakage power dissipation. Low-power & high-speed circuit design is the recent trends of Integrated Circuit fabrication [11-15] In this work, the two input CMOS NAND gate has been constructed. Context to the low power and high-speed integrated circuit fabrication, the power consumption & delay of the CMOS NAND gate has been measured and reported.

II. DESIGN OF TWO INPUT CMOS NAND FUNCTION USING SPICE

The schematic diagram of two input CMOS NAND gate is shown in Fig.1. Two NMOS transistors are connected in series in the pull-down network. Two PMOS transistors are connected in parallel in the pull-up network. To avoid the body bias effect, body terminal is connected to the source terminal. The source terminals of PMOS transistors are connected to power supply voltage (V_{DD}) and source terminal of one of the NMOS transistor is connected to ground. Two-bit sources are used for the generation of the input signal. The node "A" and "B" are considered as input terminals and node "Y" has been considered as output terminal.

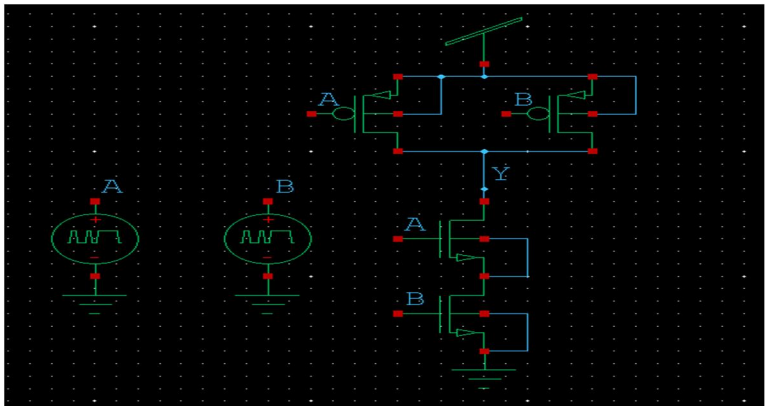

Fig.1: Schematic Diagram of Two Input CMOS NAND Gate

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III. CLARIFICATION OF FUNCTIONALITY OF CMOS NAND GATE

For the correctness of the design, the netlist of the circuit has been generated and simulated at 150 nm channel length of MOS transistor. For the clarification of the functionality of the CMOS NAND gate, the truth table of the CMOS NAND gate is shown in table1. The input and output waveforms are shown in Fig.2. As shown in Fig.2, the output is logic "High", whenever any of the input is at logic "Zero". However, when all the inputs are at logic "High" output transits to logic "Zero". The simulated waveforms as shown in Fog.2 is like the bit patterns according to the truth table of Table.1. This indicates the correct functionality of the circuit.

Table 1. Truth Table of CMOS NAND Gate

Input		Output
A	**B**	**Y**
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

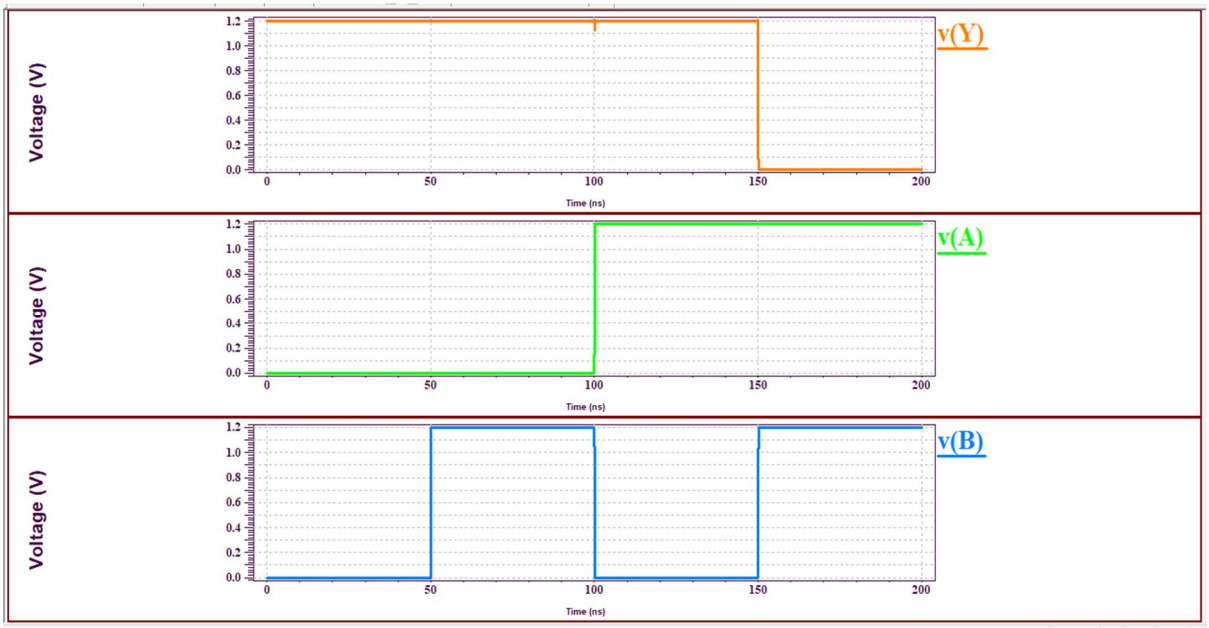

Fig. 2: Input (A, B) and Output (Y) Waveforms of CMOS NAND Gate

IV. AVERAGE POWER CONSUMPTION, SPEED AND PDP ANALYSIS OF CMOS NAND GATE AT 150 NM CHANNEL LENGTH OF MOS TRANSISTOR

The average power consumption, gate delay of the CMOS NAND gate has been measured and presented in Table 2. The Power-Delay Product (PDP) of the circuit has also been calculated and shown in Table 2. The graph related to average power consumption is shown in Fig.3. The power dissipation in the circuit increases with increasing V_{DD}. Therefore, to reduce the power consumption the V_{DD} needs to be scaled down. The graphical variation of delay is shown in Fig.4. It is found that, the gate delay decreases for the higher value of V_{DD}. Therefore, reference to Fig. 3 and 4, it is contradictory regarding the value of V_{DD} for which the performance is acceptable. To get the optimum value of V_{DD}, the PDP has been calculated. The graphical variation of PDP is shown in Fig.5. From Fig.5, it has been observed that in between 1 Volt and 1.2 Volt of V_{DD}, at 0.6 V, 0.7 V and 0.9 V PDPs are supposed to be optimum.

Table 2: Average Power Dissipation, Gate Delay and PDP of CMOS NAND Gate

V_{DD}(V)	Average Power(nW)	Gate Delay (ps)	PDP (aJ)
0.5	1.07	98.80	0.106
0.6	1.45	64.40	0.093
0.7	2.25	46.70	0.105
0.8	2.75	37.60	0.104
0.9	3.40	29.20	0.099
1	4.41	23.60	0.104
1.1	7.07	20.50	0.145
1.2	11.10	17.90	0.200

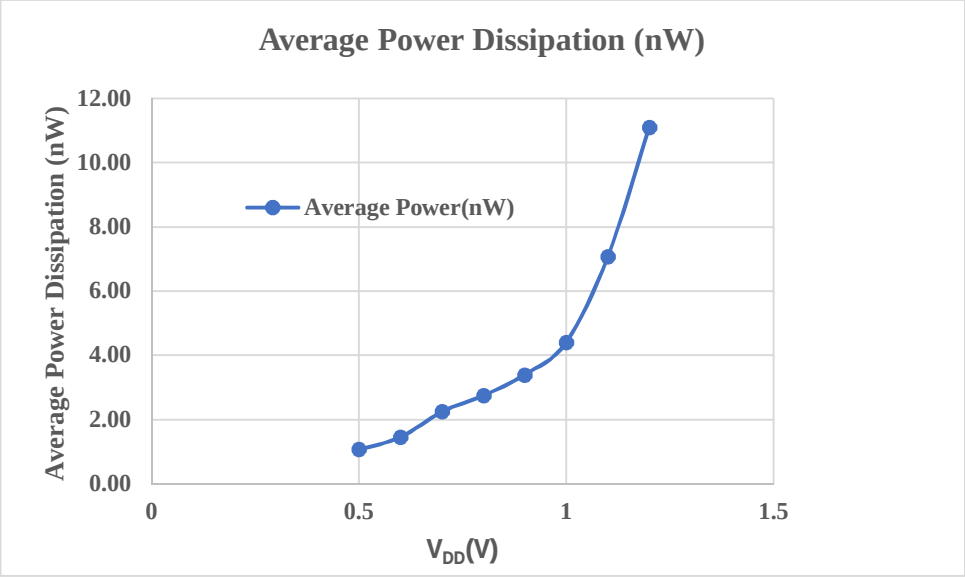

Fig. 3: Average Power Dissipation across the CMOS NAND Gate at 150 nm Channel Length

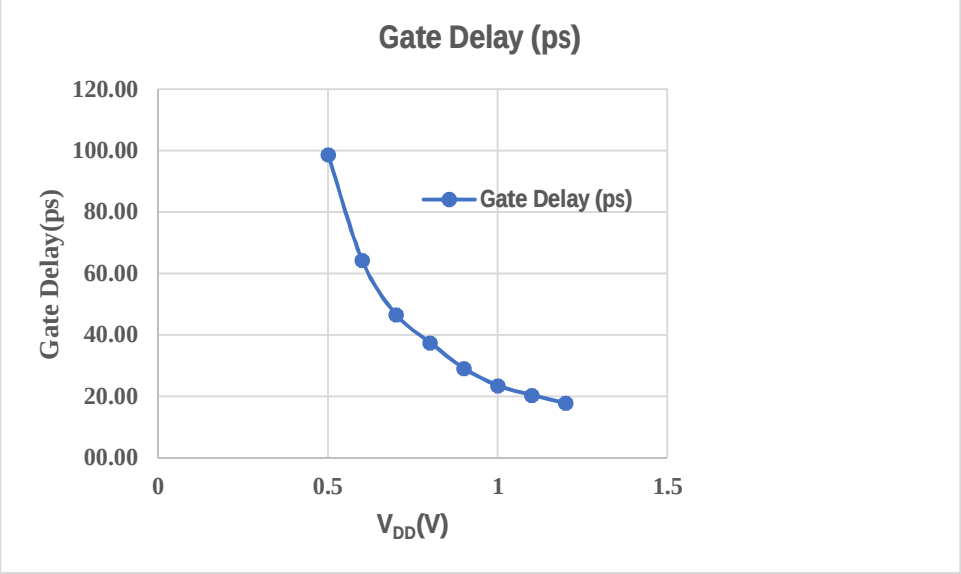

Fig. 4: Gate Delay of Two Input CMOS NAND Gate at 150 nm Channel Length

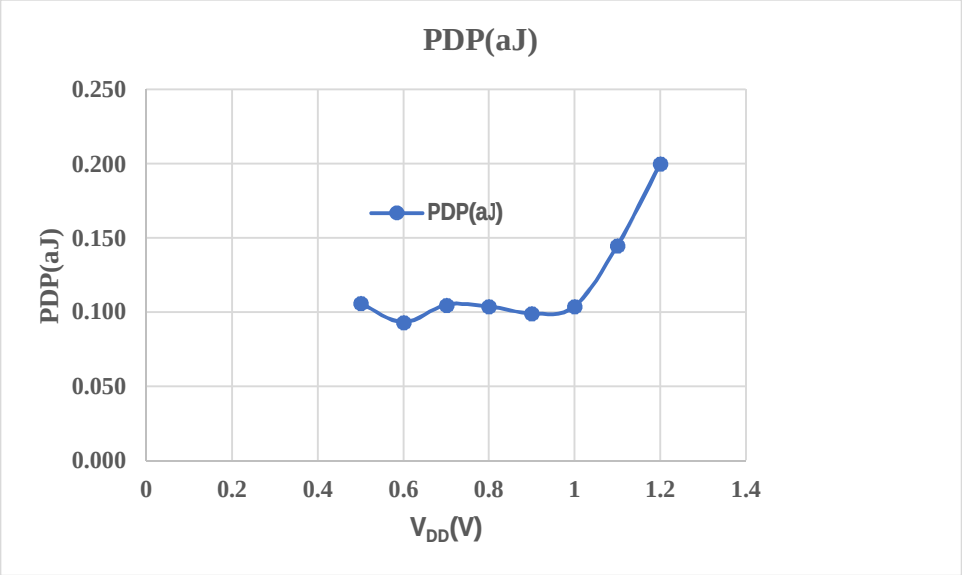

Fig.5.: Power Delay Product (PDP) Vs. V_{DD}

V. CONCLUSION

In this work, the two input CMOS NAND gate has been designed at 150 nm channel length of MOS transistor. The functionality of the circuit has been verified. Average power consumption and gate delay of the circuit has been measured and reported. Power dissipation increases with increasing V_{DD} but gate delay decreases that is speed of response increases with increasing V_{DD}.. For better operation power-delay product has been calculated and plotted. It is found that within the range of 0.5 V to 1.2 V of $V_{DD,}$ at 0.6 V ,0.7 V and 0.9 V PDP is supposed to be optimum with values 0.096 aJ, 0.105 aJ and 0.099 aJ respectively. The values of PDP, average power consumption and gate-delay are very small in this work. Therefore, results in this work are considerable for low-power and high-speed integrated circuit design and fabrication.

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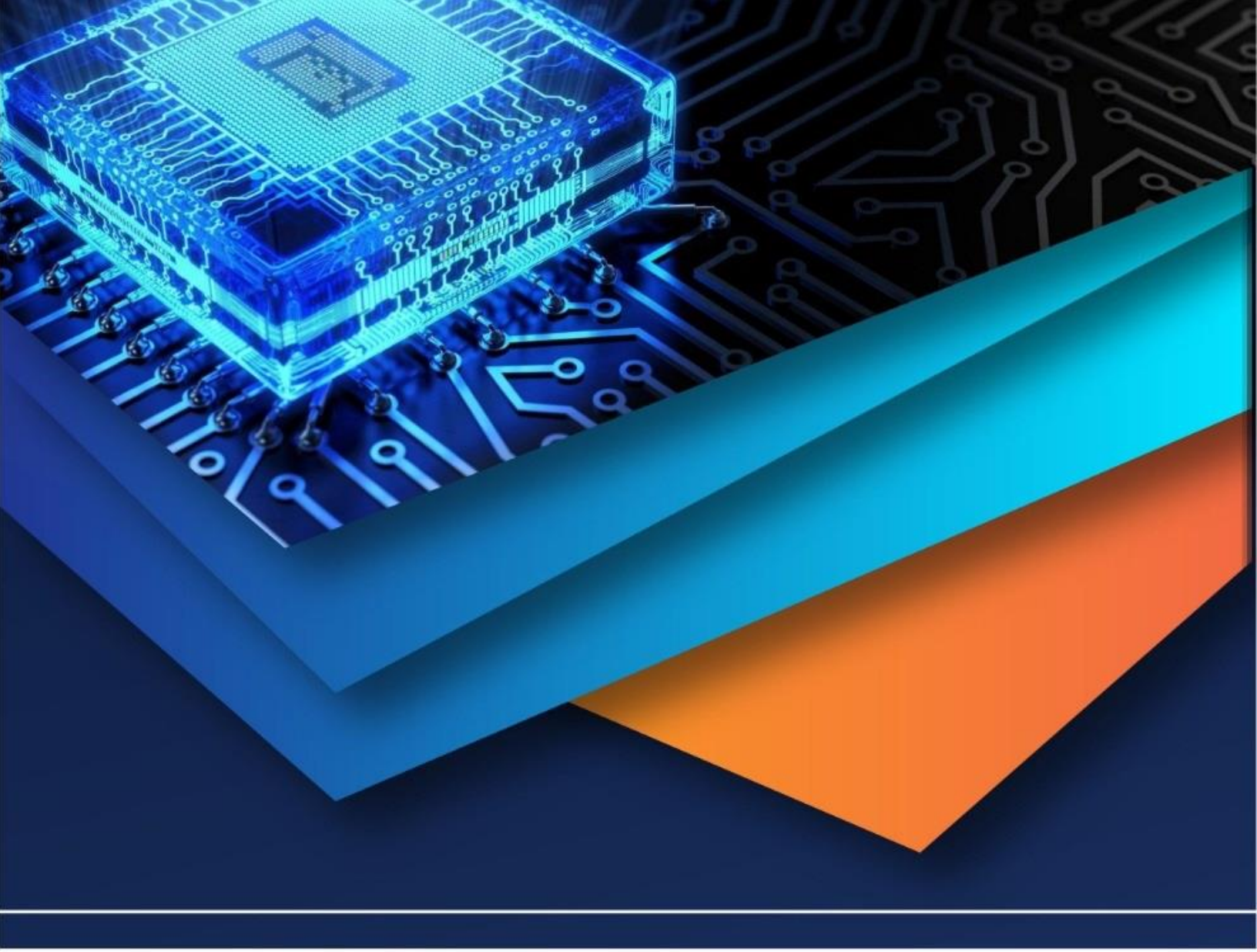

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