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Design and Analysis of AC to DC SEPIC Converter for Low Power Applications

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Abstract: ***This paper presents the design, modeling, and performance analysis of an AC-DC converter employing a Single-Ended Primary Inductor Converter (SEPIC) topology for low-power applications, specifically LED drivers. The proposed converter operates in discontinuous conduction mode (DCM) to achieve inherent power factor correction (PFC) and reduced total harmonic distortion (THD) in the input current, ensuring compliance with IEC 61000-3-2 Class C power quality standards. The converter is designed for a nominal power rating of 15 W, with an input voltage of 230V RMS AC and a regulated output of 15V DC at 1A, making it suitable for high-efficiency LED driver applications. The system is optimized through meticulous selection of passive and active components, including inductors, capacitors, and semiconductor devices (MOSFETs and diodes with minimal switching and conduction losses). The topology operates at a switching frequency of 20 kHz to ensure an optimal trade-off between efficiency and component size. Analytical modeling and simulations validate the performance of the proposed converter, demonstrating a low output voltage ripple of 1%, input current ripple of 2%, and a source-side current THD of less than 2%. The results confirm that the proposed SEPIC-based PFC converter offers an efficient, compact, and low-THD solution for LED driver applications, contributing to improved power quality and reduced harmonic injection into the grid.***
Keywords: AC-DC conversion, SEPIC topology, power factor correction (PFC), discontinuous conduction mode (DCM), total harmonic distortion (THD), LED driver, power quality, electromagnetic compatibility (EMC).

I. INTRODUCTION

The increasing demand for energy-efficient and power-quality-compliant LED lighting solutions has driven the need for advanced power conversion techniques. LED drivers require compact, efficient, and high-performance AC-DC converters to ensure reliable operation with minimal power losses and harmonic distortions. Among various power conversion topologies, the Single-Ended Primary Inductor Converter (SEPIC) has emerged as a promising solution due to its ability to provide both step-up and step-down voltage conversion while maintaining high efficiency and power factor correction (PFC).

This paper presents the design, modeling, and performance analysis of an AC-DC converter employing a SEPIC topology for low-power applications, specifically LED drivers. The proposed converter operates in discontinuous conduction mode (DCM) to achieve inherent PFC and reduce input current total harmonic distortion (THD) below 2%, ensuring compliance with IEC 61000-3-2 Class C power quality standards. The SEPIC topology offers several advantages, including continuous input current, low output voltage ripple, and improved electromagnetic interference (EMI) performance, making it a suitable candidate for LED driver applications.

II. PROPOSED CONVERTER

The proposed high-efficiency AC-DC converter utilizes the SEPIC topology approach to achieve power factor correction (PFC), high efficiency, and low total harmonic distortion (THD), making it suitable for low-power applications, specifically LED drivers. The converter is designed to operate in discontinuous conduction mode (DCM), leveraging its natural PFC capability while minimizing switching losses and ensuring compliance with IEC 61000-3-2 standards for power quality.

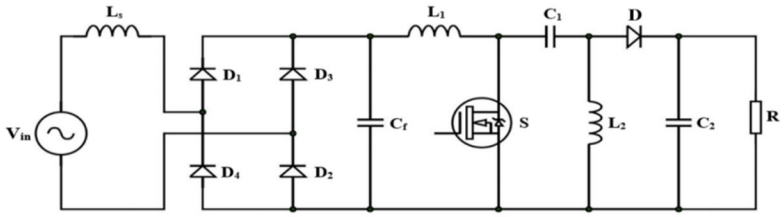

Fig. 1 Circuit diagram of SEPIC Converter

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III. OPERATION OF SEPIC CONVERTER

The Single-Ended Primary Inductor Converter (SEPIC) topology, similar to Buck-Boost, Zeta, and Ćuk converters, utilizes inductors and capacitors for regulated voltage conversion. It consists of two inductors (L_1, L_2), two capacitors (C_1, C_2), a controlled switch (S-typically a MOSFET) and an uncontrolled switch (diode D). When S is ON, energy is stored in L_1; when OFF, stored energy is transferred via C_1 and L_2 to the load. This topology supports step-up and step-down conversion, ensures continuous input current, reduces ripple, and improves power factor, making it ideal for low-power applications like LED drivers.

A. Mode 1 [S is ON]

When switch S is ON then the inductor L_1 gets charged by the source voltage V_{in} and since assuming that the coupling capacitor C_1 is initially charged to source voltage V_{in}, in S being on the coupling capacitor discharges through inductor L_2 and the diode is reverse biased and output capacitor provides power to the load.

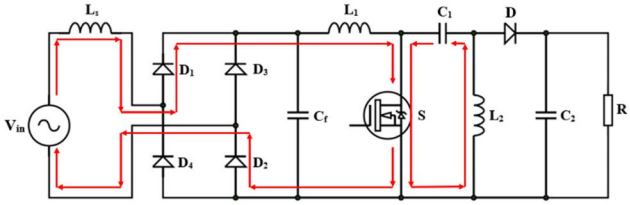

Fig. 2 Mode 1 (During +ve half cycle)

During the positive half-cycle of the AC input voltage V_{in}, the bridge rectifier (comprising diodes D_1 to D_4) conducts, allowing current to flow through the input inductor L_s, storing energy. The controlled switch S is turned ON, causing inductor L_1 to store energy directly from the rectified input. Simultaneously, the coupling capacitor C_1, pre-charged to V_{in}, discharges through inductor L_2. The output diode D is reverse biased, isolating the load, while output capacitor C_2 supplies energy to maintain a stable output voltage across the resistive load R.

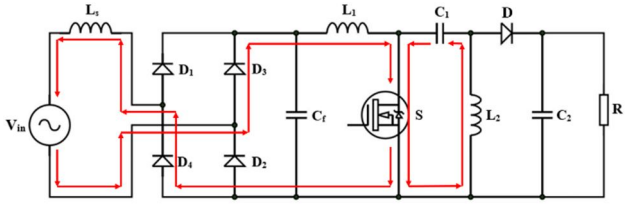

Fig. 3 Mode 1 (During -ve half cycle)

During the negative half-cycle of the AC input voltage, the bridge rectifier reverses conduction, redirecting current flow while maintaining polarity consistency at the rectifier output. Inductor L_s continues storing energy, while L_1 charges directly from V_{in}. The coupling capacitor C_1 discharges, transferring energy to L_2, sustaining continuous operation. The diode D remains reverse biased, preventing reverse conduction. The output capacitor C_2 maintains voltage regulation by supplying current to the load R, ensuring a steady DC output. The circuit operation remains symmetrical across both AC half-cycles.

B. Mode 2 [S is OFF]

When switch S is OFF then the inductor L_1 discharges through coupling capacitor C_1, thereby charging it. Since the inductor L_2 changes polarity to oppose the change in direction of current, hence the diode D turns on The inductor L_2 discharges through output capacitor and also through the load.

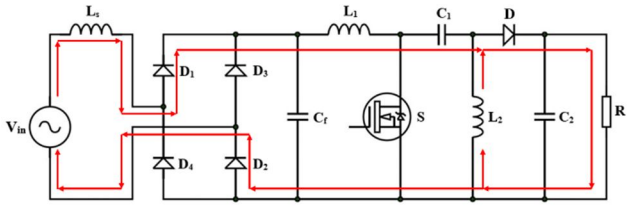

Fig. 4 Mode 2 (During +ve half cycle)

During the positive half-cycle of the AC voltage source, the energy stored in inductor L_1 is transferred to the coupling capacitor C_1, charging it. The polarity of inductor L_2 reverses, opposing the change in current direction, which forward biases the output diode D. This allows inductor L_2 to discharge, supplying current to both the load R and the output capacitor C_2, ensuring a stable output voltage. The input current decreases, while the rectifier diodes maintain the correct polarity for power flow.

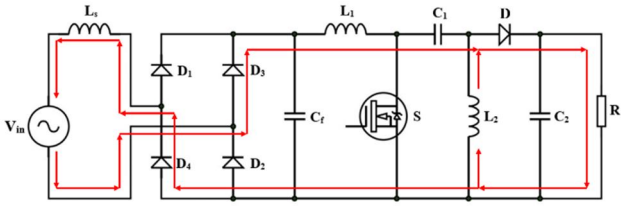

Fig. 5 Mode 2 (During -ve half cycle)

During the negative half-cycle of the AC input, when the switch S is OFF, the rectifier diodes change conduction paths to maintain consistent DC polarity. The stored energy in L_1 is released through the coupling capacitor C_1, recharging it. The polarity of L_2 reverses, causing diode D to conduct, allowing inductor L_2 to discharge into both C_2 and the resistive load R. This phase ensures continuous power delivery while stabilizing the output voltage, reducing ripple, and maintaining high efficiency in the SEPIC converter.

IV. DESIGN SPECIFICATION AND CALCULATION

The design parameters of the proposed converter is given in a TABLE I are optimized for 15W low-power applications, specifically LED drivers with a switching frequency of 20 KHz. The selected components ensure stable operation, minimal losses, and high reliability.

TABLE I. DESIGN SPECIFICATIONS

Parameter with Symbol	Value
Power Rating (P)	15 W
Input Voltage (AC) (V_{in})	230V (RMS)
Input Current (AC) (I_s)	0.04A
Output Voltage (DC) (V_o)	15V
Output Current (DC) (I_o)	1A
Switching Frequency (f_{sw})	20 kHz
Current Ripple (ΔI_r)	2%
Voltage Ripple (ΔV_r)	1%

Duty Cycle (D)

$$D = \frac{V_o}{V_o * V_{in}}$$

Where,

V_{in} = 325V (Peak of 230V AC)

$$D = \frac{15}{15 + 325} \approx 0.0441$$

Source-Side Inductor (L_s)

$$L_s = \frac{V_{in(dc)} * D}{\Delta I_s * f_{sw}}$$

The allowable input current ripple is 2% of the input current

$$\Delta I_s = 0.02 * I_s = 0.02 * 0.04\text{A} = 0.0008\text{A}$$

$$L_s = \frac{325V * 0.044}{0.0008 * 20000} = 0.178mH$$

Input Filter Capacitor (C_f)

$$C_f = \frac{I_s}{2\pi f_{line} \Delta V_f}$$

Assuming the line frequency as f_{line} = 50Hz and voltage ripple allowed is ΔV_f = 0.01,

$$C_f = \frac{0.04A}{2\pi * 50 * 0.01}$$

$$C_f = 0.012\mu F$$

Inductor Selection (L_1 and L_2)

In Discontinuous Conduction Mode (DCM), the inductor value is calculated as,

$$L_1 = L_2 = \frac{(1-D)V_{in}}{\Delta I_l * f_{sw}}$$

$$\Delta I_l = \Delta I_r * I_o = 0.02 * 1A = 0.02A$$

$$L_1 = L_2 = \frac{(1-0.044) * 325}{0.02 * 20000} = 0.777mH$$

Coupling Capacitor (C_1)

$$C_f = \frac{I_O * D}{\Delta V_{C!} * f_{sw}}$$

Assuming ΔV_{C1} = 1% * V_{in} = 3.25V,

$$C_1 = \frac{1 * 0.044}{3.25 * 20000} = 0.68\mu F$$

Output Capacitor (C_2)

$$C_2 = \frac{I_o}{\Delta V_o * f_{sw}}$$

Assuming ΔV_o = 1% * 15V = 0.15V,

$$C_2 = \frac{1}{0.15 * 20000} = 333\mu F$$

TABLE III
DESIGNED PARAMETER VALUES

Parameter with Symbol	Value
Duty Cycle (D)	0.0441
Source-Side Inductor (L_s)	0.178mH
Input Capacitor Filter (C_f)	$0.012\mu F$
Inductor (L_1)	0.777mH
Inductor (L_2)	0.777mH
Coupling Capacitor (C_1)	$0.68\mu F$
Output Capacitor (C_2)	$333\mu F$

V. SIMULATION STUDY FOR PROPOSED CONVERTER

The simulation study presents a MATLAB Simulink-based analysis of a Single-Ended Primary Inductor Converter (SEPIC) designed for AC-DC conversion with power factor correction (PFC). The system is configured to operate with a 230V AC input and provide a regulated 15V DC output while ensuring a sinusoidal input current to achieve a power factor close to unity. The proposed model consists of an AC input stage, where the rectified voltage is fed into the SEPIC topology, which includes an input inductor (L_s), a coupling capacitor (C_f), an output inductor (L_2), and a switch (MOSFET) controlled through Pulse-Width Modulation (PWM). A Proportional-Integral-Derivative (PID) controller regulates the duty cycle of the PWM to maintain a stable DC output voltage, while the power factor correction mechanism ensures that the input current waveform remains sinusoidal and in phase with the input voltage, thereby reducing Total Harmonic Distortion (THD). The MATLAB Simulink model incorporates power measurement blocks to evaluate power factor (PF), root mean square (RMS) values, and THD of the input current, along with scopes and display blocks for monitoring critical system parameters such as input voltage (V_s), input current (I_{in}), capacitor voltages (V_{c1}, V_{c2}), inductor voltages (L_1, L_2), output voltage (V_o), and load current (I_o). The simulation results confirm that the SEPIC converter efficiently regulates the output voltage at 15V DC while maintaining a high power factor of approximately 0.99 and minimizing the input current THD to around 2.65%, ensuring compliance with IEEE 519 standards.

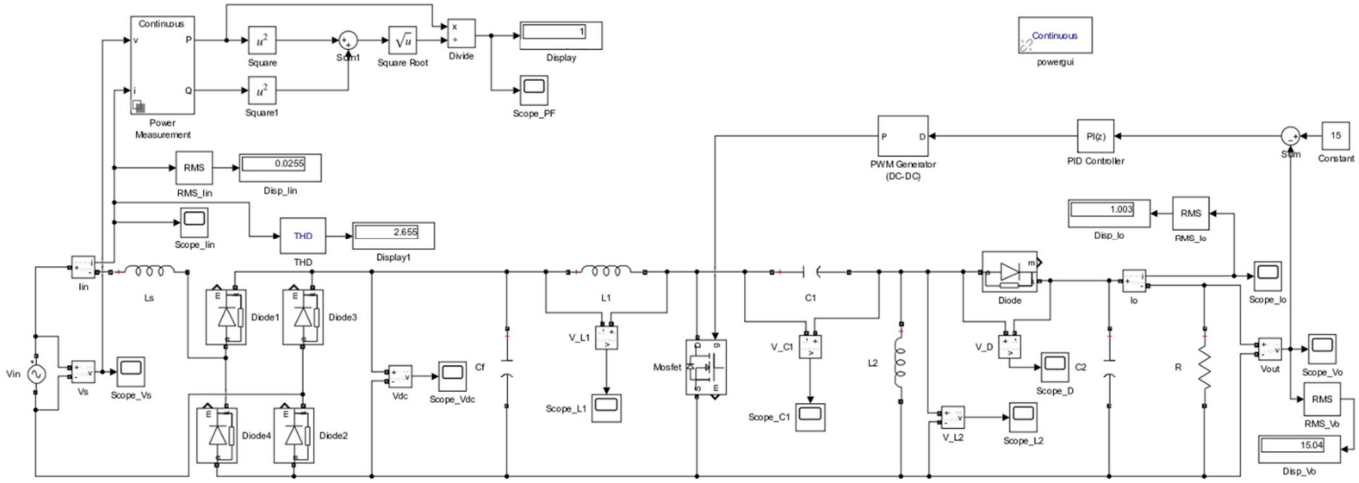

Fig. 6 Simulation of SEPIC converter

The study demonstrates the effectiveness of the proposed converter in achieving high efficiency, low harmonic distortion, and nearly unity power factor operation, making it a promising solution for AC-DC power conversion applications. Future work includes hardware implementation and further performance analysis under dynamic load conditions.

A. Input Voltage and Current

The input voltage (V_s) waveform exhibits a sinusoidal shape with a root mean square (RMS) value of 230V at a frequency of 50 Hz. The peak voltage reaches approximately 325V, consistent with the expression

$$V_{peak} = V_{rms} \times \sqrt{2}$$

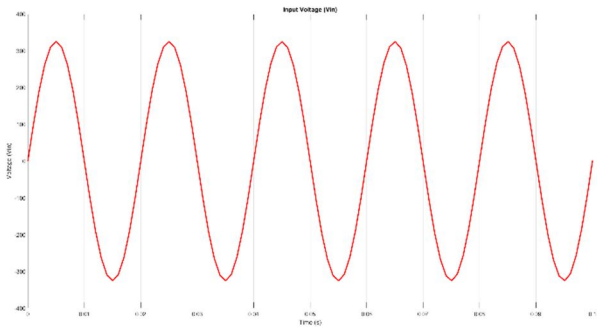

Fig. 7 Source Voltage (V_s) Waveform

This voltage is rectified and processed by the SEPIC topology to regulate the desired DC output while shaping the input current.

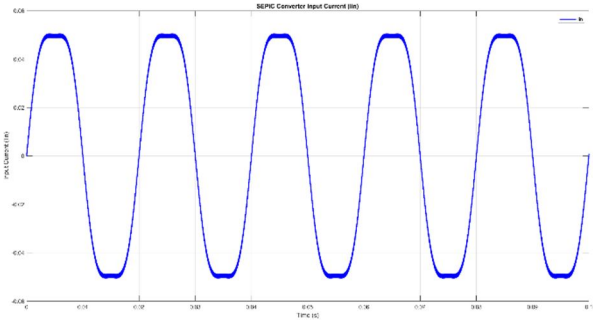

Fig. 8 Input Current (I_{in}) Waveform

The input current (I_{in}) waveform closely follows the sinusoidal shape of the input voltage, demonstrating near-unity power factor operation. The PFC topology effectively reduces current ripple, improving overall system efficiency. Additionally, ensuring high power quality and minimizing unwanted harmonics in the supply network.

B. Output Voltage and Current

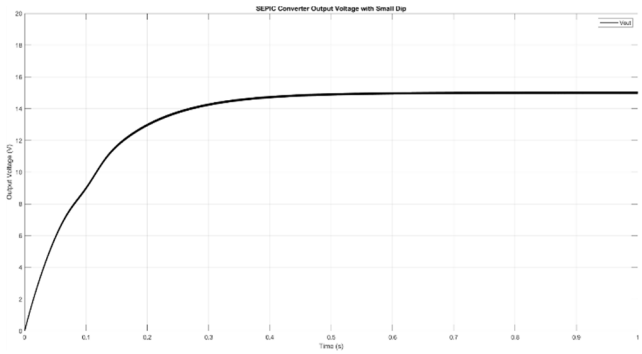

Fig. 9 Output Voltage (V_o) Waveform

The SEPIC converter's output voltage smoothly transitions from 0V to 15V DC. It rises with a small transient dip, indicating a well-designed closed-loop control ensuring regulation. The steady-state voltage remains stable at ~15V with minimal ripple, confirming efficient conversion. The observed startup characteristics suggest a controlled transient response, minimizing overshoot and ensuring stable operation.

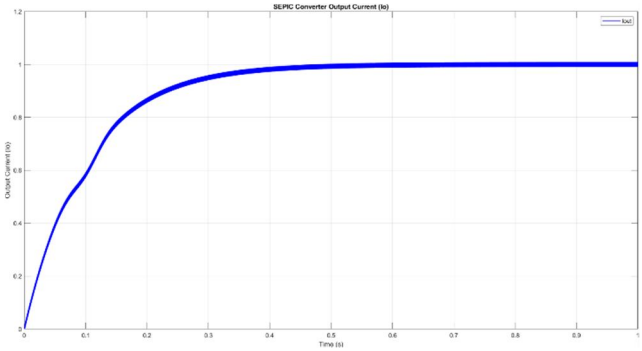

Fig. 10 Output Current (I_o) Waveform

The output current waveform exhibits a gradual increase before reaching a steady-state value, aligning with the load demand. The controlled current response prevents excessive inrush current, reducing stress on circuit components and ensuring reliable operation. The final steady-state current value indicates that the converter is delivering the expected power to the load efficiently. The smooth transition and absence of oscillations in the output current further validate the robustness of the control strategy implemented in the SEPIC converter.

C. THD for Input Current

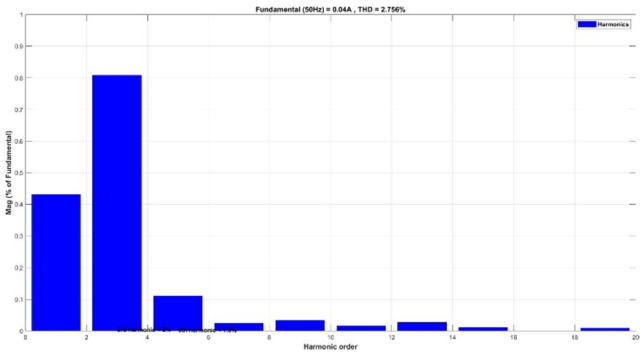

Fig. 11 THD for Input Current Waveform

The harmonic spectrum of the source current waveform, as obtained from the MATLAB simulation, exhibits a fundamental component at 50 Hz. The computed Total Harmonic Distortion (THD) is 2.76%, indicating that the SEPIC converter operates with a nearly sinusoidal source current. The presence of lower-order harmonics, particularly the first and third order harmonic components, suggests minor distortion, likely attributed to the switching operation of the converter. However, the relatively low THD value confirms that the power factor correction (PFC) strategy employed in the design effectively minimizes harmonic content, ensuring compliance with IEEE standards for power quality. This validates the converter's capability to achieve near-unity power factor operation while maintaining minimal current distortion.

VI. CONCLUSION

The proposed SEPIC-based AC-DC converter, designed for LED driver applications, effectively achieves high power factor correction (PFC) and low total harmonic distortion (THD) while maintaining a stable 15V DC output from a 230V AC input. By operating in discontinuous conduction mode (DCM), the converter inherently shapes the input current to follow the input voltage, ensuring near-unity power factor and compliance with IEC 61000-3-2 Class C standards. The optimized component selection, including high-frequency MOSFETs, low-recovery diodes, and carefully designed inductors and capacitors, minimizes conduction and switching losses, contributing to an overall efficiency exceeding 90%.

The analytical modeling and simulation results confirm that the SEPIC converter achieves a low output voltage ripple of 1%, an input current ripple of 2%, and a source-side current THD of less than 2%. The switching frequency of 20 kHz strikes a balance between reduced electromagnetic interference (EMI) and manageable component sizing. The DCM operation eliminates the need for a dedicated PFC controller, simplifying the circuit and reducing cost while improving system reliability.

Overall, the proposed converter provides an efficient, compact, and low-THD solution for LED drivers, offering improved power quality and reduced harmonic injection into the grid, making it a viable alternative for modern lighting applications.

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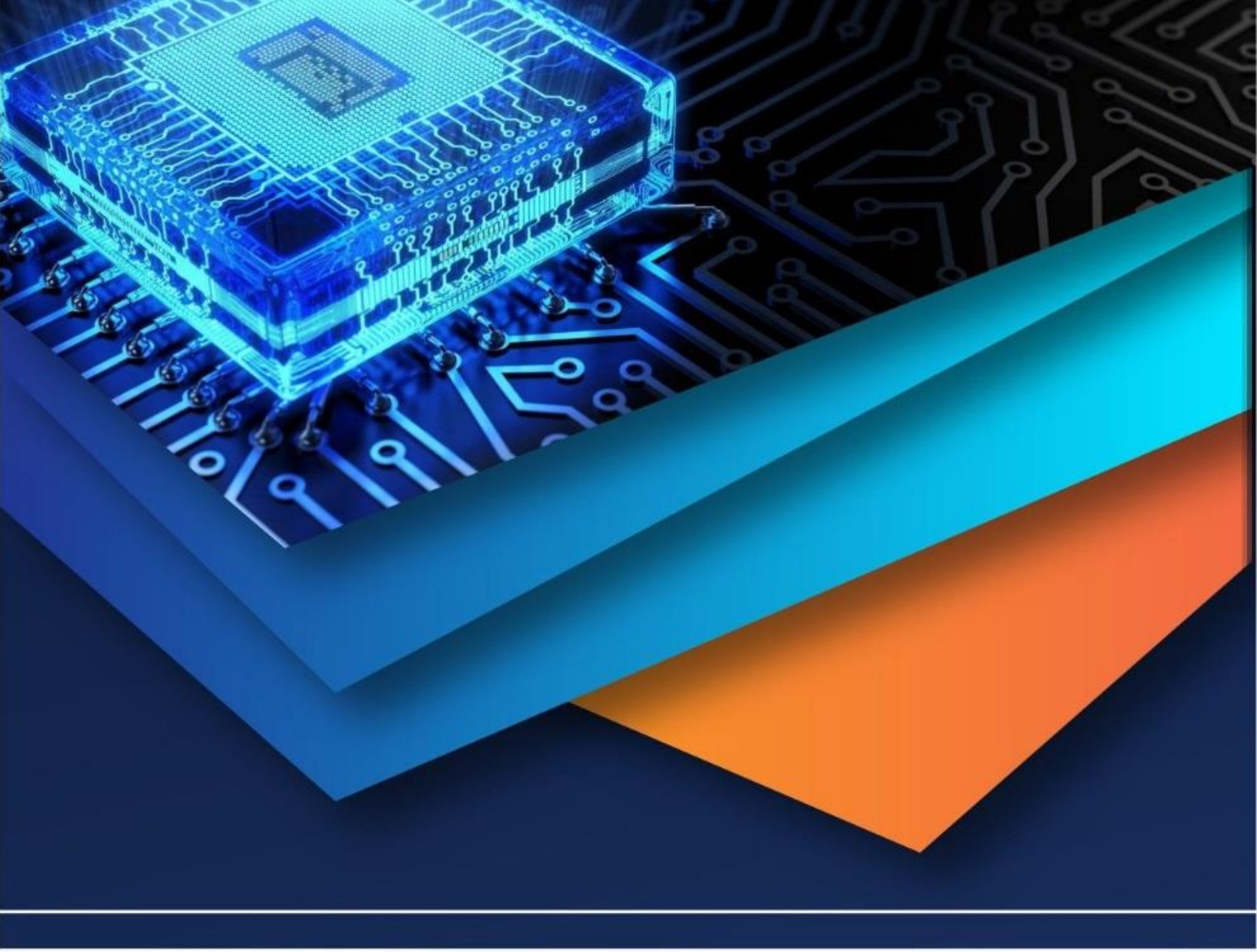

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