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Design and Implementation of Seven Segment Display Using Reversible Logic Gates

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Abstract: ***An important issue in Seven segment display is heat, but the reversible logic gives less amount of heat dissipation. So, it's an important role in nanotechnology, less energy complementary metal oxide semiconductor CMOS designs etc. Seven segment displays are most effective devices used in electronic meters, digital calculators, clock radios, digital clocks, odometers, displays in home appliances, etc.In this project, an efficient seven segment display is designed using reversible logic gates CNOT, FREDKIN and PERES gates. Retrievability is a feature which every electronic device wants to posses , In reversible logic gates the inputs and outputs can be retrievable from each other. Backward operation is used in this circuit which allows to retrieve the inputs from the outputs therefore consuming zero power. Reversible logic circuits are also known as lossless circuits, which has neither information loss nor energy loss. The reversible logic operations dissipate less heat and can't erase information.***

Keywords: Reversible logic, FREDKIN, PERES,CNOT, Retrievability, odometers, nanotechnology.

I. INTRODUCTION

Seven segment displays are most effective devices used in electronic meters, digital calculators, clock radios, digital clocks, odometers, displays in home appliances, etc. An important issue in Seven segment display is heat, but the reversible logic gives less amount of heat dissipation. So, it's an important role in nanotechnology, less energy complementary metal oxide semiconductor CMOS designs etc. Retrievability is a feature which every electronic device wants to posses , In reversible logic gates the inputs and outputs can be retrievable from each other. Backward operation is used in this circuit which allows to retrieve the inputs from the outputs therefore consuming zero power. Reversible logic circuits are also known as lossless circuits, which has neither information loss nor energy loss. The reversible logic operations dissipate zero heat and can't erase information.

II. REVERSIBLE LOGIC

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates.

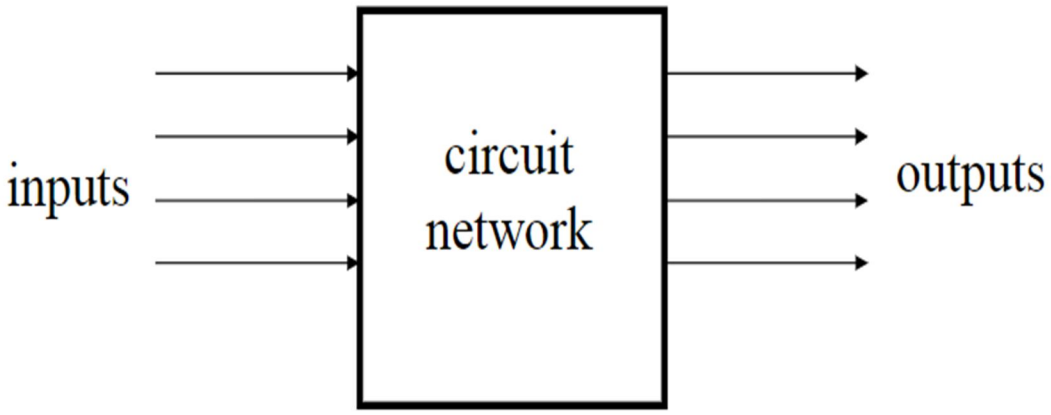

Figure.2.1 Reversible Logic

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III. IMPLEMENTATION OF THE PROJECT

A. Reversible Logic Gates

1) Peres Gate

Fig 5 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A xor B and R=AB xor C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

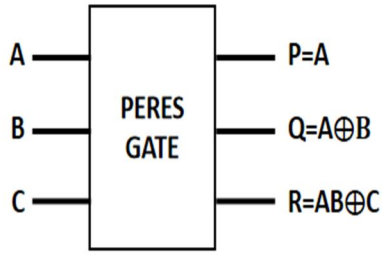

Figure.3.1 Peres Gate

2) Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B xor AC and R=A′C xor AB. Quantum cost of a Fredkin gate is 5

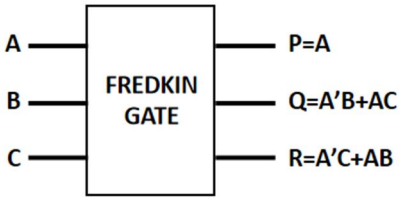

Figure.3.2 Fredkin Gate

3) NOT Gate using CNOT Gate

CNOT gate can be used to design an inverter, with one input of the CNOT gate fixed at logic 1. Any one input connected to logic 1 gives the complement of other input, as output. A=A, B=1. Quantum cost of this design of the inverter is 1. This is as shown in below figure

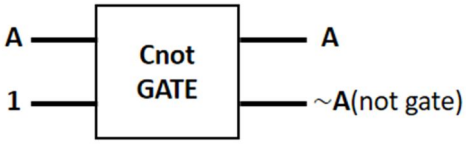

Figure.3.3 NOT Gate using CNOT Gate

4) AND Gate using PERES Gate

AND gate implementation using Peres gate, where the third input C is grounded, i.e., A=A, B=B, C=0, which gives P=A; Q = A ⊕ B; C = A AND B. Quantum cost of this proposed AND gate is 4.

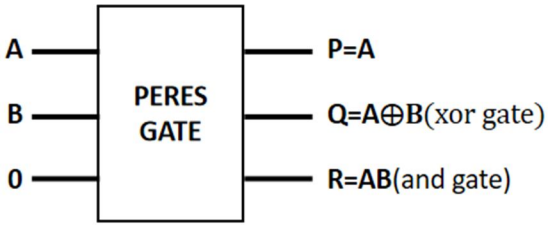

Figure.3.4 AND Gate using PERES Gate

5) OR gate using FREDKIN Gate

OR gate implementation using Fredkin gate, where the third input C is connected to logic ‘
“1” i.e., A=A, B=B, C=1 which gives P=A; Q = A + B; C = AB. Quantum cost of this proposed AND gate is 4.

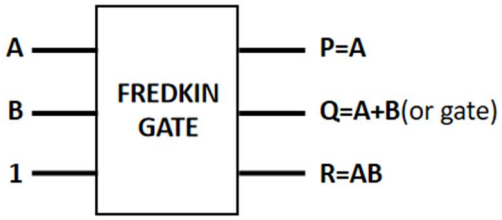

Figure.3.5 OR gate using FREDKIN Gate

6) Working of 7-Segment Display Circuit

7 LED segments of the display and their pins are “a”, “b”, “c”, “d”, “e”, “f” & “g” as shown in the figure given below. Each of the pins will illuminate the specific segment only.We assume common cathode LED segment as our example.
Suppose we want to display digit ‘0’, in order to display 0, we need to turn on “a”, “b”, “c”, “d”, “e”, “f” & turn-off the “g”, which would look like the figure given below.

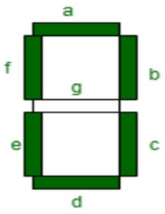

Figure.3.6 Seven Segment Display

IV. ADVANTAGES & DISADVANTAGES OF REVERSIBLE LOGIC GATES

The main advantages of Reversible gates are reduced power consumption and low latency found useful in Quantum computing. Its low power consumption and quicker operation makes them to be useful in applications Microprocessors, DSP processors and Quantum computers.The main disadvantage is high number of constant inputs is used. Hence it has scope on improvement. Improvement on following the basic rule for Reversible Gates, i.e number of inputs should equal the number of outputs is possible by optimizing the constant inputs and garbage outputs.

V. RESULT & ANALYSIS

A. RTL Schematic

The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the architecture and is used to verify the designed architecture to the ideal architecture that we are in need of development .The hdl language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e verilog. The RTL schematic even specifies the internal connection blocks for better analyzing .The figure represented below shows the RTL schematic diagram of the designed architecture.

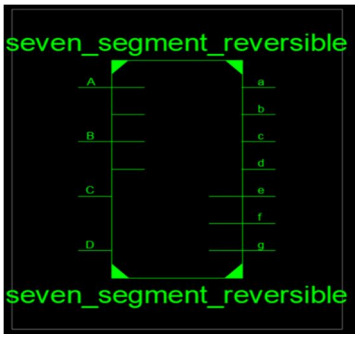

Figure.5.1 RTL Schematic

B. Technology Schematic

The technology schematic makes the representation of the architecture in the LUT format, where the LUT is consider as the parameter o area that is used in VLSI to estimate the architecture design .the LUT is consider as an square-unit the memory allocation of the code is represented in there LUTs in FPGA .

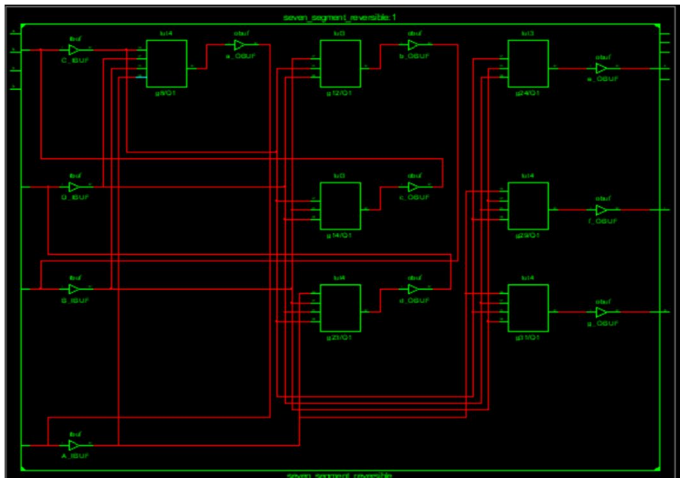

Figure.5.2 Technology Schematic

C. Simulation

The simulation is the process which is termed as the final verification in respect to its working whereas the schematic is the verification of the connections and blocks. The simulation window is launched as shifting from implantation to the simulation on the home screen of the tool ,and the simulation window confines the output in the form of the wave forms. Here it has the flexibility of providing the different radix number systems.

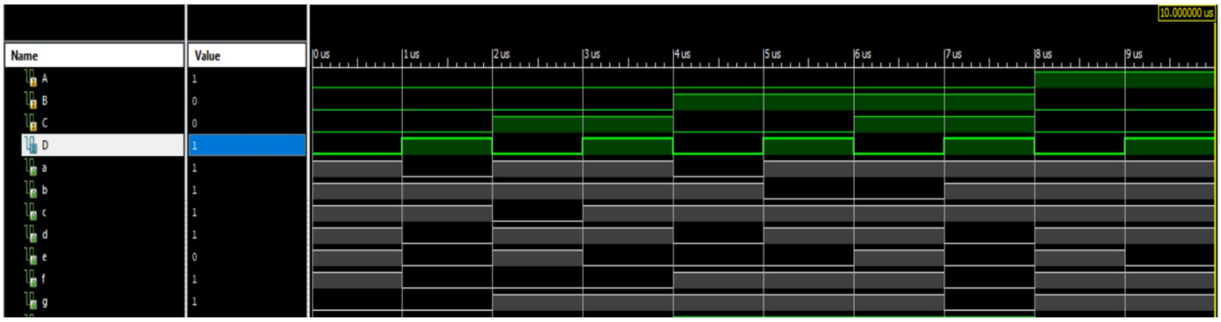

Figure.5.3 Simulated Waveforms

VI. CONCLUSION

The main design parameter that VLSI engineers need to bother when designing with the integrated circuits is energy loss and information loss. This project has presented the design methodologies of a compact seven segment display using reversible logic gates. The proposed design efficiency has been proved with simulation analysis. By comparative analysis the proposed circuit has been constructed with low quantum cost, optimum number of gates, less power and garbage values. As the better than the other circuits this seven segment display using reversible gates has zero amount of heat dissipation and zero amount of information loss that means neither information loss nor energy loss. As the circuit performance is better than the other circuits this type circuits can be used in many electronic applications.

VII. ACKNOWLEDGMENT

We hereby express our sincere gratitude to the HOD of Electronics and Communication Engineering, Prof. G. Srikanth for providing us seamless knowledge and support over past one year and for providing right suggestions at every phase for successful completion of project. We express our sincere gratitude to our guide Assoc. Prof. SK. DILSHAD, Department of Electronics and Communication Engineering, for her constant guidance and for providing required guidance as internal guide for result-oriented implementation of ideas relevant to my project.

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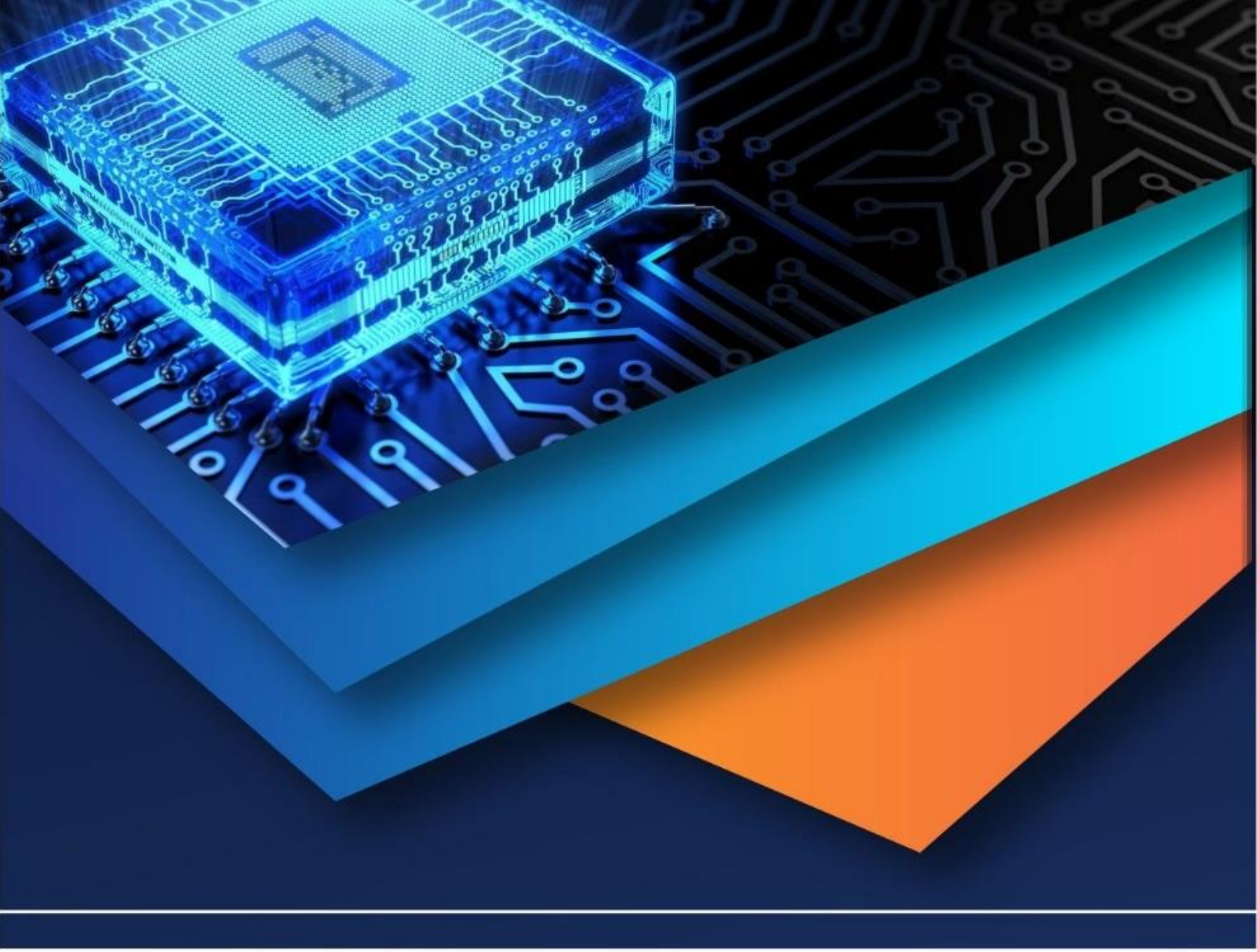

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