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Design and VLSI Implementation of Vedic Multiplier using 45nm Technology

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Abstract: ***This paper proposes low-power multiplier architectures based on Vedic mathematics, which is a set of ancient Indian techniques for performing arithmetic operations. The proposed architectures use the Urdhva-Tiryagbhyam sutra from Vedic mathematics, which enables the efficient multiplication of numbers with fewer partial products. The proposed architectures have been implemented and simulated using the 45-nm CMOS technology. The simulation results demonstrate that the proposed architectures achieve significant power savings compared to conventional multipliers while maintaining reasonable area and delay. Therefore, the proposed architectures are suitable for use in low-power and high-performance applications. The Vedic multiplier consists of several sub-modules, each of which performs a specific function in the multiplication process. These sub-modules include the partial product generator, the multiplier, and the adder. The partial product generator generates partial products based on the input numbers and the Vedic sutras. The multiplier module then combines these partial products to create the final product. Finally, the adder module adds the product to the previous state of the circuit to generate the final result.***
Index Terms: Urdhva-Tiryagbhyam, CMOS,Vedic multiplier;

I. INTRODUCTION

The Vedic multiplier is a novel approach to multiplication that is based on ancient Indian mathematics. It offers a faster and more efficient way to perform multiplication operations than traditional methods, making it an attractive option for a range of applications in digital signal processing, cryptography, and other areas.In this context, designing and implementing a Vedic multiplier using advanced semiconductor manufacturing technologies, such as 45nm technology, can offer several advantages, including higher performance, reduced power consumption, and smaller chip area.The design and VLSI implementation of a Vedic multiplier using 45nm technology involves creating a circuit that can perform multiplication operations using Vedic sutras in a digital environment. This requires a detailed understanding of the mathematical principles underlying the Vedic sutras and their implementation in a hardware circuit.The Vedic multiplier circuit typically consists of several sub-modules, including a partial product generator, a multiplier, and an adder. The partial product generator generates partial products based on the input numbers and the Vedic sutras. The multiplier module then combines these partial products to create the final product. Finally, the adder module adds the product to the previous state of the circuit to generate the final result. Optimization tools can then be used to improve the design for performance, power, and area. Once the design is finalized, it can be fabricated on a chip using 45nm technology, which involves using advanced lithography techniques to create high-density circuits on a small chip area.Overall, the design and VLSI implementation of a Vedic multiplier using 45nm technology offers a highly efficient and high-performance solution for multiplication operations in digital systems. The use of advanced semiconductor manufacturing technologies enables the creation of highly optimized and compact circuits that can deliver high-speed performance while minimizing power consumption and chip area.
The design and VLSI implementation of a Vedic multiplier using 45nm technology involves creating a digital circuit that can perform fast and efficient multiplication using the principles of ancient Indian mathematics. In this process, the design is optimized to work with 45nm technology, which is a semiconductor manufacturing process that allows for the creation of small and efficient electronic circuits.The Vedic multiplier is based on the Vedic sutras, which are a set of principles that were used in ancient Indian mathematics for fast and efficient arithmetic. The Vedic multiplier consists of several sub-modules, including the partial product generator, the multiplier, and the adder. Each of these modules performs a specific function in the multiplication process, and the design must be optimized to work with 45nm technology.The VLSI implementation of the Vedic multiplier involves using a hardware description language, such as Verilog or VHDL, to model the circuit. This model is then optimized for the 45nm technology using software tools that simulate the circuit's behavior and optimize it for speed and area.The final design is then fabricated on a chip using 45nm semiconductor manufacturing processes. This process involves creating a mask that is used to transfer the design onto a silicon wafer.

The wafer is then processed in a series of steps that involve etching, doping, and other techniques to create the circuit's components.The resulting circuit is a Vedic multiplier that is optimized for 45nm technology and can perform fast and efficient multiplication using the principles of ancient Indian mathematics. It has applications in many areas of digital signal processing, including image and video processing, as well as in cryptography and other security applications. The use of 45nm technology allows for the creation of small and efficient circuits that can be used in a variety of electronic devices.

II. THEORETICAL BACKGROUND

Many researchers have suggested Vedic multiplier using various many technologies.A brief review of some important contributions of the existing technologies are represented below:

Suryasnata Tripathy, published Low Power Multiplier Architectures Using Vedic Mathematics in 45nm Technology for High Speed Computing. The paper presents low power multiplier architectures based on Vedic mathematics to achieve high-speed computing. The proposed 4-bit and 8-bit multiplier topologies use the Urdhva Tiryakbhyam sutra of Vedic mathematics and are implemented using 45nm CMOS process technology in Cadence EDA tool. The design uses a 5T AND gate based on pass transistor logic and transmission gate logic to generate partial products, instead of the conventional 6T CMOS based design. The adder chains in the multiplier units are composed of 14T full adders and 9T half adders optimized for low power and high-speed arithmetic. The use of these modified topologies results in a smaller silicon area requirement. Additionally, the overall delay associated with the proposed architectures is reduced, as the number of transistors in the critical path is fewer due to the new adder topologies. The proposed designs' performance analysis is carried out for both schematic and layout stages, with a voltage supply of 1V. Overall, this study introduces new multiplier architectures that utilize Vedic mathematics and low power design techniques to achieve high-speed computing while reducing silicon area and overall delay[1].

Sushma R. Huddar and Sudhir Rao, published Novel High Speed Vedic Mathematics Multiplier using Compressors. This paper presents a new architecture that utilizes ancient Vedic mathematics techniques to achieve high-speed multiplication. The architecture also incorporates new 4:2 compressors and novel 7:2 compressors for addition, which contribute to its high speed. The paper compares this compressor-based multiplier to other popular multiplication methods and finds that it is nearly two times faster, with only a 1% reduction in area. The experiments were conducted on a Xilinx Spartan 3e FPGA, and the design's timing and area on the FPGA were calculated. Overall, this study introduces a new approach to multiplication that is faster than conventional methods and demonstrates its feasibility through experimentation on an FPGA. [2].

Lee Shing Jie et al ,proposes a 2x2 bit Vedic multiplier with different adders in 90nm CMOS technology.The paper presents a 2x2 bit Vedic multiplier designed using three different adder circuits in 90nm CMOS technology. The three adder circuits are composed of two half adders utilizing a 3T XOR gate, two full adders using a 6T XOR gate, and two hybrid full adders with 13 transistors. These adders are combined with four AND gates to create a multiplier module for executing a Vedic mathematics algorithm. The algorithm reduces the number of partial products compared to conventional multiplication, making it faster. The performance parameters of power consumption, delay, and output swing were evaluated using Synopsys Custom Tools and GPDK of 90nm CMOS technology. The results showed that the 2x2 Vedic multiplier with the 13T HFA adder had the best performance, with a full output voltage swing and the second lowest power consumption of 22.96 µW and a delay of 47.70 ps. Overall, this study successfully demonstrates a new combination of multiplier method using hybrid full adders and Vedic mathematics that achieves low power and low delay [3].

G.Challa et al proposes VLSI Architecture for delay efficient 32-bit Multiplier using Vedic Mathematic sutras. This paper presents a VLSI architecture for both the Urdhva-Tiryagbhyam and Nikhilam sutras, which are implemented and synthesized using Xilinx software. The results show that the Urdhva-Tiryagbhyam multiplier has less delay and memory usage compared to the Nikhilam multiplier. Additionally, the paper proposes modifications to the Vedic multiplier structure, including the use of a Binary to excess-1 code converter, to further reduce the delay of the multiplier. The paper suggests that the delay and memory consumption of a multiplier are largely dependent on the adders used for the summation of partial products. By using modified adders with less delay and memory, the total delay and memory consumption of the multiplier can be reduced. The performance of a multiplier is typically determined by the time taken to perform the multiplication process, and hence, multipliers with less delay are preferred [4].

Rishi Yadav et al. proposes Implementation of 4X4 Fast Vedic Multiplier using GDI Method The paper focuses on the design of a Vedic multiplier, which is based on the ancient mathematics discovered by Shri Bhartiya Krishna Tirtha Maharaja. The Urdhva Tiryagbhyam method is used for multiplication, which involves a combination of vertical and crosswise operations. This technique relies on the simultaneous addition of partial products to complete the overall calculation. The goal of this design is to reduce power consumption. To achieve this, the Vedic multiplier technique is employed.

A 4x4 multiplier is implemented using both CMOS and GDI logic, with the latter resulting in less delay. The key components of the multiplier design are the half adders and full adders [5].

III. DESIGN AND IMPLEMENTATION

A. 2x2 Vedic Multiplier

The Vedic multiplier (VM) module for 2x2 multiplication is designed using two half adders and four 2-input AND gates. The module takes two 2-bit numbers, A and B, where A is represented as ala0 and B as b1b0.The multiplication starts by multiplying the least significant bits (LSBs) of the two numbers, which gives the LSB of the final product (vertical multiplication). Then, the LSB of the multiplicand (a0) is multiplied with the next higher bit of the multiplier (b1), and the product of the LSB of the multiplier (b0) is multiplied with the next higher bit of the multiplicand (al). These two products are added together (crosswise multiplication), and the resulting sum gives the second bit of the final product. The carry obtained from this addition is added with the partial product obtained by multiplying the most significant bits (al and b1), to give the sum and carry. The sum is the third corresponding bit, and the carry becomes the fourth bit of the final product. Fig.1 shows the architecture of the proposed 2x2 Vedic Multiplier [5].

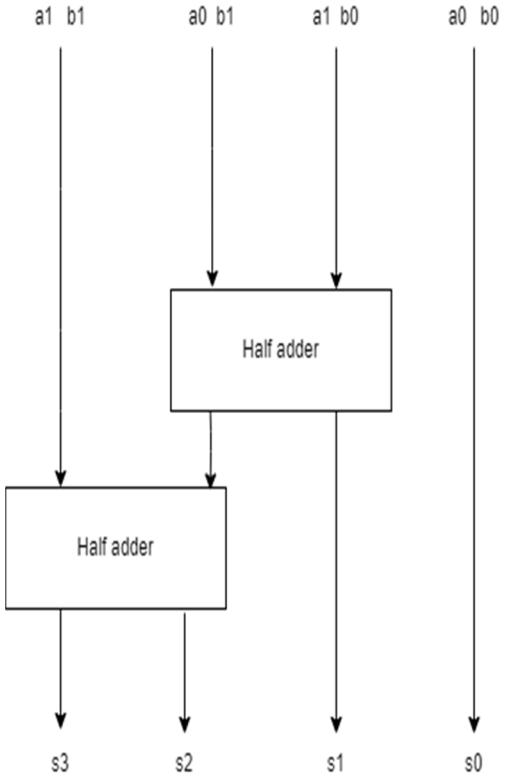

Figure 1: Architecture of the proposed 2x2 Vedic Multiplier [5]

B. 4x4 Vedic Multiplier

To implement a 4x4 multiplier, we use four 2x2 Vedic multiplier blocks, a ripple carry adder, and a half adder. The output of each 2x2 block is fed into the ripple carry adder, while the half adder handles the carry. Let's assume we have two 4-bit numbers A and B, where A is represented as a3a2a1a0 and B as b3b2b1b0.The multiplication process is shown in the block design figure below, and the final product is represented as s7s6s5s4s3s2s1s0. The partial products are calculated in parallel, which significantly reduces the delay compared to serial multiplication. The least significant bit (s0) is obtained by multiplying the LSBs of the multiplier and the multiplicand. The 4x4 Vedic Multiplier schematic, as shown in Figure 3.11, uses four 2x2 Vedic multiplier blocks, a ripple carry adder, and a half adder to efficiently multiply two 4-bit numbers. The module uses parallel computation of partial products to reduce delay, and the least significant bit is obtained through vertical multiplication of the LSBs. The final product is obtained through the addition of all the partial products using the ripple carry adder and half adder. Fig.1 shows the architecture of the proposed 4x4 Vedic Multiplier [1].

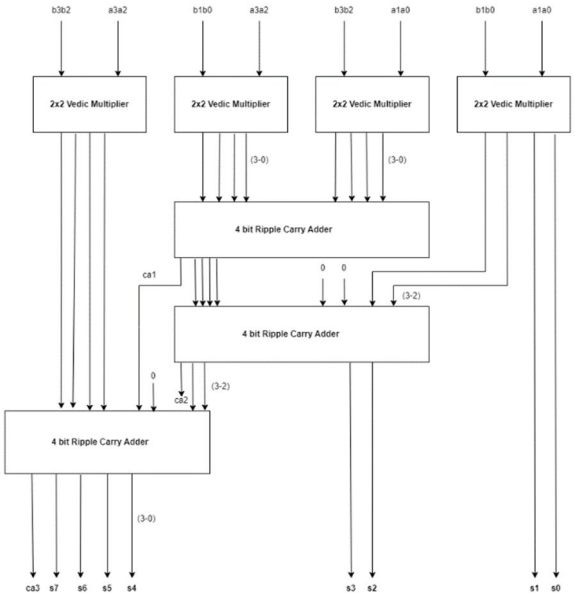

Figure 2: Architecture of the proposed 4x4 Vedic Multiplier [1]

C. Half adder

A half adder is an arithmetic circuit that performs binary addition of two input bits (A and B) and produces two output bits: a sum bit (SUM) and a carry bit (CARRY). The SUM bit is obtained by performing an exclusive OR (XOR) operation on the input bits A and B, while the CARRY bit is obtained by performing an AND operation on the same input bits.To implement a half adder, only one XOR gate and one AND gate are required, making it a simple combinational circuit. However, it can only add two input bits and cannot consider any carry input bit. This means that if there is any carry input, it will be ignored and the half adder will only perform the addition of the two input bits A and B. Therefore, it is called a half adder as it performs only a part of the binary addition process.

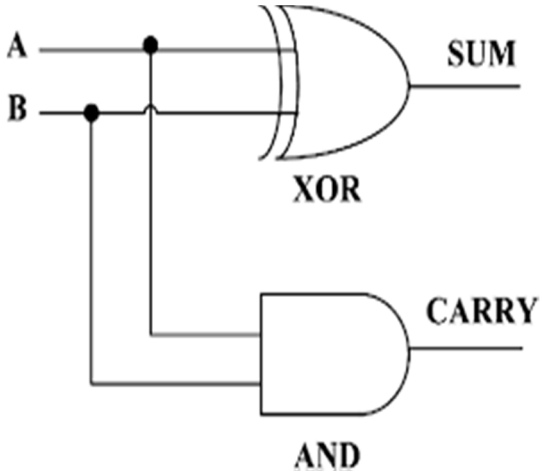

Figure 3: Half adder

D. Full adder

A full-adder circuit has three inputs, namely A, B, and Cin, and two outputs, namely S and Cout. The SUM output is obtained by performing an exclusive OR operation on the three input bits A, B, and Cin. The COUT output is generated if any two out of the three input bits are HIGH. The equations for computing S and Cout for a full adder are: SUM = A XOR B XOR Cin, and Cout = (A AND B) OR (B AND Cin) OR (A AND Cin).

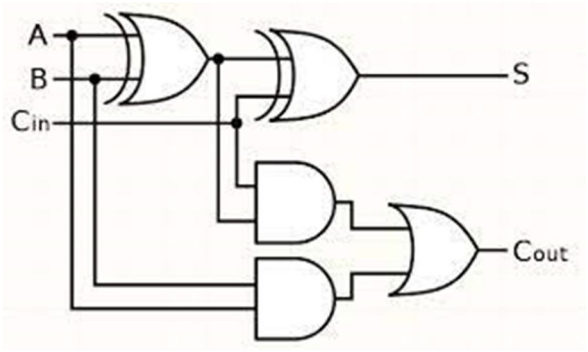

Figure 4: Full adder

IV. PERFORMANCE ANALYSIS

A. Comparision Half Adder And Full Adder

Table.1 shows comparision of half adder and full adder .The propagation delay of a full adder is generally longer than that of a half adder. This is because a full adder is a more complex circuit than a half adder, as it has an additional input carry bit.A full adder requires more transistors and logic gates than a half adder, which leads to longer propagation delay. In a full adder, the carry output is generated by adding three input bits, while in a half adder, the carry output is not considered.Moreover, a full adder requires more input transitions than a half adder to generate the output, which adds to the overall delay. The extra logic required in a full adder to generate the carry output makes it slower compared to the half adder.

Topology	Propagation Delay
Half adder	25.19×10^{-12}sec
Full adder	44.75×10^{-12}sec

V. CONCLUSION

The objective of this project was to implement a high-performance 4-bit Vedic multiplier using 45nm technology in Cadence Analog environment. The multiplier takes digital inputs and provides digital outputs, and consists of digital circuits such as basic gates and various adders. In conventional designs, readily available digital components like basic gates are used in semi-custom designs, however, this approach may not yield optimal design parameters. Thus, this project employs a full-custom design approach that utilizes an analog platform, where design parameters are determined at the transistor level. It can be inferred that using Vedic multipliers in 45nm technology results in reduced power consumption and increased multiplication speed.

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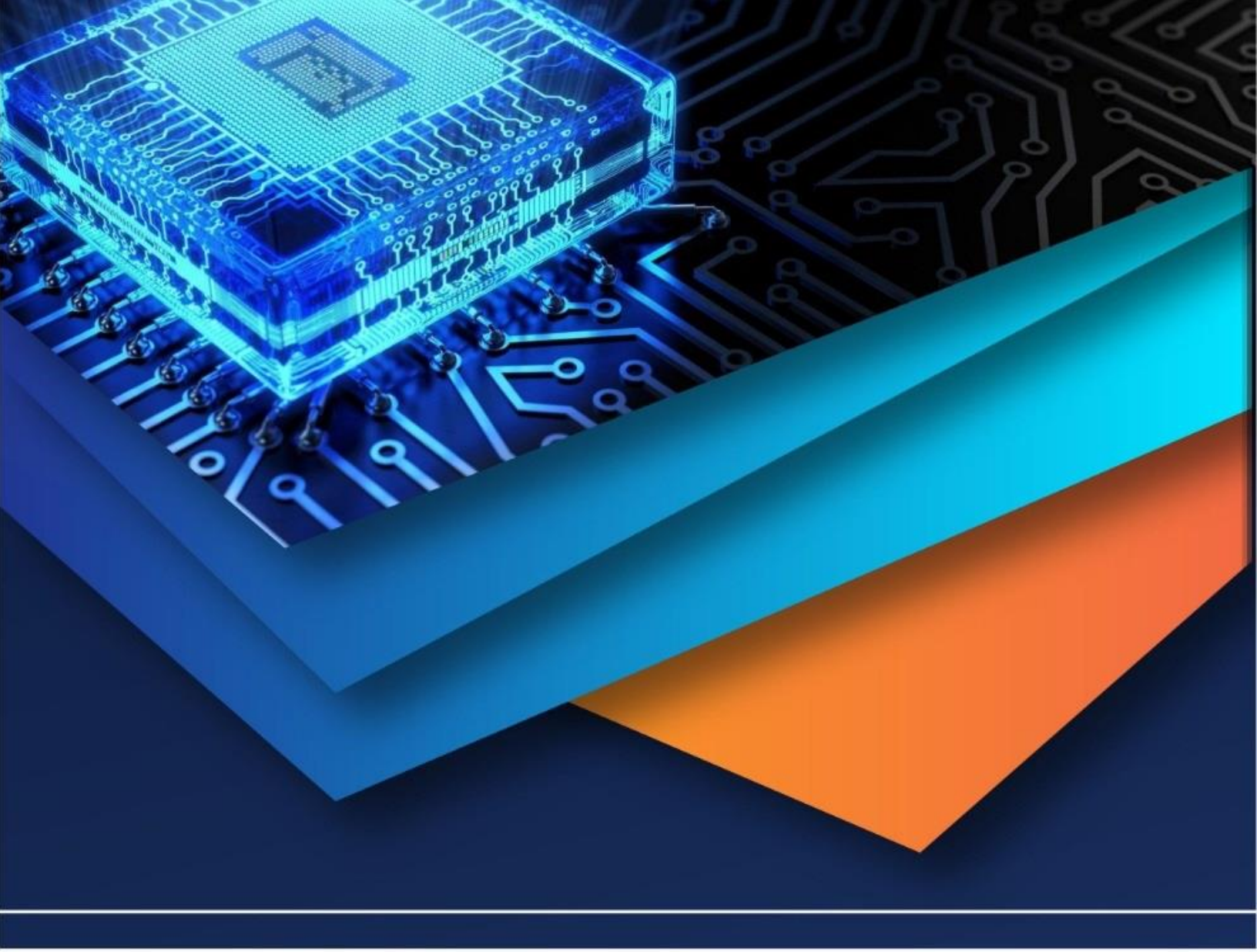

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