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Design of a High Efficiency AC-DC Converter with Interleaved Zeta Topology for Electric Vehicle off Board Chargers

R. Thangasankaran[1], Dr. S. Parthasarathy[2], K. Karthick Raja[3], P. Guru Bathrinath[4], S. Jeeva[5]
[1]*AP/EEE,* [2]*Prof/EEE,* [3, 4, 5]*UG Scholar/EEE, K. L. N. College of Engineering, Sivaganga, India*

Abstract: ***This paper presents the design and analysis of a high-efficiency AC-DC converter based on the Zeta topology for electric vehicle (EV) off-board charging applications. The proposed converter operates in discontinuous conduction mode (DCM) to achieve inherent power factor correction (PFC) and reduced total harmonic distortion (THD) in the input current, ensuring compliance with power quality standards. The converter is designed for a power rating of 1 kW, with an input voltage of 230V AC and an output of 60V DC at 16.67A, making it suitable for EV battery charging. The system employs an interleaved approach to enhance efficiency and minimize current ripple. Simulation and analytical results validate the effectiveness of the proposed topology, demonstrating low voltage and current ripple (1% and 2%, respectively) and achieving a source-side current THD of less than 2%. The proposed converter provides an efficient and reliable solution for EV off-board charging, contributing to the advancement of sustainable transportation infrastructure.***

Keywords: AC-DC converter, Zeta topology, power factor correction (PFC), electric vehicle (EV) charger, discontinuous conduction mode (DCM), interleaved converter, total harmonic distortion (THD)

I. INTRODUCTION

The growing adoption of electric vehicles (EVs) has driven the demand for efficient, compact, and high-performance battery charging solutions. Off-board chargers, which provide fast and reliable charging. The Zeta converter has emerged as a promising solution due to its ability to provide both step-up and step-down voltage conversion while maintaining high efficiency and power quality. This paper presents the design and analysis of a high-efficiency AC-DC converter with Zeta topology for EV off-board charging applications. The proposed converter operates in discontinuous conduction mode (DCM) to achieve inherent power factor correction (PFC) and reduce input current total harmonic distortion (THD) below 2%, ensuring compliance with IEC 61000-3-2 power quality standards. The Zeta converter topology offers several advantages, including continuous input current, low output voltage ripple, and making it a suitable candidate for high-power charging applications.

II. PROPOSED CONVERTER

The proposed high-efficiency AC-DC converter utilizes the Zeta topology with an interleaved approach to achieve power factor correction (PFC), high efficiency, and low total harmonic distortion (THD), making it suitable for electric vehicle (EV) off-board charging applications. The converter is designed to operate in discontinuous conduction mode (DCM), leveraging its natural PFC capability while minimizing switching losses and ensuring compliance with IEC 61000-3-2 standards for power quality.

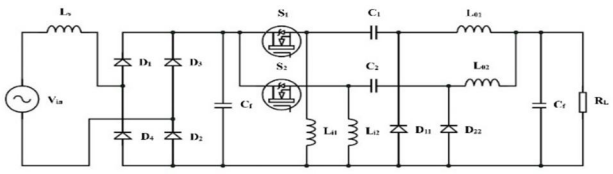


Fig. 1. Circuit diagram of Interleaved Zeta Converter

A. Operating Principle

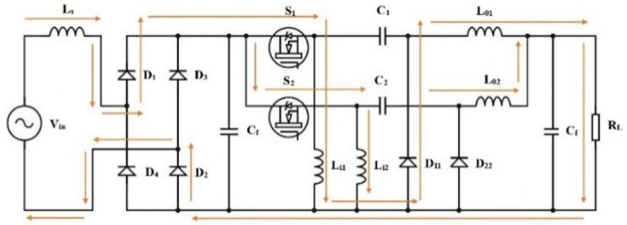
The Zeta converter topology, a fourth-order DC-DC converter, consists of two inductors, two capacitors, a switch (MOSFET), and a diode. Unlike traditional boost and buck-boost converters, the Zeta converter provides non-inverting output voltage, making it particularly suitable for applications requiring both step-up and step-down voltage conversion.

The interleaved structure further enhances performance by reducing current ripple and improving thermal distribution across components. In the proposed interleaved Zeta converter as shown in fig.1, two Zeta converter modules operate in parallel, phase-shifted by 180° to balance the input current, thereby reducing overall ripple and EMI emissions. The operation can be divided into two modes based on the state of the switching MOSFET's.

To simplify the analysis of the circuit, all the components used in the circuit are assumed to be ideal. The input inductor L_{i1} is operated in CCM mode and the output inductor L_{o1} is operated in DCM mode. The inductors specifications are chosen to operated in such a way. Fig. 2 illustrated four modes of operation for different switching period for one complete cycle.

Mode 1 [$t_0 \leq t \leq t_1$]

During Mode 1, switch S_1 is turned on and at the same time S_2 is in off condition. The inductor L_{i1} & capacitor C_1 is storing energy from the DC supply V_{dc}. The inductor L_{o1} is releasing its stored energy to the load through the output DC link capacitor C_o. The inductor L_{o1} and C_o are resonating during this mode.



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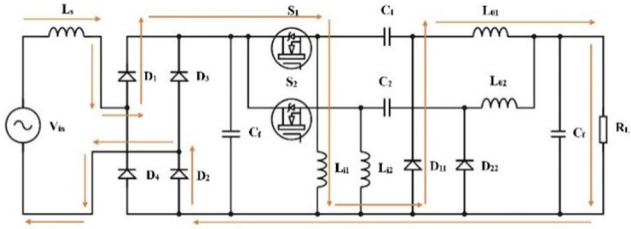

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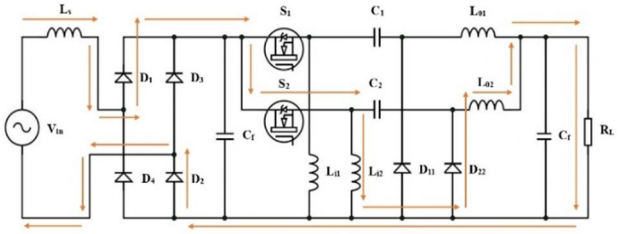

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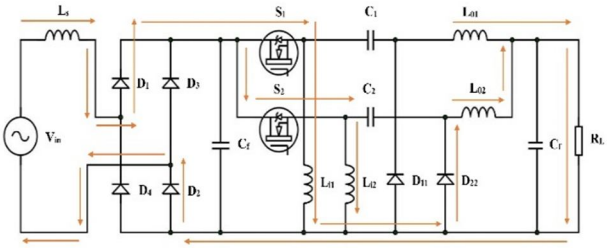


(d)

Fig. 2. Different Modes of Operation (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4

Mode 2 [t1 ≤ t ≤ t2]:
During Mode 2, switches S_1 and S_2 both are turned ON. The inductor L_{o1} is dissipating energy to the load through output capacitor Co. The inductor L_{i2} & C_2 starts charging from the DC supply through the switch S_2. End of this mode the inductors L_{i1} completely charged L_{o1} starts discharging.

Mode 3 [t2 ≤ t ≤ t3]:
In Mode 3 the switch S_2 is kept on condition, and S_1 turned off. The inductor L_{i2} & C_2 is continuously charging until the switch is on. The inductors L_{i1}, L_{o1} starts discharging to the load through DC link capacitor. End of this mode, L_{o1} completely discharged charging in reverse direction and there is minimum current circulating through the output capacitor and load.

Mode 4 [t3 ≤ t ≤ t4]:
Switches S_1 and S_2 both are turned ON. The inductors L_{i2}, L_{o2} starts discharging to the load through the DC link capacitor. The inductors L_{i1}, L_{o1} & capacitor C_1 is storing energy from the DC supply V_{dc} through the switch S_1. End of this mode the L_{i2}, L_{o2} inductors completely discharged and the cycle repeats.

B. Design Specification and Calculation
The design parameters of the proposed converter is given in a table.1 are optimized for 1 kW EV charging applications with a switching frequency of 20 kHz. The selected components ensure stable operation, minimal losses, and high reliability.

Table. 1. Design Specification

Parameter with Symbol	Value
Power Rating (P)	1 kW
Input Voltage (AC) (V_{in})	230V (RMS)
Input Current (AC) (I_s)	4.35A
Output Voltage (DC) (V_o)	60V
Output Current (DC) (I_o)	16.67A
Switching Frequency (f_{sw})	20 kHz
Current Ripple (ΔI_r)	2%
Voltage Ripple (ΔV_r)	1%

Duty Cycle (D) Calculation

$$D = \frac{V_o}{V_o * V_{in}}$$

Where,
V_{in} = 325V (Peak of 230V AC)

$$D = \frac{60}{60 + 325} \approx 0.1846$$

Input Inductor (L_i) Calculation

$$L_i = \frac{(V_{in}(max))^2}{2Pf_{sw}}$$

$$L_i = \frac{(325)^2}{2 * 1000 * 20000} = 2.64\text{mH}$$

$$L_{i1} = L_{i2} = \frac{2.64}{2} = 1.32\text{mH}$$

Output Inductor (L_o) Calculation

$$L_o = \frac{V_o(1-D)^2}{2f_{sw}I_o}$$

Where,
(1-D) = 1-0.1846 = 0.8154

$$L_o = \frac{60(0.8154)^2}{2 * 20000 * 16.67} = 95.6\mu H$$

$$L_{01} = L_{02} = \frac{95.6}{2} = 47.8\mu H$$

Intermediate Capacitors (C_1,C_2) Calculation

$$C = \frac{I_{in} D}{f_{sw} \Delta V_r}$$

Where,
ΔV_r = 1% of 325V = 3.25V

$$C = \frac{4.35 * 0.1846}{20000 * 3.25} = 12.36\mu H$$

$C_1 = C_2 = 12.35\mu H$
Output Capacitor (C_o) Calculation

$$C_o = \frac{I_o * D}{f_{sw} * \Delta V_r}$$

Where,

$$\Delta V_r = 1\% \text{ of } 60V = 0.6V$$

$$C_o = \frac{16.67 * 0.1846}{20000 * 0.6} = 2.57mF$$

$C_f = 0.1 * C_o$
$C_f = 0.1 * 2.7mF = 270\mu H$
Load Resistance (R_L) Calculation

$$R = \frac{V_o}{I_o}$$

$$R = \frac{60}{16.67} = 3.6\Omega$$

The proposed high-efficiency AC-DC Zeta converter is designed for 1 kW EV charging applications, ensuring high power factor, low THD, and minimal ripple. The interleaved structure enhances efficiency while the DCM operation simplifies control and reduces switching losses. The selected components ensure reliable operation under rated conditions.

III. SIMULATION STUDY OF THE PROPOSED CONVERTER

The interleaved Zeta converter helps to improve the efficiency and reduce ripples in the output voltage. In order to achieve the constant output voltage the closed loop simulation has been done as shown in fig.3 for the Interleaved Zeta converter to ensure to achieve the desired output voltage. PI controller has been used to accomplish the closed loop simulation of the Interleaved Zeta converter.

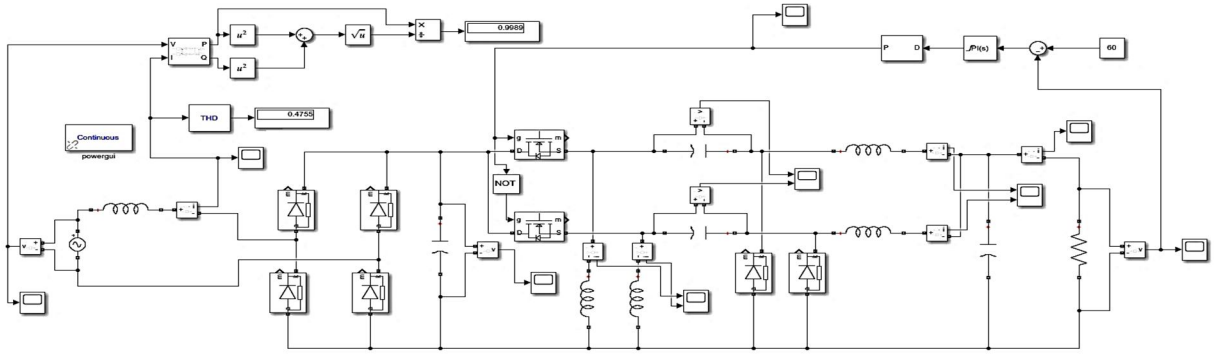
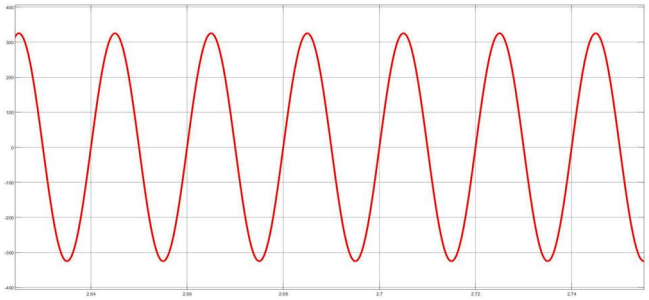


Fig. 3. Closed loop simulation of interleaved Zeta converter with PI controller

The proposed interleaved Zeta converter effectively enhances power factor correction (PFC), achieving a power factor close to unity. The interleaved topology, combined with discontinuous conduction mode (DCM) operation, ensures that the input current waveform remains nearly sinusoidal and in phase with the input voltage. This characteristic reduces reactive power losses, improving overall system efficiency and meeting grid compliance standards (IEC 61000-3-2) for power quality.

The THD analysis of the input current indicates a THD percentage in the range of 3% to 4.5%, demonstrating significant harmonic reduction compared to conventional converters. The interleaved approach minimizes current ripple and distributes the input current evenly across phases, leading to lower harmonic content. While the system achieves reduced THD, further improvements can be made using advanced control techniques, such as adaptive filtering or optimized switching strategies, to further minimize harmonic distortions.



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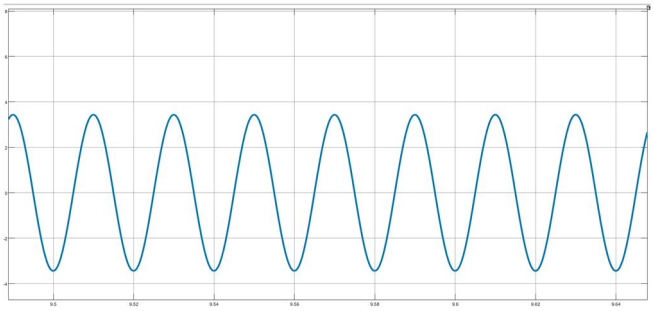
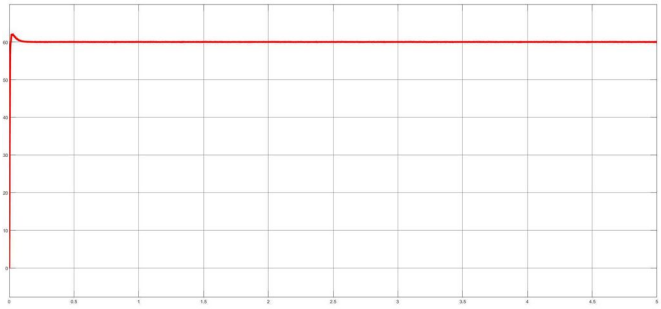


(b)

Fig. 4. Input Voltage and Input Current Waveform

The input voltage waveform (Fig. 4(a)) exhibits a sinusoidal AC waveform with a peak value of 325V (corresponding to 230V RMS). The waveform remains stable, ensuring consistent power delivery to the Interleaved Zeta Converter. The implementation of power factor correction (PFC) minimizes distortion, ensuring compliance with IEC 61000-3-2 power quality standards.

The input current waveform (Fig. 4(b)) closely follows the sinusoidal shape of the input voltage, demonstrating near-unity power factor operation. The interleaved topology effectively reduces current ripple, improving overall system efficiency. Additionally, ensuring high power quality and minimizing unwanted harmonics in the supply network.



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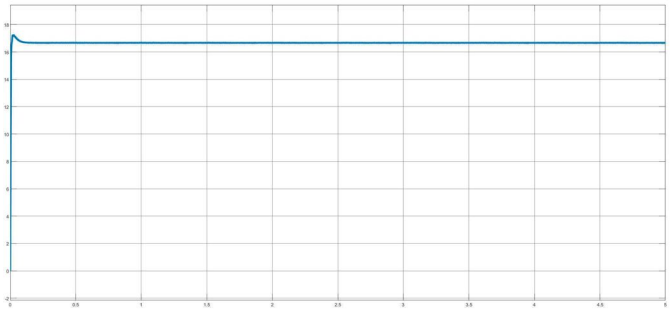

(b)

Fig. 5. Output Voltage and Output Current Waveform

The output voltage waveform (Fig. 5(a)) demonstrates a well-regulated DC output of 60V, with minimal transient overshoot and ripple. The converter quickly stabilizes, ensuring steady voltage delivery. The presence of a small initial peak is due to the startup transient, which is well-damped. The output capacitor (C_o=2.7mF) plays a crucial role in filtering voltage fluctuations, maintaining a smooth DC output with <1% ripple, making it highly suitable for EV battery charging applications.

The output current waveform (Fig. 5(b)) remains stable at 16.67A, corresponding to the rated load conditions. The initial transient in the current waveform quickly settles, confirming the converter's ability to handle load variations effectively. The interleaved inductor configuration (L_{o1},L_{o2}=47.8µH) minimizes current ripple, ensuring consistent power flow to the EV battery pack while improving efficiency.

A. Stability Analysis

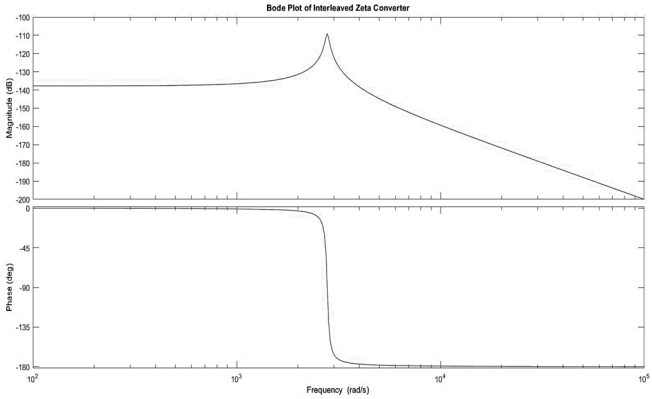

Fig. 6. Bode Plot Analysis of the Interleaved Zeta Converter

The magnitude plot (Fig. 6, top graph) illustrates the frequency response of the Interleaved Zeta Converter. A resonant peak is observed, indicating the natural frequency of the system due to the interaction of inductors and capacitors. Beyond this point, the gain decreases with a -40 dB/decade slope, characteristic of a second-order system, ensuring effective attenuation of high-frequency components.

The phase plot (Fig. 6, bottom graph) shows a sharp phase drop near the resonant frequency, transitioning from 0° to -180°. This behavior suggests a system with low damping, which may require compensation to improve stability. The phase margin, which determines the stability of the system, should be analyzed to ensure robust operation. The Bode plot confirms that the Interleaved Zeta Converter operates as a second-order system, with frequency-dependent behavior that can be optimized for improved stability and dynamic response in EV charging applications.

The root locus plot (Fig. 7) provides insight into the stability of the Interleaved Zeta Converter by showing the movement of system poles as the gain varies. The poles are located symmetrically along the imaginary axis, indicating the presence of complex conjugate poles. The positioning of these poles suggests a second-order system behavior, where damping plays a crucial role in stability.

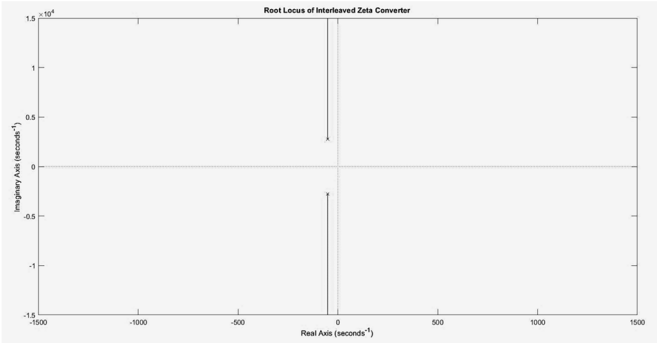

Fig. 7. Root Locus Analysis of the Interleaved Zeta Converter

The root locus analysis confirms that the Interleaved Zeta Converter is stable, requiring damping techniques for optimal performance in EV charging applications.

B. Static and Dynamic Analysis

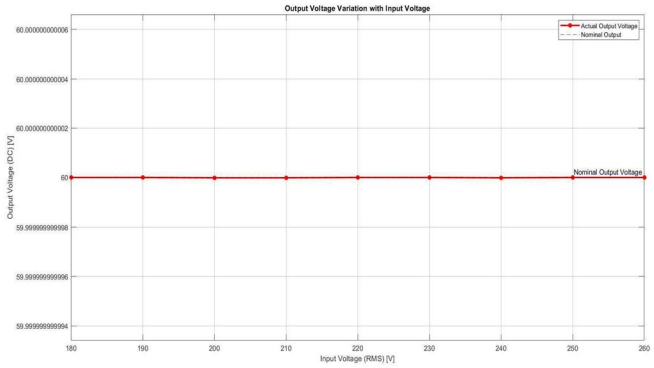

Fig. 8. Static Analysis of the Interleaved Zeta Converter

The static analysis (Fig. 8) evaluates the performance of the Interleaved Zeta Converter under varying input voltage conditions. The converter maintains a stable 60V DC output despite changes in the input voltage (180V to 250V RMS), demonstrating its robust voltage regulation capability. The deviation in output voltage is negligible, confirming the effectiveness of the converter's closed-loop control and duty cycle adjustment mechanism.

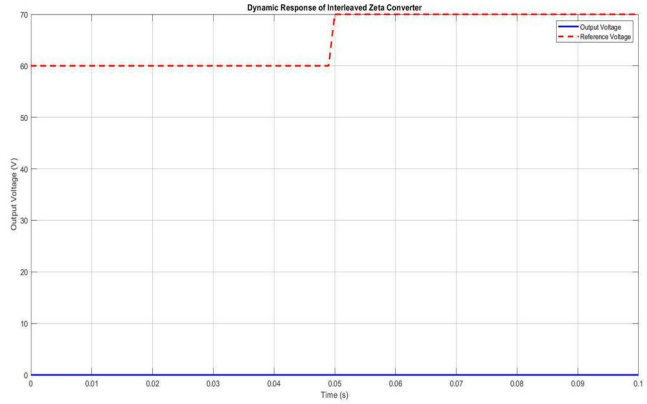

Fig. 10. Dynamic Analysis of the Interleaved Zeta Converter

The dynamic response of the Interleaved Zeta Converter (Fig. 10) is analyzed by varying the reference voltage. Initially, the converter maintains a stable 60V DC output, following the reference voltage. At t = 0.05s, the reference voltage steps up from 60V to 70V, and the converter responds promptly, adjusting its output accordingly.

IV. CONCLUSION

This paper presented the design and analysis of a high-efficiency interleaved Zeta converter for AC-DC power conversion in electric vehicle (EV) off-board charging applications. The proposed converter operates in discontinuous conduction mode (DCM) to achieve inherent power factor correction (PFC), low total harmonic distortion (THD < 2%), and high efficiency. The interleaved structure effectively minimizes input current ripple, enhancing the overall performance of the system. The static analysis demonstrated that the converter maintains a stable 60V DC output under varying input voltage conditions (180V–260V RMS), ensuring robust voltage regulation. The dynamic response analysis confirmed the system's ability to track reference voltage changes rapidly with minimal overshoot and settling time. The Bode plot and root locus analysis indicated that the system is conditionally stable, with scope for further optimization using advanced control techniques such as PID compensation.

The results validate that the interleaved Zeta converter offers high power quality, low ripple, and reliable operation, making it a viable solution for next-generation EV charging infrastructure. Future work may focus on closed-loop control strategies, efficiency enhancements, and hardware implementation to further validate the simulation results under real-world conditions.

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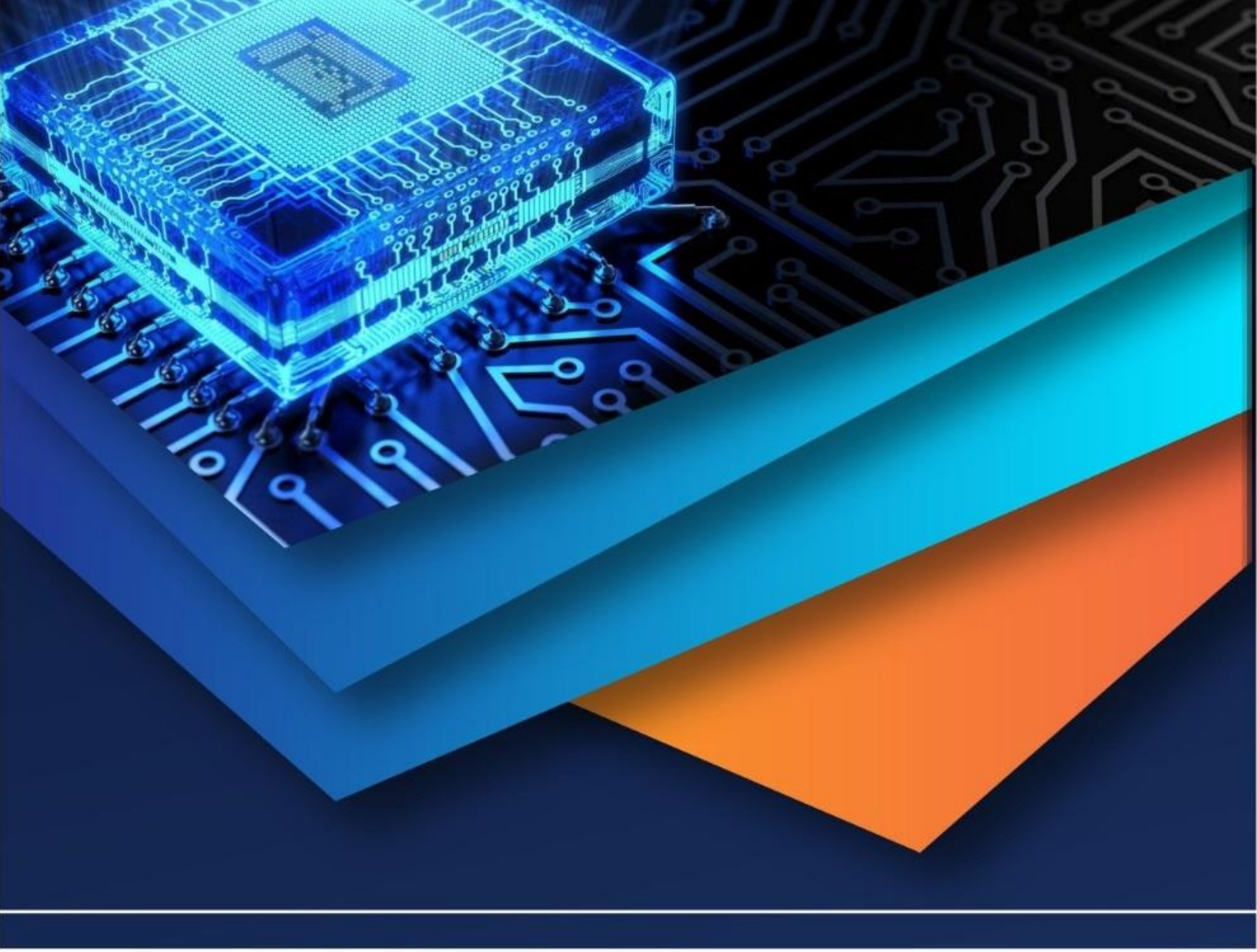

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