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Design of GPIO Transmitter

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Abstract: ***This paper presents a comprehensive design approach for a versatile 1.8V GPIO transmitter tailored for a 5pf load capacitance. The work introduces a novel design that accommodates 1.8V IO supply, enhancing the flexibility and compatibility of the GPIO transmitter. The GPIO consists of a level shifter and a driver. A level up shifter is used along with a driver capable of driving the signals without any data loss. The work embarks on the objective of designing a robust GPIO transmitter by utilizing a combination of level shifting and driver circuitry. The methodology encompasses meticulous simulation-driven design, encompassing a 45nm technology node and the Cadence Virtuoso platform. The design incorporates a level shifter that elevates input data from a core domain operating at 0.8V to IO levels of 1.8V , ensuring seamless communication across various voltage domains. The driver circuit, implemented with progressive sizing, effectively drives the substantial load capacitance of 5pF, maintaining the integrity of input data. Through detailed analysis, the architecture ensures compliance with the demanding specifications of Intel Max 10 FPGA. Simulation results exhibit the efficacy of the proposed design. The level shifter successfully transforms an incoming 0.8V data signal to 1.79V , aligning with the 1.8V IO requirements. The driver also drives the same signal out with a load of 5pf. The level shifter and driver is combined to check for the working of transmitter, with input at 0.8V and the signal is obtained at the expected voltage level at the output of driver.***

Keywords: GPIO, Transmitter, Level shifter, Driver, Cadence, Layout, 45nm technology

I. INTRODUCTION

The General Purpose Input Output plays a pivotal role in bridging the gap between microcontrollers and various electronic devices, enabling seamless communication and control. It's like a translator, facilitating the exchange of information and instructions between devices that speak different "languages." Just like a bridge, GPIOs ensure that signals from the microcontroller, which operates at a specific voltage level, can be effectively conveyed to and interpreted by external components.

Here the focus is directed towards the implementation of GPIOs optimized for a voltage threshold of 1.8V. This voltage threshold holds importance due to its relevance in modern electronic systems, where energy efficiency and compatibility with lower voltage standards are critical considerations.

The transmitter block, a crucial intermediary responsible for conveying signals from the microcontroller's core circuitry to the output pin. This block consists of the level shifter, and driver. These components collaborate harmoniously to ensure signal integrity, efficient voltage level conversion, and optimal output performance.

When devices with varying voltage requirements need to talk to each other, a level shifter steps in to ensure that signals are understood correctly. It's like having a mediator who can speak both languages fluently and convey messages accurately. Level shifters play a crucial role in maintaining compatibility and enabling data exchange between different parts of a circuit or between distinct electronic devices.

In essence, a level shifter's task is to take a signal from one voltage level and convert it to another voltage level that the receiving device can understand. This translation process is vital to prevent data corruption, signal distortion, or even damage to sensitive components. Level shifters come in various designs and configurations to accommodate different voltage disparities and communication protocols.

Imagine a scenario where a device operating at 3.3V trying to communicate with another device running at 1.8V. Without a level shifter, their "conversation" would be confusing, like two people speaking different languages without a translator. A level shifter steps in and ensures that the signal from the 3.3V device is translated accurately to 1.8V so that the other device can comprehend it properly. The complexity of level shifters varies based on factors such as the voltage levels involved, the speed of communication, and power efficiency requirements. Some level shifters are simple, working like basic language translators, while others are more advanced, considering intricate nuances of voltage transition and signal timing.

The design of the driver is a pivotal decision point, heavily influenced by the load-bearing capacity of the circuit. Just as a vehicle's design depends on its intended use, the driver's configuration must be tailored to meet the specific requirements of the circuit it interacts with. Here a load capacitance of 5pf is considered.

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II. DESIGN AND METHODOLOGY

The methodology employed here involves a systematic approach to designing a 1.8V GPIO transmitter for the load capacitance of 5pf. The design process encompasses various stages, including level shifting, driver circuit design and simulation.
The general block diagram of a transmitter and its components is shown in figure 1.

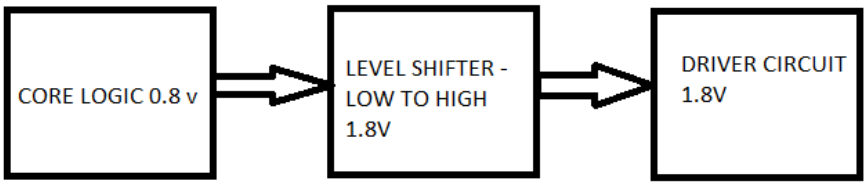

Figure 1: Block diagram of a transmitter

A. Design of Level Shifter

Design a level shifter to elevate the input data levels from the 0.8V core domain to the desired 1.8V IO levels.

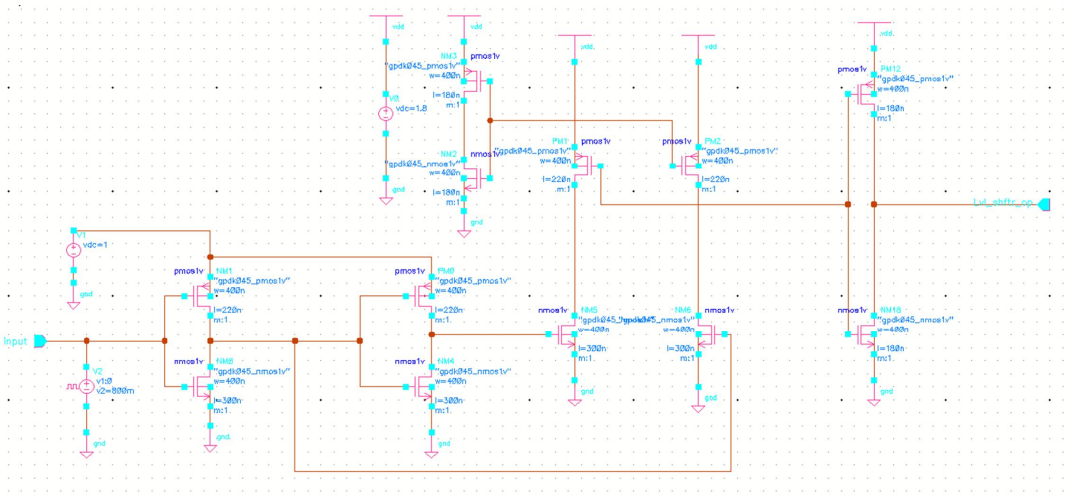

Figure 2: Schematic of Level shifter

To ensure effective level shifting in the context of a 45nm technology design, thoughtful selection of transistor configurations and sizing becomes paramount. The objective is to seamlessly bridge the gap between different voltage domains while adhering to the specifics of the 45nm technology.
At the input to the transmitter: Data-in. This input emanates from the core domain, which operates at a core supply of 0.8V. However, this core-level signal is inadequate to directly drive the main driver, which functions at the IO supply level of 1.8V. The primary task is to facilitate this transition, transforming the core-level signal into an IO-compatible signal at 1.8V. The design of a high-speed level shifter is therefore orchestrated to perform this crucial task.
In this setup, a pair of NMOS devices takes center stage. These devices receive input signals, namely IN and IN BAR, which are characterized by core-level voltages of 0.8V. The process unfolds as follows: When the input signal IN registers a logic high (logic-1), the N0 transistor is activated. Following this, the P0 transistor is engaged, leading to the gradual pull-up of the vn node to the IO voltage level of 1.8V. Similarly, in instances where IN BAR holds a logic high, the vp node is progressively elevated to 1.8V.
This yields a level-shifting mechanism that enables seamless translation of input signals from the core voltage domain (1V) to the IO voltage domain (1.8V). It's akin to a relay, where the core-level signals are passed on to a mechanism that appropriately elevates them to IO voltage levels for compatibility.
This is further fortified by the integration of inverters operating at the IO voltage level. These inverters are strategically positioned to serve as differential outputs, acting as the conduits that ultimately carry the transformed signals. The interplay between the NMOS and PMOS devices, combined with the IO-level inverters, results in a comprehensive system that ensures accurate and rapid level shifting.

B. Design of Driver

The level shifter on its own lacks the capability to effectively drive the substantial 5pF load capacitance. To address this challenge, a dedicated driver circuit is engineered. This circuit serves the purpose of efficiently propelling larger capacitance loads while preserving the inherent attributes of the input data.

The design of the driver circuit revolves around the need to accommodate the considerable load capacitance. A single-stage buffer could potentially suffice, but it comes with the caveat of necessitating a substantial current output to manage the load capacitance effectively.

To overcome this limitation and find a more efficient solution, an innovative approach known as progressive sizing is adopted in the driver design. The schematic representation of this approach depicts the cascading of inverters, each equipped with incrementally increasing drive strengths. The components involved in this configuration are labeled as follows: 'A' represents the sizing factor, 'N' denotes the number of stages, 'CIN' signifies the input capacitance, and 'COUT' stands for the output capacitance of the final stage.

Applying this progressive sizing approach to the design at hand, the driver must be engineered to manage a load capacitance of CLoad = 5pF. The input capacitance of the initial-stage standard CMOS inverter is quantified as CIN = 5fF. With careful consideration, a total of four stages (N = 4) is deemed suitable, and a sizing factor 'A' is computed as 5.68.

Ensuring symmetry and balance in performance, the aspect ratios of the devices comprising the first-stage CMOS inverter are meticulously chosen based on the established design of a standard CMOS inverter, where charging and discharging times remain equivalent.

Moving progressively through the stages, the aspect ratios of the CMOS inverter devices are systematically increased by a factor 'A' compared to their respective preceding stages. This approach is consistently applied across the second, third, and fourth stages, optimizing each stage's capability to manage the increasing load.

For an at-a-glance reference, the specific aspect ratios assigned to each device are outlined in Figure 3. This comprehensive design approach, embracing progressive sizing, empowers the driver circuit to effectively handle the substantial capacitance loads, ensuring the integrity of data transmission while accommodating the distinct challenges posed by the load capacitance.

	First-stage	***Second-stage***	***Third-stage***	***Fourth-stage***
PMOS $(W/L)_{0,1,2,3}$	0.96 /0.2	5.76 /0.2	11.52 /0.2	66.66 /0.2
PMOS $(W/L)_{4,5,6,7}$	0.328 /0.2	1.968 /0.2	39.36 /0.2	44.608 /0.2
NMOS $(W/L)_{0,1,2,3}$	0.32 /0.2	1.968 /0.2	38.4 /0.2	43.52/0.2
NMOS $(W/L)_{4,5,6,7}$	0.32 /0.2	1.968 /0.2	38.4 /0.2	43.52/0.2

Figure 3: Aspect ratios of the devices

The schematic of the driver is shown below in the figure 4.

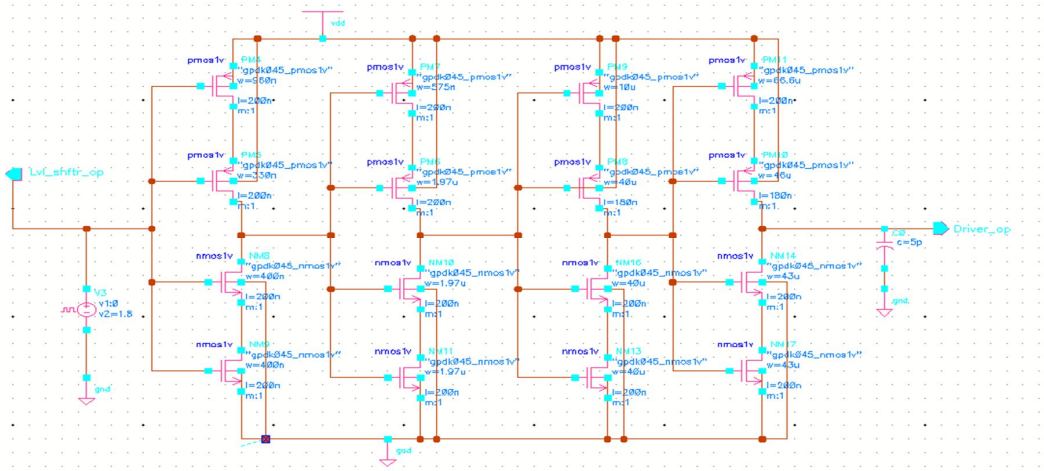

Figure 4: Schematic of driver

The driver and the level shifter are connected together to form the transmitter. The figure 5 below shows the schematic of the transmitter.

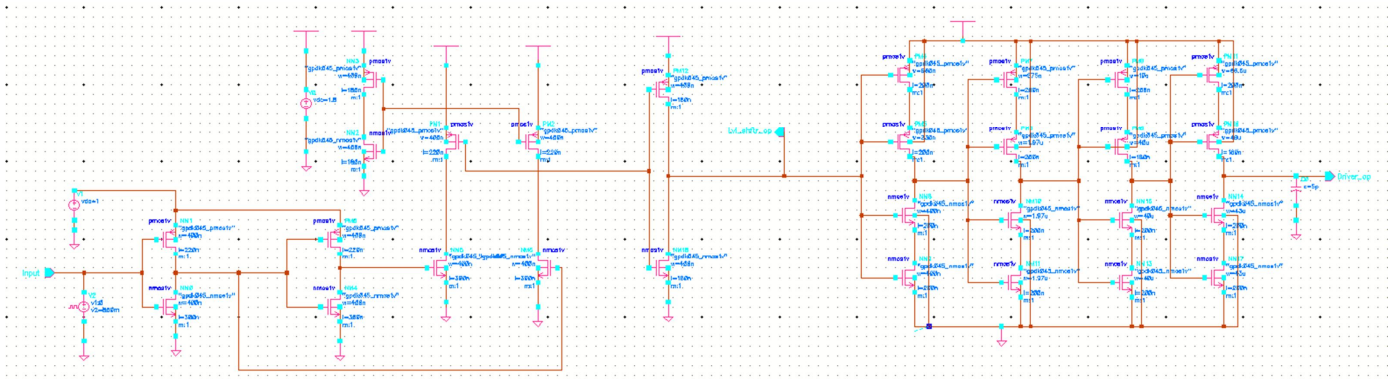

Figure 5: Schematic of transmitter

III.RESULTS AND DISCUSSION

The simulation waveform of all the schematic designs are shown in this section. The figure 5 below shows the simulation of level shifter. The input signal at 0.8V is successfully shifted to 1.791V.

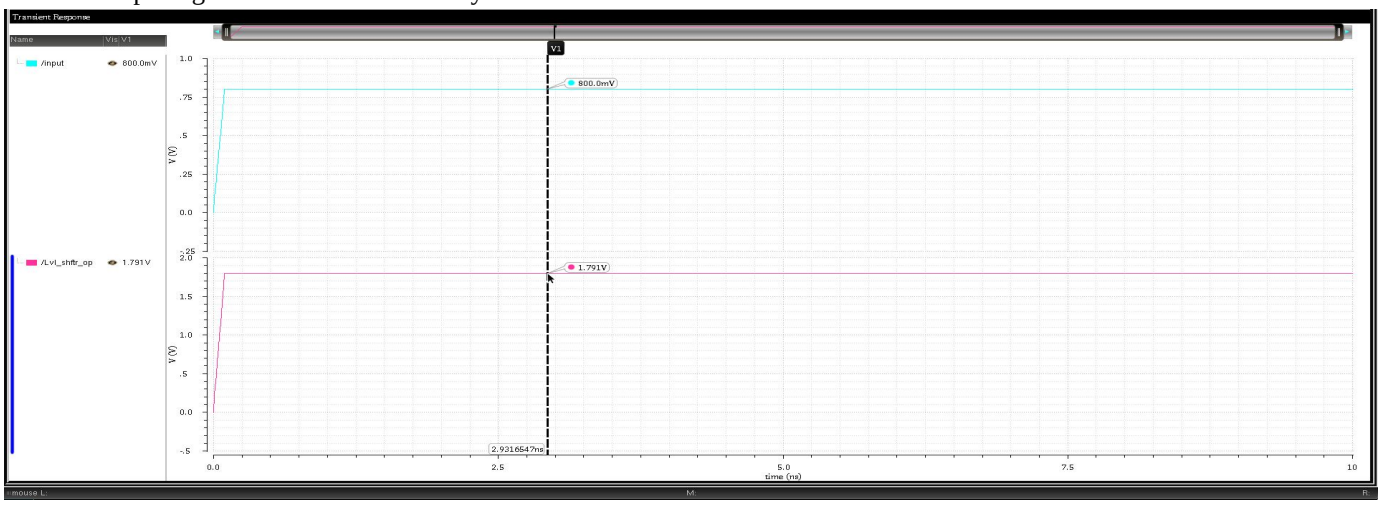

Figure 6: Simulation waveform of level shifter

Figure 6 below shows the simulation of driver. The input signal at the driver and the output should be at the same levels which can be clearly observed. The load capacitance of 5pf is driven by thus driver.

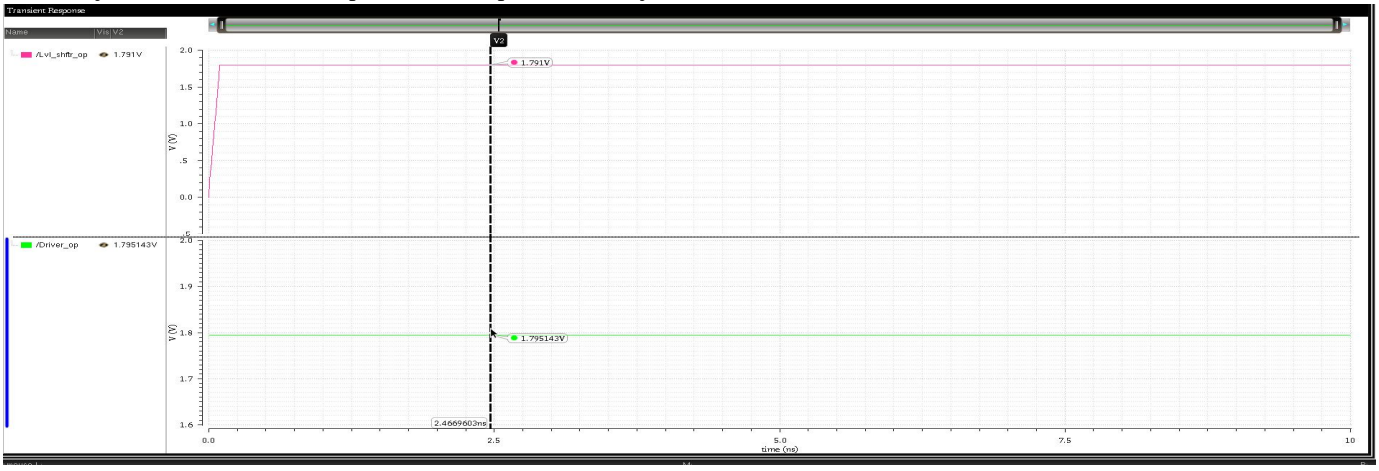

Figure 7: Simulation waveform of driver

The transmitter is a combination of both level shifter and the driver. The waveform below in figure 7 shows the input signal at 0.8V is successfully level shifted and driven out. The intermediate result at the junction is also shown.

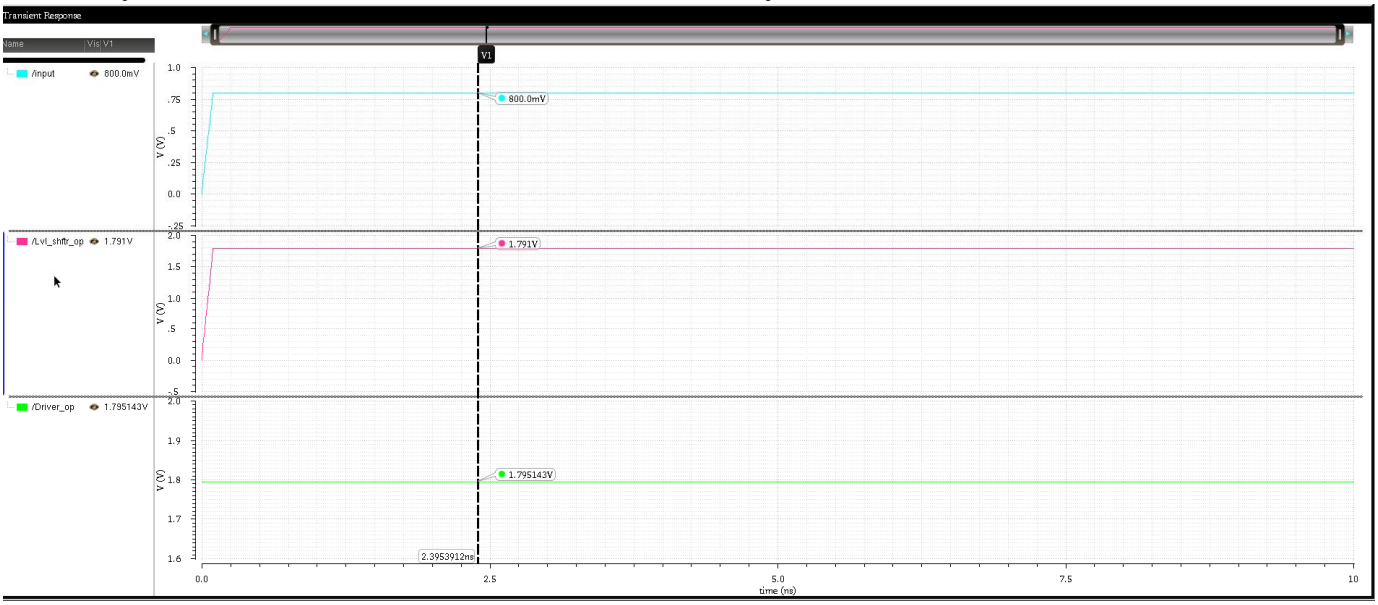

Figure 8: Simulation waveform of transmitter

IV. CONCLUSIONS

Here the design of GPIO transmitter for load capacitance of 5pf is presented. The proposed design is realized on cadence virtuoso platform with 45nm technology node. The level shifter and driver is designed separately and later combined to form the transmitter. The level shifter performs up shifting of signal from 0.8V to 1.8V and the driver drives it with a load capacitance of 5pf. The input signal of 0.8v is successfully level shifted to 1.8V and transmitted through the driver.

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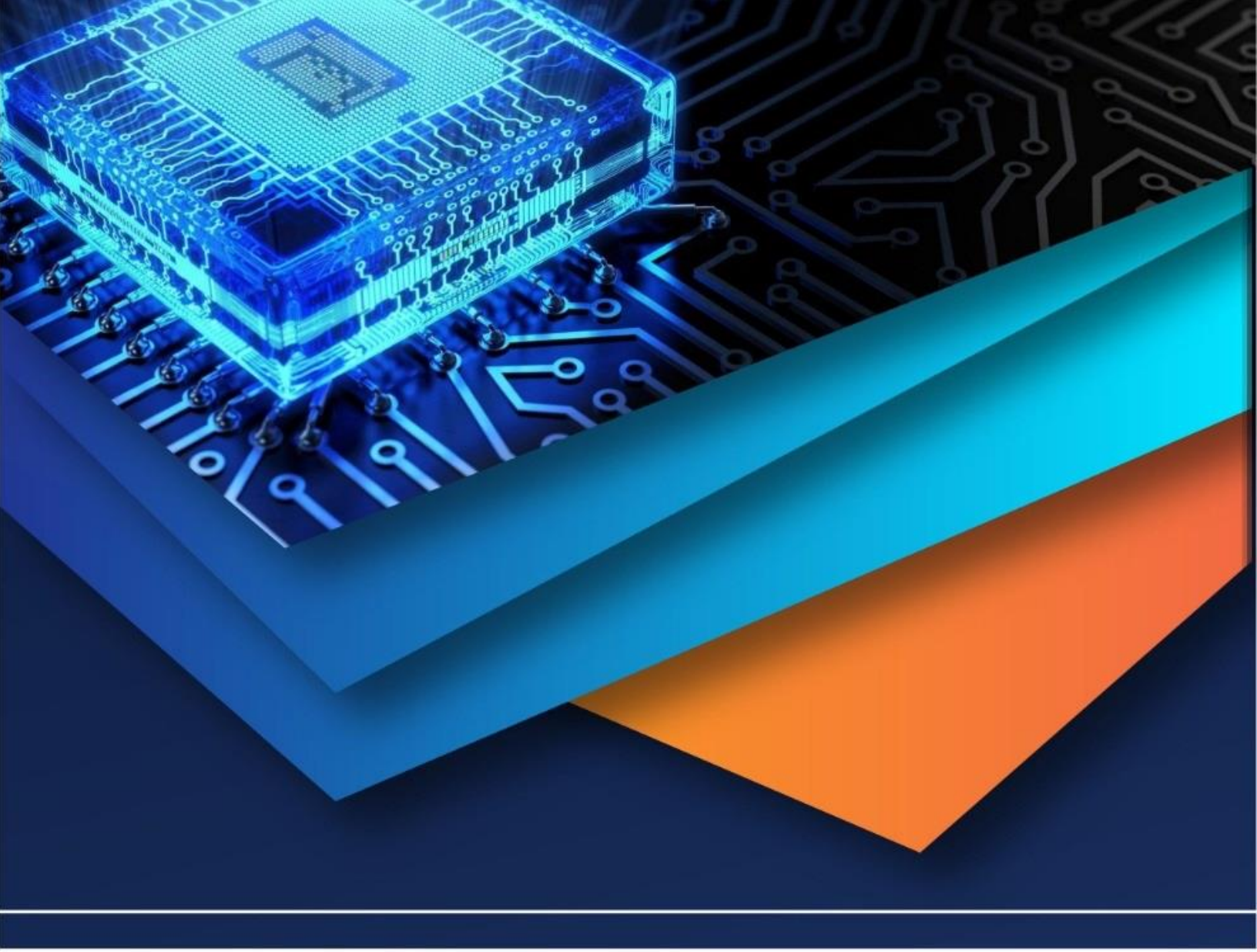

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