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Physical Design of VCO with Wide Frequency Tuning Range Using Deep Submicron CMOS Technology

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***Abstract:** This paper presents a new design approach of CMOS voltage controlled oscillator (VCO) with low power and wide frequency tuning range. A novel current starved delay cell has been proposed based on dual delay path architecture. The results have been obtained in 45 nm CMOS technology with supply voltage 1 V. The proposed VCO achieves a controllable frequency range from 1.81 GHz to 10.55 GHz with a wide tuning range. The control voltage (Vctrl) has been varied from 0.3V to 1V for obtaining the different output frequencies. The power dissipation of proposed VCO is 34.932 uW with current consumption as 0.079 mA at a control voltage of 1V and very optimised surface area as 14.8µm2.*
***Keywords:** Current starved delay cell, Low Power, Tuning range, VCO, etc.*

I. INTRODUCTION

The voltage-controlled oscillator (VCO) is very useful in applications such as: analog-to-digital converters [1] [2], phase-locked loops [3], and it continues. In last three decades, the high speed and low power consumption are the major design consideration in portable electronic devices.

Voltage Controlled Oscillator (VCO) is an oscillator whose output frequency can be varied over a range and can be controlled by the input DC voltage. The output frequency of VCO may vary from a few hertz to GHz, depending on the design of the VCO. The period of oscillator is equal to the product of the number of stages and delay of each inverter [4]. The delays can be controlled using two ways, capacitance and current of the device. With changing length of transistor technology, capacitance can be altered to observe change in frequency but at a current existing application requires to have one stable single channel length, hence the inverter current is altered. Connecting a trail of the inverter blocks with a feedback gives a 'Ring' configuration to the oscillator. Furthermore, biasing circuit is included in the design to introduce the control voltage into the oscillator for control over frequency of oscillations. Hence, it's called Ring VCO [4].

Another VCO architecture is an improved version of Ring VCO, called Current Starved VCO. The operation is similar to Ring VCO with additional MOS transistors are added so as to operate as current sources with the MOS transistors that operate as inverter. This technique is known as current starving. The current source produces control current to lower the threshold voltage of inverter transistors, which increases the effective drive resistance and thus increases the delay [3].

The desired considerations in designing a VCO is associated to accomplish low power consumption, minimum layout area, high frequency and wide control tuning and voltage range. These target specifications become very difficult to achieve due to the continuous down scaling of silicon CMOS technologies [10]. Now a days, designing a VCO in a ring topology is frequently a more attractive alternative because it allows accomplishing a wide tuning (control voltage) range, small layout area, high gain, low cost, robustness to variations, simplicity and scalability in nanoscale CMOS processes [7] [8]. As we know that, CMOS technology shrinking with time and shifting towards nanometer feature sizes which interconnect in the order of delays and leakage power, dominating gate delays and dominating power. High performance and low power circuit design face many challenges [7] [8] [10].

A voltage control oscillator can be design by using different technique but the most efficient technique is to use the ring oscillator, as ring oscillators are very small in size & compatible with digital circuitry. Hence the VCO design by using ring oscillators makes them ideally suited to provide clocks for systems. The oscillation frequency F_osc of a VCO can be evaluated by,

$$F\_osc = \frac{1}{2N\ Stages\ tD}$$

$$F\_osc = \frac{ID}{2N\ Stages\ CG\ Vth}$$

Where, ID is drain current, N indicates the number of stages and t is a time constant that depends on the associated resistance of the active load and the value of the capacitor load [5]. F_osc varies in a range determined by a control voltage Vctrl, and depends on the number of CMOS differential stages N, but decreasing N yields a reduction in gain, which may result in the oscillation mitigation [1] [2] [5].

This paper proposed a physical design of current starved VCO using CMOS 45nm technology with BSIM 4 MOS modelling technique considering low power design with wide tuning range of frequency. The proposed VCO is simulated to Monte Carlo simulations and power dissipations variations for random variables. The analysis is repeated 50 times and the effect of the same is varied on the power dissipation is verified. This analysis will show the behavior of proposed VCO to robust.

II. PROPOSED DESIGN OF VCO

A voltage-controlled oscillator (VCO) is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The VCO generates a clock with a controllable Frequency. The VCO is commonly used for clock generation in phase lock loop circuits. The clock may vary typically by +/-50% of its central frequency. The proposed typical transistor sizing with respect to Width and Length is given in the table below considering the current of each transistor.

Table 1: Proposed Transistor sizing

Transistor (PMOS)	Width (W)	Length (L)	Transistor (NMOS)	Width (W)	Length (L)
P1	0.240 um	0.040 um	N1	0.200 um	0.340 um
P2	0.440 um	0.040 um	N2	0.200 um	0.040 um
P3	0.440 um	0.040 um	N3	0.200 um	0.040 um
P4	0.440 um	0.040 um	N4	0.200 um	0.040 um
P5	0.440 um	0.040 um	N5	0.200 um	0.040 um
P6	0.440 um	0.040 um	N6	0.200 um	0.040 um

The current-starved inverter chain uses a voltage control ‘Vctrl’ to modify the current that flows in the N1, P1 branch. The current through N1 is mirrored by N2, N3, N4, N5 and N6. The some current flows in P1. The current Through P1 is mirrored by P2, P3 and P4. Consequent by the change in ‘Vctrl’ induces a global change in the inverter currents and acts directly on the delay. The figure 1 shows the schematic design of VCO using 45 nm technology. It is a transistorized design where ‘Vctrl’ is a controlling input and ‘F_osc’ is the output.

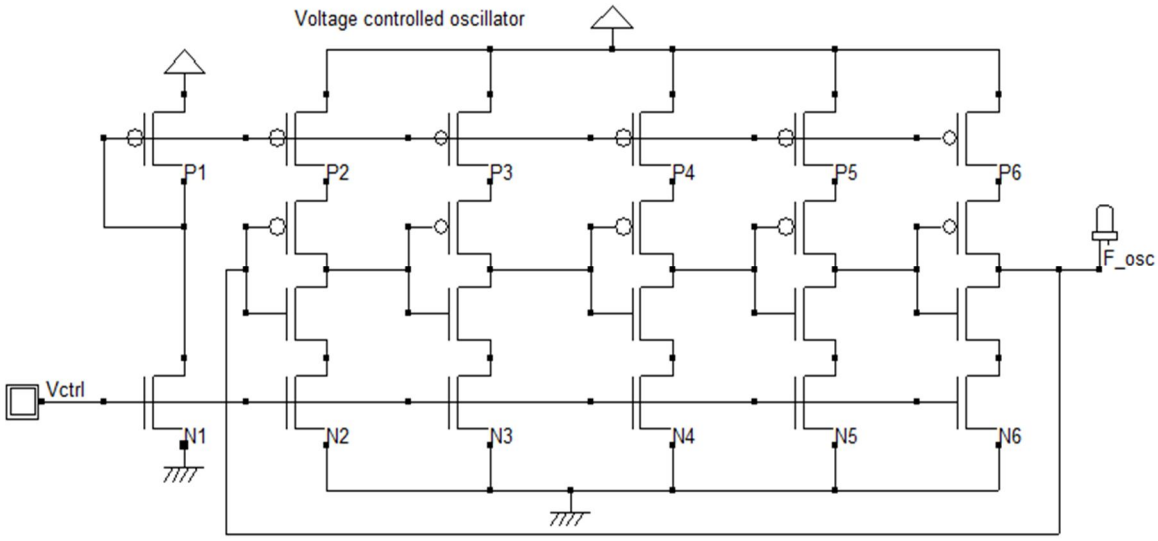

Figure 1: Schematic design of VCO

The VCO design is based on an inverter type ring oscillator supplied by a current coming from the voltage to current converter [5]. The VCO consists of five-stage fully differential delay cells performing full switching. Phase noise [5], tuning range, power consumption and device size are the main areas to be considered while designing any VCO circuit. Nowadays, the VCO designs are made in such a way that greater emphasis is on reducing power consumption, so it is difficult to achieve low phase noise and wide tuning range because of more emphasis on the low-power VCO designs [15]. The physical design of VCO is drawn using Microwind EDA Layout editing tool and verified using BSIM4 MOS Modelling for layout guidelines with Design Rule Check.

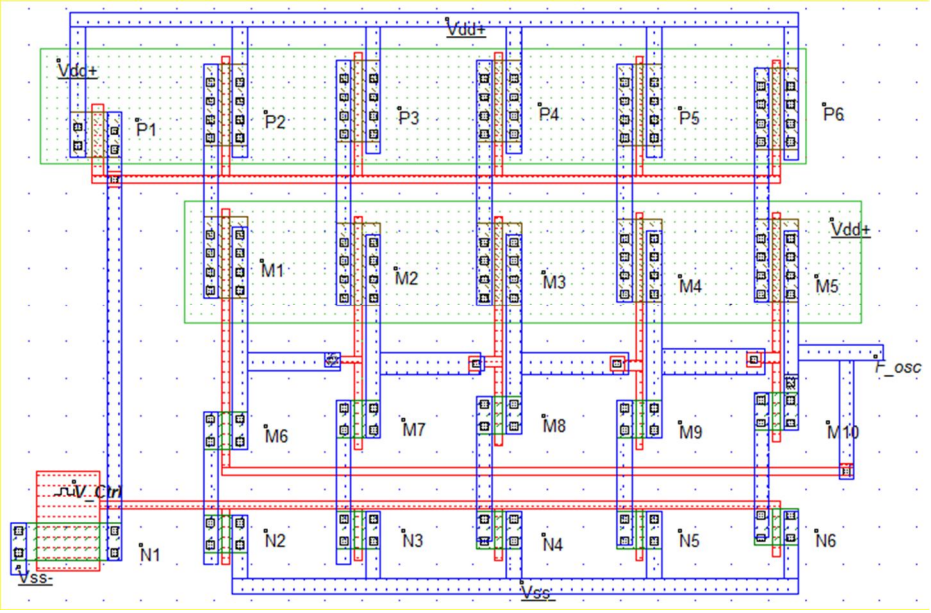

Figure 2: Physical design of VCO

III. RESULT AND DISCUSSSION

The proposed Current Starved ring VCO is simulated using Microwind software CMOS 45nm technology with control voltage variation from 0.1V to 1V.

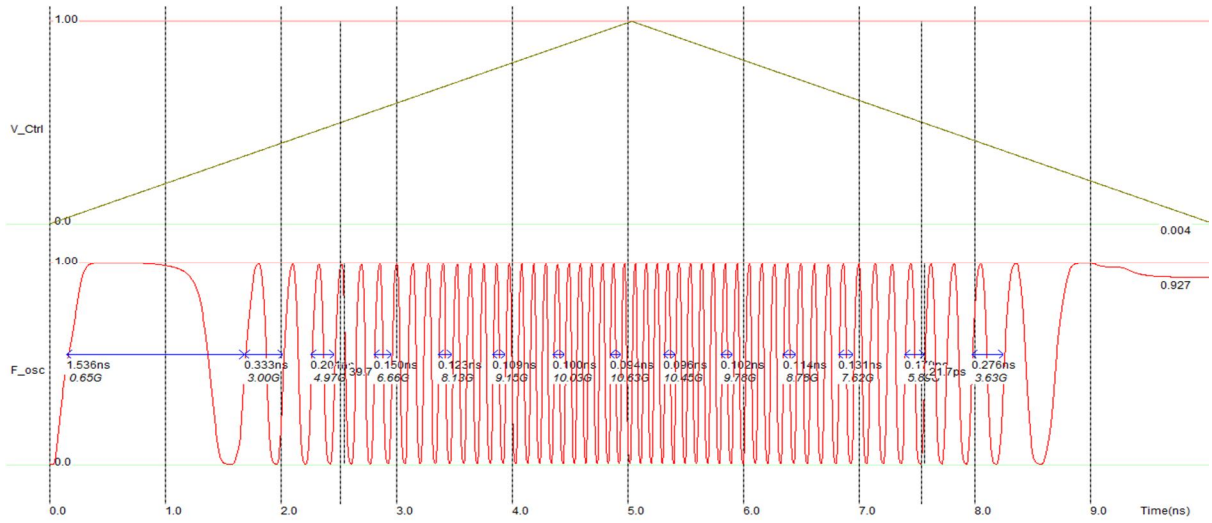

Figure 3: Transient analysis for voltage of VCO

The figure 3 shows the transient analysis of VCO. From the simulation it is clear that VCO starts oscillating with increase in frequency as the Vctrl starts increasing. The power dissipation of proposed VCO is 34.932 uW with current consumption as 0.079 mA at a control voltage of 1V.

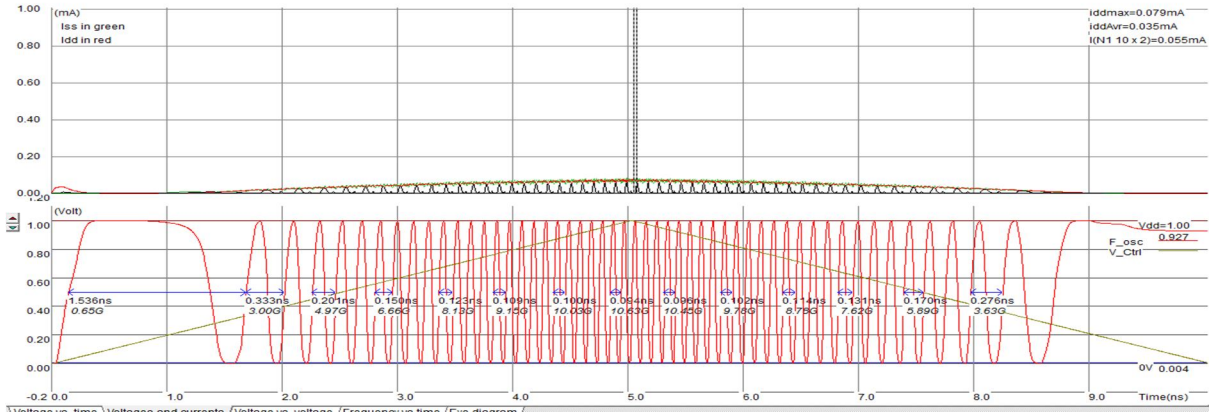

Figure 4: Transient analysis for current of VCO

We chose to modify Vctrl very slowly, in order to see the influence on the oscillations. We put Control higher than 0.5 V, because there are no any oscillations under that value. The proposed VCO achieves a controllable frequency range from 1.81 GHz to 10.55 GHz. VCO starts oscillating with 0.65GHz and maximum frequency is 10.55GHz.

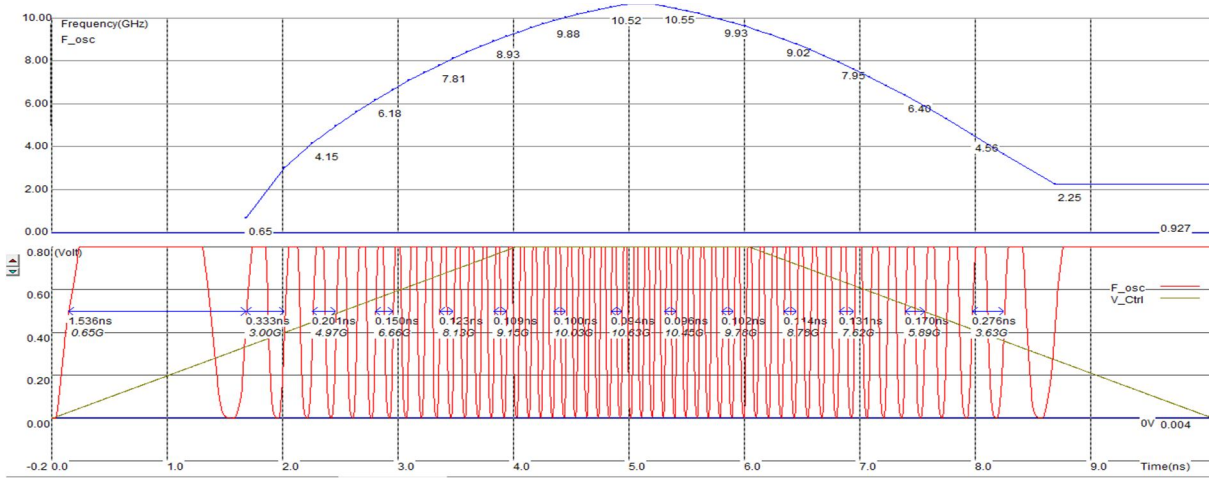

Figure 5: AC analysis of VCO

For observing the performance and stability of the proposed VCO, there is variation of supply VDD from 0.3V to 1V, the output frequency VCO increases with the increase supply voltage linearly. It proves the high stability of the VCO. The result shows the linear increase in Frequency with respect to increase in control voltage.

Table 2: Simulation results of VCO with respect to change in control voltage

	VDD=1 V	
Control Voltage (Vctrl)	Output Frequency (F_osc)	Power Dissipation
0.3 V	1.81 GHz	13.226 uW
0.4 V	3.78 GHz	25.151 uW
0.5 V	5.60 GHz	35.529 uW
0.6 V	7.13 GHz	44.382 uW
0.7 V	8.42 GHz	52.081 uW
0.8 V	9.45 GHz	58.655 uW
0.9 V	10.21 GHz	63.785 uW
1.0 V	10.76 GHz	67.797 uW

Monte Carlo analysis is an integrated circuit's statistical analysis in which a circuit devices parameters and mismatch are varied randomly. Monte Carlo simulation allows the designer to consider the possible effects of a random variation of certain circuit's parameter over its performance [16]. Monte Carlo analysis is carried out through the variation of Width (W) and Length (L) for each one of the 30 feasible solutions over many runs. The outcome of the Monte Carlo simulations is employed to compute the mean and the standard deviation of the objective function value [7] [16]. The proposed CMOS VCO is simulated to Monte Carlo simulations and power dissipations variations for 30 feasible random variables. The analysis is repeated 50 times and the effect of the same is varied on the power dissipation. This analysis will show the behaviour of proposed VCO to robust.

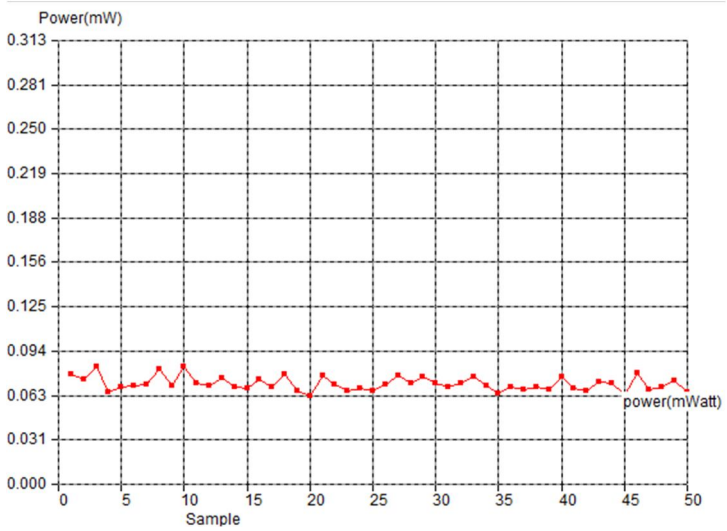

Figure 6: Monte Carlo simulation for VCO

Monte Carlo analysis is performed on the proposed VCO design. The analysis is repeated 50 times and the effect of the same is varied on the power dissipation is verified. Simulation result is shown in figure 6. From the simulations, the power dissipation ranges between 0.063mW to 0.085 mW.

IV. CONCLUSION

The proposed structure of the VCO is designed using current starved ring path techniques to achieve high oscillation frequency and a wide tuning range. VCO achieves a controllable frequency range from 0.65 GHz to 10.55 GHz with a very wide frequency tuning range with the variation in control voltage from 0.1V to 1V keeping supply voltage at 1V. The proposed VCO dissipates a power of 34.932 uW with current consumption as 0.079 mA at a control voltage of 1V and very optimized surface area as 14.8µm2.at a control voltage of 1V. The result shows the linear increase in Frequency with respect to increase in control voltage. The Monte Carlo analysis is performed on the proposed VCO design provided the robust nature of proposed design.

The proposed VCO design has been compared with previously reported design and the present approach shows significant power saving with high oscillation frequency.

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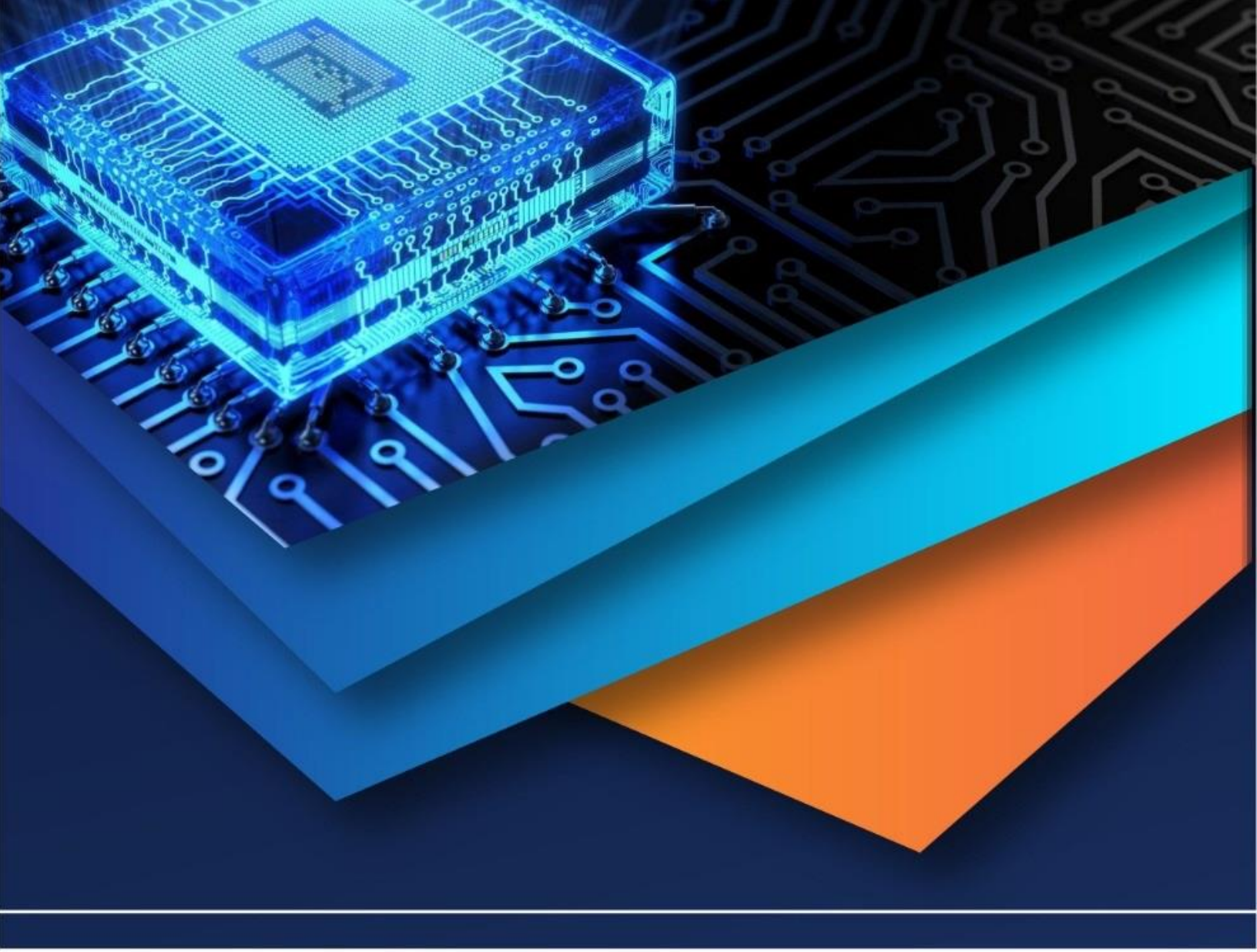

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