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Design Wallace Tree Multiplier Using Reversible Gates

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Abstract: ***Multipliers are essential components in digital circuit design. They have wide spread applications in digital signal processing and communication systems. Circuit designers in VLSI design seek compact, small scale circuits with low power consumption and minimal delay. The Wallace tree multiplier is an advanced version of tree based multipliers. Numerous algorithms have been developed to create the fastest multipliers, and the Wallace tree multiplier is one such example. It utilizes reversible compressors, full adders, and half adders. The results demonstrate that the Wallace tree multiplier using reversible gates outperforms traditional multipliers in terms of power dissipation and delay, with values of 0.027W and 29.327nS re-spectively.***

Keywords: Wallace tree multiplier, Compressor, Full adder, Half adder, Xilinx ISE

I. INTRODUCTION

Convolutional units are vital in signal proce-ssing tasks as they are heavy on computations and impact performance. The basic parts of these units are adders and multipliers, but multiplie-rs have a hefty role in se-tting the area, delay, and energy use. There is a big need for speedy, space-saving, and energy efficient multipliers in real world tasks that involve computational units [1]. Examples of these tasks are convolutional neural networks and multimedia. The act of multiplying is generally split into three parts: 1) creating partial products with an AND gate array, 2) partial product accumulation, and 3) adding the final partial products. The part where partial products are piled up is big in setting the over all delay of the multiplier action. As a result, people who research have zoomed in on making this part better [3]. They use parallel and quick accumulation methods to make the final two terms for the third part.

Algorithms from Dadda and Wallace have made considerable steps in creating architecture for delay optimization in the accumulation stage. The accumulation phase delay could be further cut down by utilizing compressors over full adders and half adders [6]. The 4:2 compressor is the compressor design that is most widely used. In modern time-s, the exploration of multipliers in approximation context has risen since they are in great demand for the successful creation of area and power optimized designs. These designs are vital for applications such as multimedia processing, neural networks, and signal processing, which can handle errors. Investigations into such optimizations have been active in areas such as CMOS, FPGA, pass transistor, and FinFET based multiplier implementations [7].

This paper aim at reduction of power consumption and delay of 8x8 Wallace tree multiplier by using the reversible logic gates and wallace tree reduction technique [4]. This is accomplished by the use of simple circuits like half adder, full adder, 4:2 compressor which are realized using the reversible logic gates like BJN gate, Peres gate and CNOT gate etc.

A. Basic Multiplication Process

The multiplication of two binary digits involves two elements they are multiplicand and the multiplier. The proce-ss consists of generating partial products. If the multiplie-r bit is '0', then the partial product will be always '0'. If the multiplier bit is '1', the partial product will be the same- as the multiplicand bit [2]. The final step is addition of the-se partial products using the half adder and full adder circuits. The block diagram shows multiplication between M-bit multiplicand and an N-bit multiplier [5].

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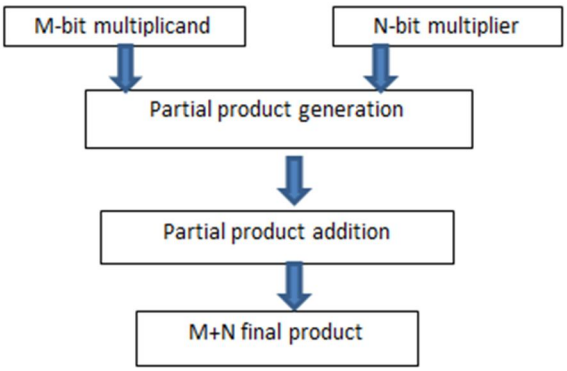

Fig 1: Multiplication process

II. LITERATURE SURVEY

1) Using parallel prefix adders, we analyse and construct a high-speed Wallace tree multiplier for very large-scale integration circuits.

Utilising four distinct PPAs the Kogge stone adder, the Brent Kung adder, the Han Carlson adder, and the Ladner Fischer adder four distinct Wallace Tree multiplier constructions have been created [13]. In phase 2, these adders are applied in the last addition procedure to enhance the multiplier's operating performance. Both steps of the multiplier operation are identical. As a first step, AND gates are used to create partial products. Use of half and full addition algorithms in a step-by-step fashion is used in Phase 2 to combine the partial products produced in Phase 1. Using PPA, the suggested design completes the second phase's incorporation of incomplete products [19].

2) Array Multiplier with Reversible Logic Structure for High Performance

The simplest definition of a multiplier is a circuit of logic that performs multiplication by two or more distinct integers. If we're going to discuss multipliers, it will be from the perspective of the designer [12], not the viewer. The proposed array multiplier uses six full adders based on reversible multiplexers and four reversible half adders. There is a connection between the array's multiplier reduction stage and this array full adder that is structured around multiplexers. There is a hierarchical structure to the partial goods in the array. At each level, there are three bits, therefore a complete adder is needed. Follow up with the previous explanation to understand how this complete adder works. There is a difference in operation when using the second multiplexer of a complete adder [16]. Below, carry bits are used as inputs to the second multiplexer. Reducing power consumption and chip space, this design increases logic circuit efficiency.

3) Logic gates with reversible inputs and their uses

Reversible logic systems are becoming more popular because of their low power consumption. Reversible logic plays an essential role in the design of low-power circuits. The significant Reversible logic synthesis may be achieved using a variety of gates, including Toffoli Gate, Feynman Gates, Fredkin Gate, New Gate Sayem, Peres Gate, and many more [8]. Here we showcase an easy-to-understand reversible gate that can be used to build more intricate circuits that can be integrated into various sequential circuits, ALUs, or, and specific circuit combinations. It gives you the rundown on the fundamentals of building. Adder circuits make use of basic reversible gates, including the Peres gate, in addition to the TSG gate [18].

III. EXISTING SYSTEMS

1) Building a Modular Architecture for Low-Power Wallace Tree Multipliers

A CBMW multiplier that is both scalable and powers down quickly is suggested. Because of this, the Wallace tree multiplier may be efficiently and easily implemented on FPGA and ASIC computers [9]. Superior to previous 7:3 counter designs, the multiplier under consideration makes use of a multiplexing and XOR gate dependent adders. The product is then generated by adding the output from the previous stage with the carry form the previous column using a single fast adder in the final step.

One 7:3 counters is used each stage, which reduces hardware requirements and significantly reduces power consumption owing to enhanced localization [17].

The findings are compared with comparable multipliers published in the literature, and the modular multiplier design is synthesised for FPGA and ASIC. The MAC unit's performance is assessed based on its design utilising the proposed CBMW [11].

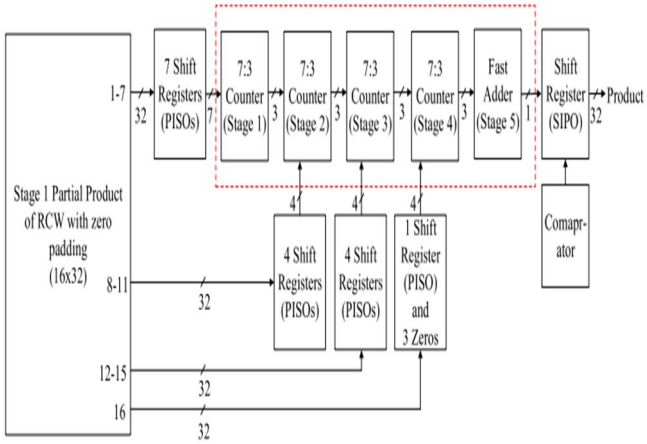

Fig 2:Counter based Wallace tree multiplier

2) Build an 8x8 Wallace Multiplier with a Full Adder & Compressor Based on MUX Network

The Wallace multipliers have two varieties. A complete adder based on MUX is used by one, while a compressor is used by the other. Because it is quicker and requires less space, the research concludes that the compressor-based Wallace multiplier is superior [10].

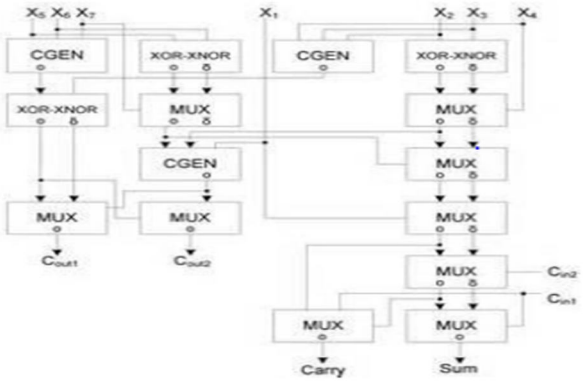

Fig 3:Compressor using multipliexer

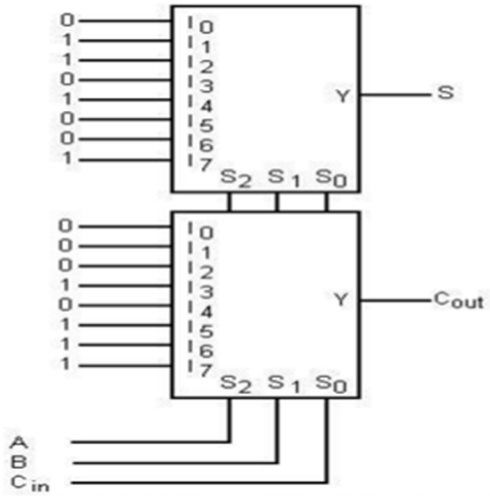

Fig 4:Full adder using multiplexer

Less space means the multiplier can work more efficiently, which is a good thing. One issue, nevertheless, does exist [14]. Both the bit size and the area increase with increasing values. In light of this, the research concludes that a MUX-based complete adder methodology, in conjunction with the compressor, is the optimal method for producing multipliers [15].

IV. LIMITATIONS OF EXISTING SOLUTIONS

As the circuit operation and the circuit complexity increases then the overall delay of the design circuit will also increase so which will result in the higher delay of the designed circuit.

Due to the complex structure of existing solution multiplier circuit consume more power during the circuit operation [20].

V. PROPOSED WALLACE TREE MULTIPLIER

In order to multiply two integers, a Wallace tree is a genius piece of hardware design. It is composed of three primary elements: The first thing it does is produce incomplete products. It then uses distinct components to reduce four adjacent rows. 3 types of adders: 4:2, half adders, and full adders. These components are selected according to the bit count in each column. A column with a single bit will go unchanged to the next level. Down to the last two rows, the process of cutting continues indefinitely. Next, a ripple carry adder is used to combine the last two rows.

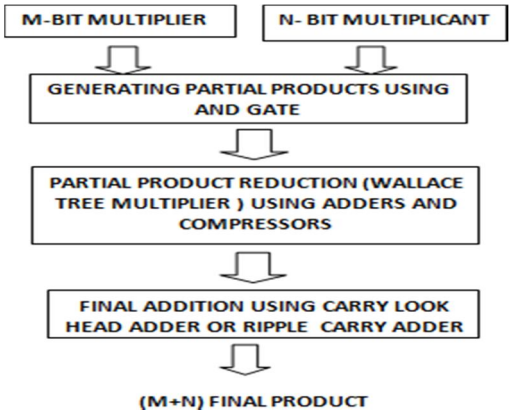

Fig 5: Design process of proposed Wallace tree multiplier

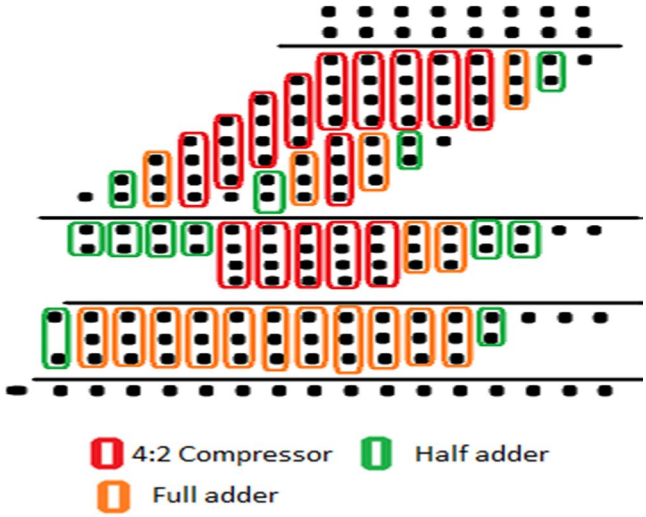

Fig 6: Proposed Wallace tree reduction technique

VI. REVERSIBLE LOGIC GATES

A Reversible logic has x inputs and x outputs with one to a function that maps the reversible gates' outputs to their inputs. You may use this to determine the outputs from the inputs and vice versa. You can get the inputs from the outputs of a reversible logic gate because of its reversible characteristic.

A. CNOT Gate

CNOT gate also called as Feynman gate. This gate has two inputs and two outputs. Inputs (A, B) and outputs (P, Q). outputs P=A and Q=A⊕B.

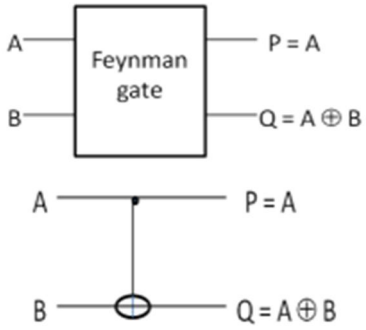

Fig 7: CNOT gate

Table 1: CNOT gate truth table

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. Toffoli Gate

Toffoli gate has three inputs (A, B, C) and three outputs (P, Q, R). P=A, Q=B, R=AB⊕C.

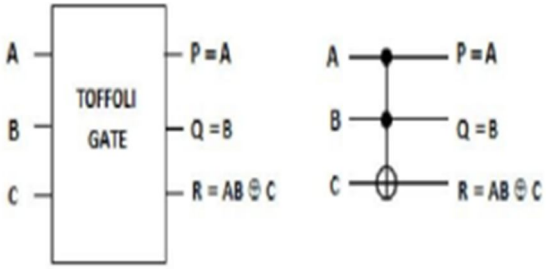

Fig 8: Toffoli gate

Table 2: Toffoli gate truth table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

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C. Fredkin Gate

The Fredkin gate is designed with 3 inputs and 3 outputs. A, B, and C for inputs and P, Q, and R for outputs.
Outputs P=A, Q=$\overline{A}\ B \oplus AC$, R=$\overline{A}\ C \oplus AB$.

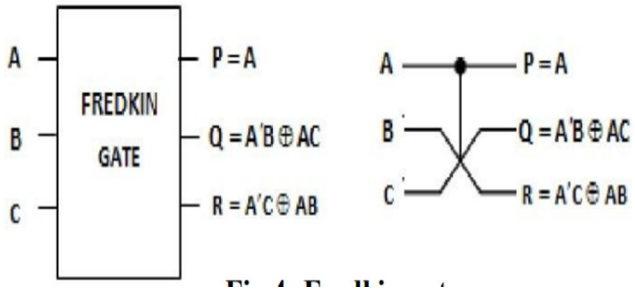

Fig 9: Fredkin gate

Table 3: Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

D. Peres Gate

There are three inputs & three outputs on a Peres gate. A, B, and C are inputs, whereas P, Q, and R are consequences.
Outputs defined as P=A, Q=A⊕B, R=AB⊕C.

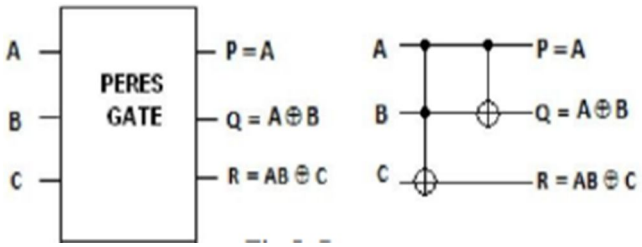

Fig 10: Peres gate

Table 4: Peres gate truth table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

E. BJN Gate

Each BJN gate has 3 inputs and 3 outputs. Here we have (A, B, C) as inputs and (P, Q, R) as outputs.
Outputs defined as P=A,Q=B,R=(A+B)⊕C.

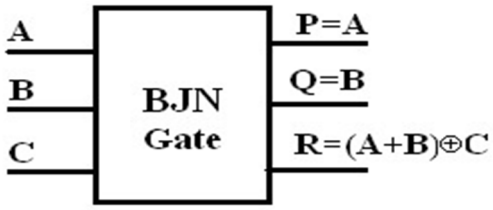

Fig 11: BJN gate

Table 5: BJN gate truth table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

VII. IMPLEMENTATION OF HALF ADDER, FULL ADDER AND COMPRESSOR

A. HALF ADDER

Half adder is a digital circuit has two inputs A , B.and outputs SUM and CARRY.

SUM=A⊕B …..(1)

CARRY=A.B…(2)

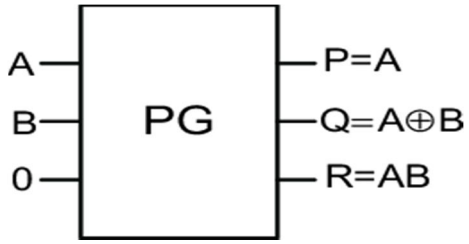

Fig 12: Half adder using reversible Peres gate

B. FULL ADDER

Three digital inputs (A, B, and C) and two outputs (SUM and CARRY) make up a full adder.

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SUM=A⊕B⊕C …….. (3)

CARRY=AB+BC+CA… (4)

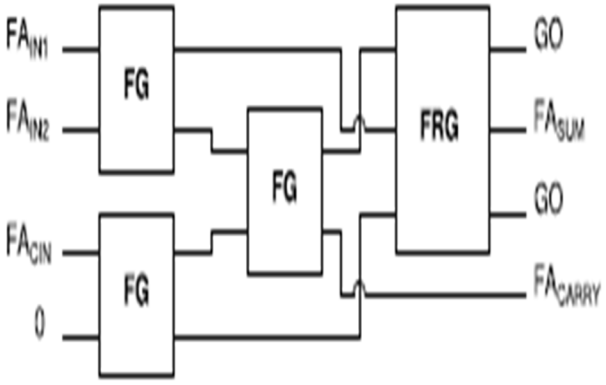

Fig 13: Full adder using reversible feyman and fredkin gate

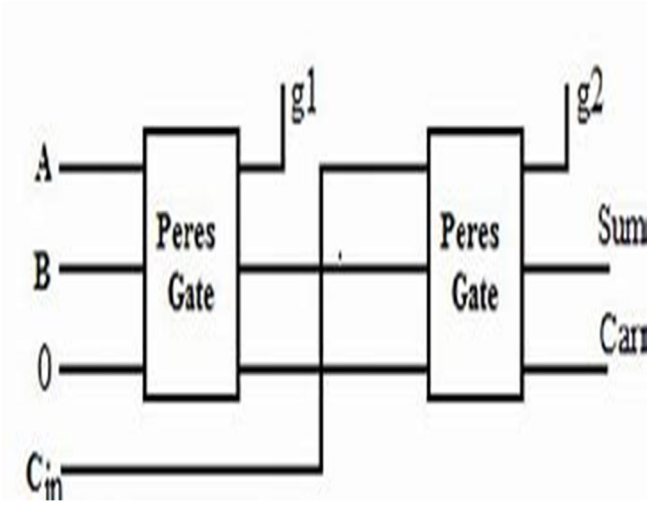

Fig 14: Proposed Full adder using reversible Peres gate

C. 4:2 COMPRESSOR

The partial product accumulation step of high-performance parallel multipliers uses 4:2 compressors to decrease latency. For every two outputs, a 4:2 compressor takes in four inputs.

SUM= $\overline{A}\,\overline{B}(C \oplus D) + C.D(A \oplus B) + \overline{C}\,\overline{D}$(A⊕B) +A.B (A⊕B) -------- (5)

CARRY= $(C \oplus D)(A \oplus B) + CD + AB$-------- (6)

Table 6: Truth table of Proposed 4:2 compressor

A	B	C	D	SUM	CARRY
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	1

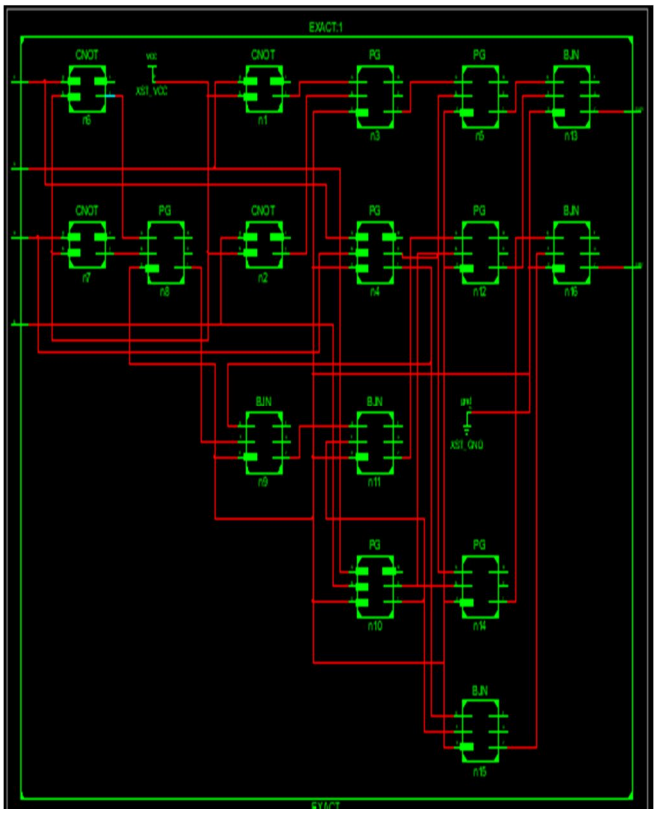

Fig 15: Synthesis of proposed 4:2 compressor

Utilising reversible CNOT, BJN, and Peres gates, the above mentioned 4:2 compressor designed.

VIII. RESULTS

Simulation and synthesis results are carried out by Xilinx ISE Design Suite 13.2 .
RTL Schematic:

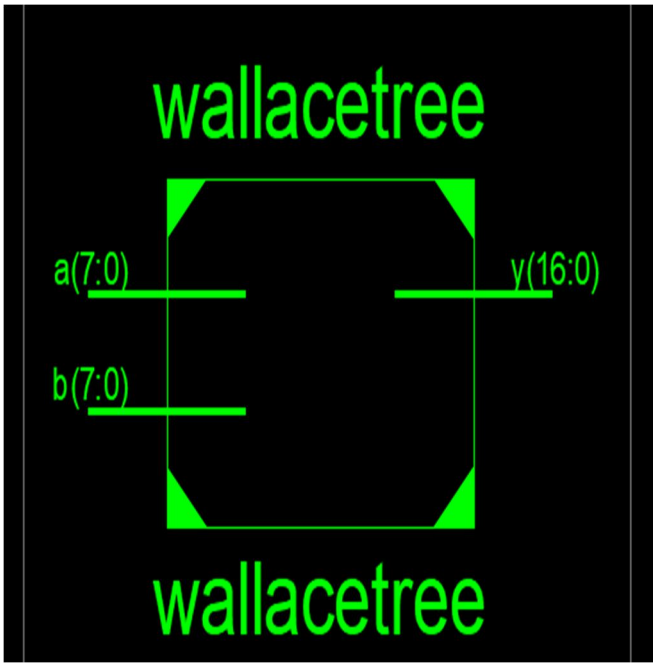

Fig 16: Wallace tree multiplier Synthesis block

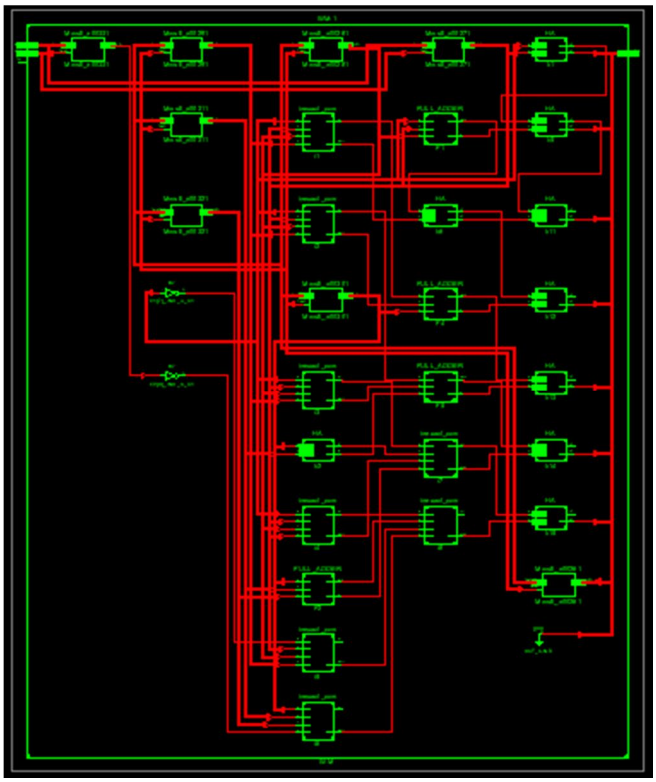

Fig 17: Synthesis of proposed Wallace tree multiplier

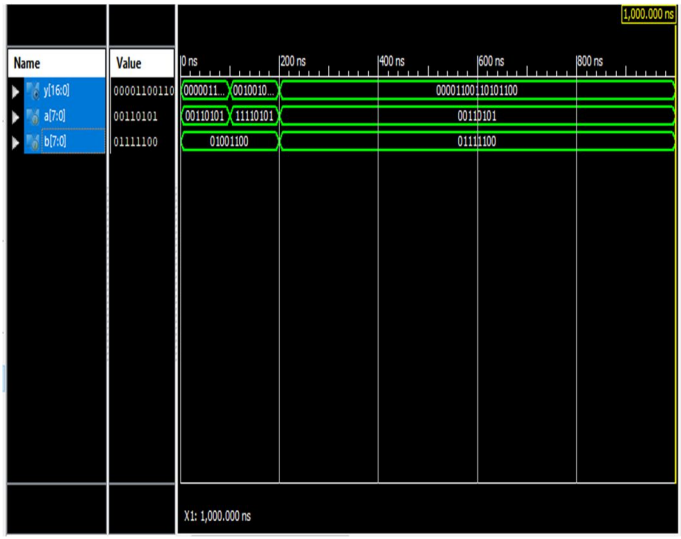

Fig 18: Simulation results of proposed Wallace tree multiplier

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	133	1,536	8%
Number of occupied Slices	74	768	9%
Number of Slices containing only related logic	74	74	100%
Number of Slices containing unrelated logic	0	74	0%
Total Number of 4 input LUTs	133	1,536	8%
Number of bonded IOBs	33	124	26%

Fig 19: Design utilization Summary of Wallace tree multiplier

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Total                     29.327ns (12.809ns logic, 16.518ns route)
                                   (43.7% logic, 56.3% route)

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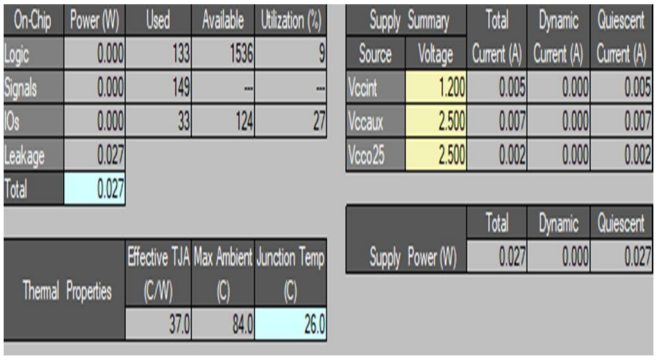
Fig 20: Timing report



On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	133	1536	9
Signals	0.000	149	--	--
IOs	0.000	33	124	27
Leakage	0.027			
Total	0.027			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.005	0.000	0.005
Vccaux	2.500	0.007	0.000	0.007
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.027	0.000	0.027

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	37.0	84.0	26.0

Fig 21: Power report

Table 7: Power comparison table

	Power	LUT's
Existing	87.12mW	242
Proposed	27mW	133

IX. CONCLUSION

The design of a Wallace tree multiplier that makes use of a reversible compressor, a full adder, and a half adder is shown in this work. This research demonstrates that the power consumption performance generated by the Wallace tree multiplier may be improved by using reversible gates. The Verilog programming language is used to implement the Wallace tree multiplier architecture. The Xilinx ISE design suite 13.2 used for simulations and synthesises results.

X. ACKNOWLEDGMENT

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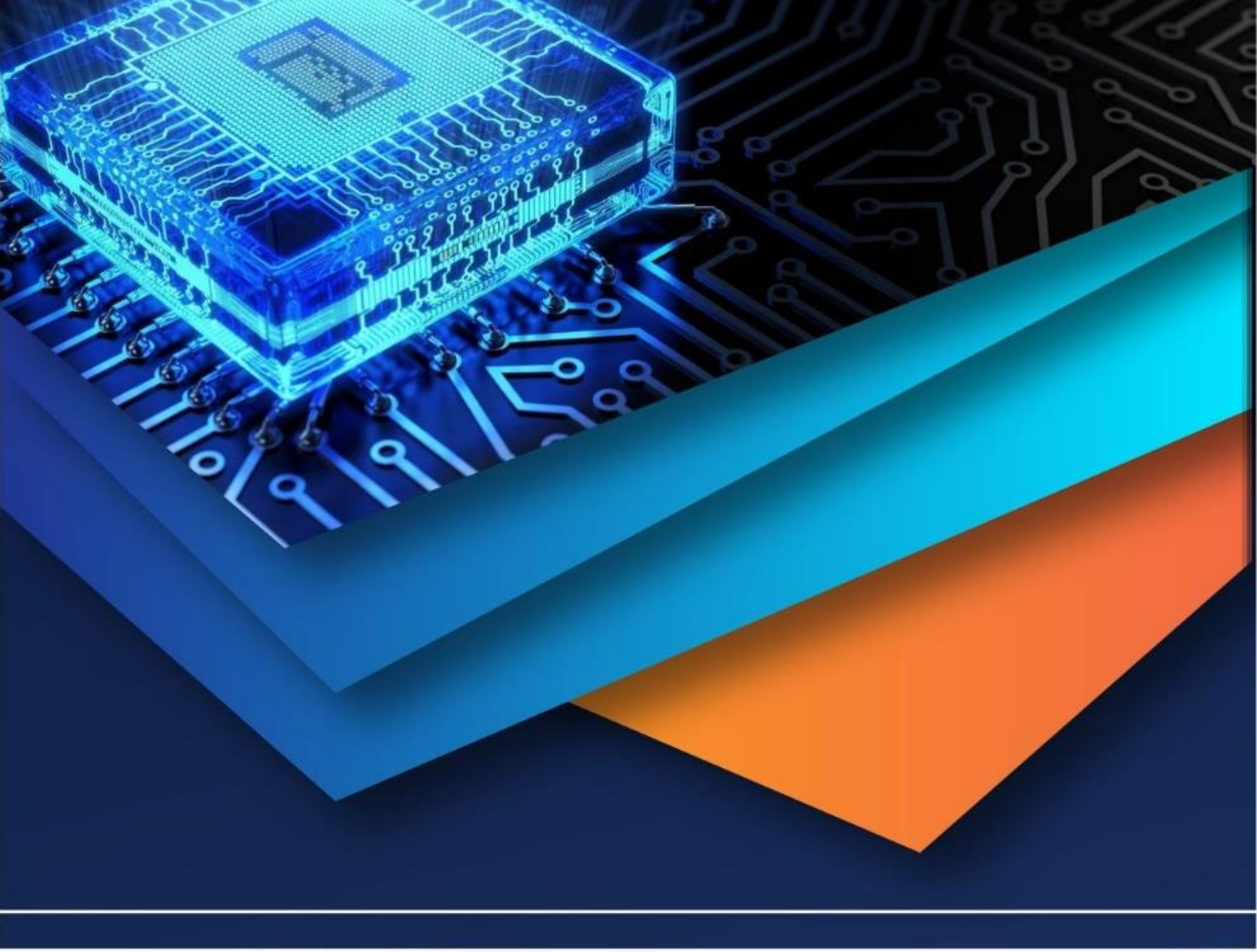
REFERENCES

[1] L. Dadda, ''Some schemes for parallel multipliers,'' Alta Frequenza, vol. 34, no. 5, pp. 349–356, Mar. 1965.
[2] C. S. Wallace, ''A suggestion for a fast multiplier,'' IEEE Trans. Electron. Comput., vol. EC-13, no. 1, pp. 14–17, Feb. 1964.
[3] Z. Wang, G. A. Jullien, and W. C. Miller, ''A new design technique for column compression multipliers,'' IEEE Trans. Comput., vol. 44, no. 8, pp. 962–970, Aug. 1995.
[4] O. Akbari, M. Kamal, A. Afzali-Kusha, and M. Pedram, ''Dual-quality 4:2 compressors for utilizing in dynamic accuracy configurable multipliers,'' IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 4, pp. 1352–1361, Apr. 2017.
[5] D. Esposito, A. G. M. Strollo, E. Napoli, D. De Caro, and N. Petra, ''Approximate multipliers based on new approximate compressors,'' IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 12, pp. 4169–4182, Dec. 2018.
[6] K. Manikantta Reddy, M. H. Vasantha, Y. B. Nithin Kumar, and D. Dwivedi, ''Design and analysis of multiplier using approximate 4- 2 compressor,'' AEU Int. J. Electron. Commun., vol. 107, pp. 89–97, Jul. 2019.
[7] P. J. Edavoor, S. Raveendran, and A. D. Rahulkar, ''Approximate multiplier design using novel dual-stage 4:2 compressors,'' IEEE Access, vol. 8, pp. 48337–48351, 2020.
[8] A. Gorantla and P. Deepa, ''Design of approximate compressors for multiplication,'' ACM J. Emerg. Technol. Comput. Syst., vol. 13, no. 3, p. 44, May 2017.
[9] A. G. M. Strollo, E. Napoli, D. De Caro, N. Petra, and G. D. Meo, ''Comparison and extension of approximate 4-2 compressors for lowpower approximate multipliers,'' IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 9, pp. 3021–3034, Sep. 2020.
[10] N. Van Toan and J.-G. Lee, ''FPGA-based multi-level approximate multipliers for high-performance error-resilient applications,'' IEEE Access, vol. 8, pp. 25481–25497, 2020.
[11] Mahalakshmi, K. S., Hajeri, S., Jayashree, H. V., & Agrawal, V. K.. "Performance estimation of conventional and reversible logic circuits using QCA implementation platform". 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT). Aug .2016

[12] Yugandhar, K., Raja, V. G., Tejkumar, M., & Siva, D. “High Performance Array Multiplier using Reversible Logic Structure”. 2018 International Conference on Current Trends Towards Converging Technologies (ICCTCT).Nov.2018.
[13] Ykuntam, Y. devi, Pavani, K., & Saladi, K. “Design and analysis of High speed wallace tree multiplier using parallel prefix adders for VLSI circuit designs.” 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT).Oct 2020
[14] He, Y., Yi, X., Zhang, Z., Ma, B., & Li, Q. A Probabilistic Prediction-Based Fixed-Width Booth Multiplier for Approximate Computing. IEEE Transactions on Circuits and Systems I. Vol: 67, December 2020.
[15] Kyung-Wook Shin &Heung-Woo Jeon.” High-speed complex-number multiplications based on redundant binary representation of partial products” International Journal of Electronics Vol 87, 2000.
[16] Murthy, G. R., Singh, A. K., Kumar, P. V. & Wilson, T. W.X. “Design of a Low Power and High Speed Comparator using MUX based Full Adder Cell for Mobile Communications”. American Journal of Applied Sciences, Volume 14, Jan 2017, 116-123.
[17] Batish, K., Pathak, S., & Gupta, R. “Comparative Analysis for Performance Evaluation of Full Adders Using Reversible Logic Gates”. 2018 International Conference on Intelligent Circuits and Systems (ICICS). Oct 2018.
[18] Reza Akbari-Hassanjani, Leila Dehbozorgi, Reza Sabbaghi-Nadooshan, "Designing D Flip-Flop using a 3×3 reversible gate", 2020 10th International Conference on Computer and Knowledge Engineering (ICCKE), pp.071-075, 2020.
[19] Krishna, N., Murugappan, V., Harish, R., Midhun, M., & Prabhu, E. (2017). “Design of a novel reversible nlfsr”. 2017 International Conference on Advances in Computing, Communications and Informatics (ICACCI). December 2017.
[20] Batish, K., Pathak, S., & Gupta,R. “Comparative Analysis for Performance Evaluation of Full Adders Using Reversible Logic Gates”. 2018 International Conference on Intelligent Circuits and Systems (ICICS). October 2018.



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