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Evaluation Performance of Seven Level Symmetrical and Asymmetrical Inverters

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***Abstract:** Any power electronic converter circuit that transforms DC voltage to AC voltage at the necessary output voltage and frequency is called an inverter. Higher Total Harmonic Distortion (THD), lower efficiency, higher dv/dt, and pulsing torque are caused by inverters' traditional practice of only offering two output voltage levels. Many strategies have been put forth to deal with these problems, and multi-level inverters are one successful approach. Depending on the amount of voltage levels that are available at the output, inverters are categorized as either two-level or multi-level. It is possible to create multi-level inverters utilizing cascaded, diode-clamped, and capacitor-clamped inverter topologies. Whereas the cascaded topology—also referred to as symmetrical multi-level inverters—uses several sources of the same value, the diode-clamped and capacitor-clamped topologies only use one source. An extensive analysis of the performance of both symmetrical and asymmetrical inverters is included in this work. The MATLAB Simulink environment is used for the simulation, and the inverters' respective performances are compared.*

***Keywords:** Multilevel Inverter, Asymmetrical Inverter, THD, Efficiency.*

I. INTRODUCTION

In industrial drive applications, conventional two-level inverters are becoming less and less useful because of their shortcomings, which include the necessity for more switching elements, extra switching losses, large driver circuit requirements, and high dv/dt issues. Differently topological multi-level inverters have been developed to tackle these issues. The diode-clamped, flying capacitor, and cascaded H-bridge topologies are examples of traditional topologies. Diode-clamped and cascaded H-bridge topologies are two of these that have become more popular in different applications. [1-2]The diode-clamped architecture connects capacitors in series to produce varying voltage levels with just one DC source needed. It does, however, have a voltage balancing issue. The cascaded topology, on the other hand, simplifies the design because it needs several DC sources. Voltage balancing and control circuit complexity are two issues with the flying capacitor topology. After experimenting with different configurations of these fundamental topologies, cascaded H-Bridge topologies emerged as a possible remedy[3-5]. It takes three voltage sources of identical magnitude and twelve switching devices per phase to operate a symmetrical seven-level multi-level inverter. While a symmetrical MLI requires eight switches and two voltage sources of different values for the same output, an asymmetrical seven-level MLI requires just two, meaning that it is more efficient[6-10].

II. STRUCTURE OF SYMMETRICAL SEVEN LEVEL CASCADED ML INVERTER

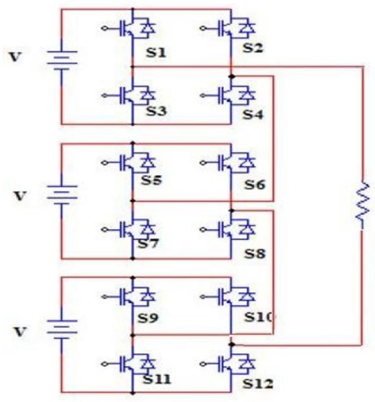
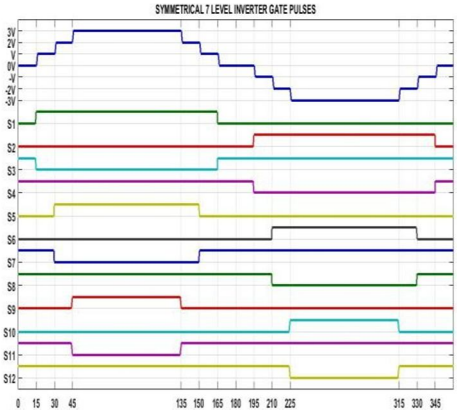


Fig.1(a) Circuit diagram



(b) Firing pulses

	3V	2V	V	0	-V	-2V	-3V
S1	1	1	1	0	0	0	0
S2	0	0	0	0	1	1	1
S3	0	0	0	1	1	1	1
S4	1	1	1	1	0	0	0
S5	1	1	0	0	0	0	0
S6	0	0	0	0	0	1	1
S7	0	0	1	1	1	1	1
S8	1	1	1	1	0	0	0
S9	1	0	0	0	0	0	0
S10	0	0	0	0	0	0	1
S11	0	1	1	1	1	1	1
S12	1	1	1	1	1	1	0

Table 1:Switching table.

Three bridges (h1, h2, and h3) cascaded in series make up the circuit diagram of the seven-level inverter depicted in Fig. 1. It also has twelve switches. Any bridge has the capacity to produce voltage V. When two bridges are operated, 2V is produced; when three bridges are run, 3V is produced; and the sum of their respective negative values results in seven levels of voltage. An advanced inverter that produces high-quality AC voltage waveforms with seven unique voltage levels is a symmetrical seven-level multi-level inverter. The symmetric distribution of these levels around zero leads to the accurate and balanced creation of waveforms. This kind of inverter greatly reduces harmonic distortion by simulating a sinusoidal waveform with several DC voltage sources or capacitors and suitable switching mechanisms. Benefits include superior power output quality, enhanced power transmission efficiency, less strain on linked devices, and enhanced power system performance overall, which makes it perfect for grid-connected power production, renewable energy systems, and motor drives. These inverters, however, are more complicated and call for higher performance switching devices, sophisticated control schemes, and additional components. In conclusion, a symmetrical seven-level multi-level inverter is an effective solution for applications requiring high-quality power conversion and transmission since it reduces harmonic distortion and improves power quality. Power semiconductor devices and other components are arranged in a certain way to provide the seven voltage levels that are needed in the output waveform while building a symmetrical seven-level multi-level inverter. This inverter is constructed using a symmetrical cascaded H-bridge topology by joining three single full bridge inverters in series. Three equal-amplitude voltage sources are needed for each bridge, which is made up of four switches (IGBTs in this example) with anti-parallel diodes.

Twelve switches in total and three voltage sources are needed for this design. It is a more traditional technique, but it is simpler than other topologies because it does not require clamping diodes or capacitors. To guarantee the inverter generates high-quality and efficient waveforms for applications such as motor drives and renewable energy systems, meticulous attention to component selection, circuit layout, and control algorithms is required throughout construction and design. The switching states of proposed inverter are as given in the Table 1 above. In the table, 1 indicates the switch is in ON state and 0 shows the switch is in OFF state.

For the voltage level 3V the switches S1, S4, S5, S8, S9 and S12are in ON state and switches S2, S3, S6, S7, S10 and S11 are in OFF state. For the voltage level 2V the switches S1, S4, S5, S8, S11 and S12are in ON state and switches S2, S3, S6, S7, S9 and S10 are in OFF state. For the voltage level V, the switches S1, S4, S7, S8, S11and S12are in ON state and switches S2, S3, S5, S6, S9 and S10 are in OFF state. For the voltage level 0V the switches S3, S4, S7, S8, S11and S12 are in ON state and switches S1, S2, S5, S6, S9 andS10 are in OFF state. For the voltage level -V the switches S2, S3, S7, S8, S11 and S12 are in ON state and switches S1, S4, S5, S6, S9 and S10 are in OFF state. For the voltage level -2V the switches S2, S3, S6, S7, S11and S12 are in ON state and switches S1, S4, S5, S8, S9 and S10 are in OFF state. For the voltage level -3V the switches S2, S3, S6, S7, S10 and S11 are in ON state and switches S1, S4, S5, S8, S9 and S12 are in OFF state.

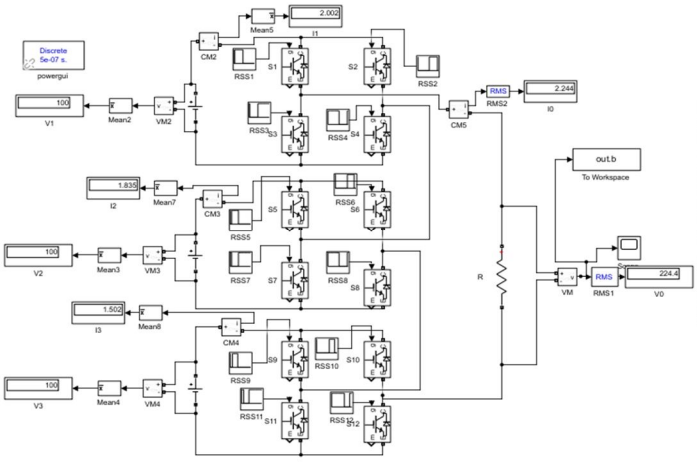


Fig.2(a): Simulation circuit diagram

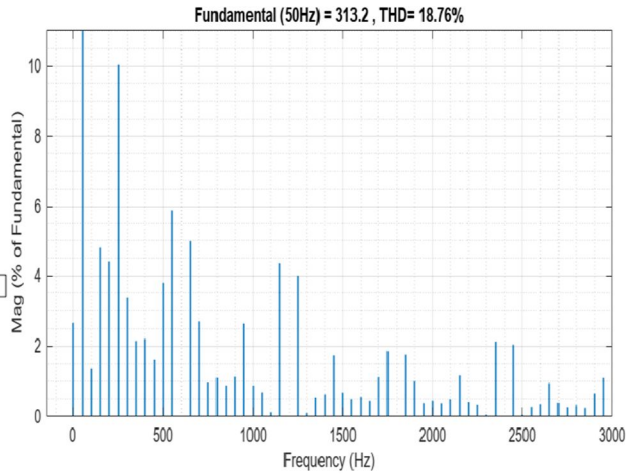


Fig.(b): Total Harmonic Distortion of output voltage

The output voltage and total harmonic distortion (THD) of a symmetrical seven-level multi-level inverter are displayed in the fig 2.The symmetrical seven-level multi-level inverter can produce a waveform that is nearly sinusoidal in shape, as shown in fig.1(b), but there is still a sizable amount of harmonic content (18.76% THD). To ensure that connected loads operate efficiently and to improve power quality, this harmonic distortion needs to be reduced. Improved component selection, improved control tactics, and harmonic filtering approaches can help achieve.

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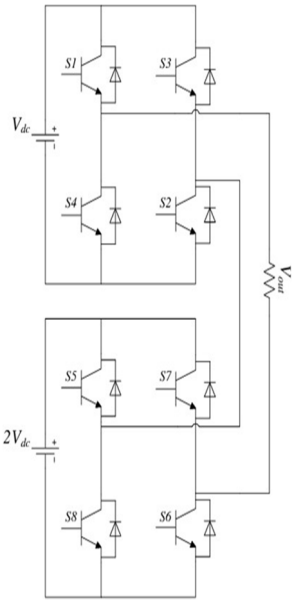
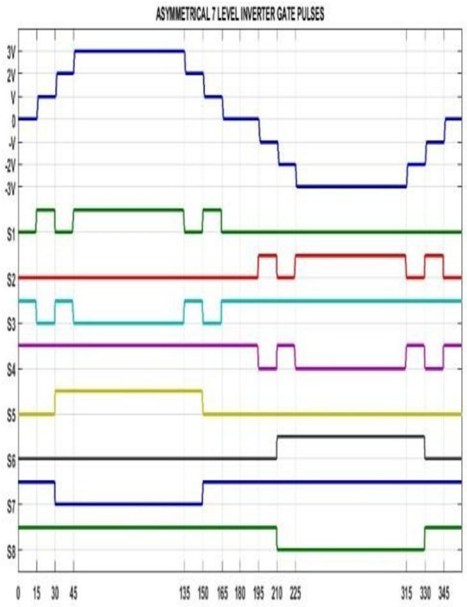
III. OPERATION OF ASYMMETRICAL INVERTER

The circuit diagram of seven-level asymmetrical inverter which has eight switches, four in upper bridge and four in lower bridge is depicted in Fig.3. The upper bridge is supplied with voltage V_{dc}, the lower bridge is supplied with voltage $2V_{dc}$, V_{dc} and $2V_{dc}$ are unequal voltages that is why the name asymmetrical. The two bridges are cascaded to each other, so when the upper bridge is operated V_{dc} is appeared at load, when lower bridge operates $2V_{dc}$ is appeared, $V_{dc} + 2V_{dc}$ is appeared when two bridges are operated, zero is appeared when neither of the voltages appeared across load and their respective negative voltages which makes it seven levels.

An asymmetrical seven-level multilevel inverter is a power electronic device that converts direct current (DC) into alternating current (AC) at multiple voltage levels. Unlike conventional multilevel inverters with equal voltage levels, asymmetrical inverters use different voltage magnitudes to achieve higher voltage levels with improved efficiency and reduced harmonic distortion.

An asymmetrical seven-level multilevel inverter achieves seven distinct voltage levels using IGBTs or MOSFETs, with unequal voltage magnitudes that enhance performance, leading to better efficiency and reduced harmonic distortion compared to symmetrical inverters. An asymmetrical seven-level multilevel inverter offers enhanced performance by utilizing unequal voltage levels, providing efficient power conversion with reduced harmonic distortion for various electrical applications.





	3V	2V	V	0	-V	-2V	-3V
S1	1	0	1	0	0	0	0
S2	0	0	0	0	1	0	1
S3	0	1	0	1	1	1	1
S4	1	1	1	1	0	1	0
S5	1	1	0	0	0	0	0
S6	0	0	0	0	0	1	1
S7	0	0	1	1	1	1	1
S8	1	1	1	1	1	0	0

Fig.3:(a) Circuit diagram (b) Firing pulses

Table 2: switching states

The switching states of proposed inverter are as given in the Table 2 above. In the table, 1 indicates the switch is in ON state and 0 shows the switch is in OFF state. The different modes of operation of 7-level inverter are given below from Fig.3:

1) Mode I: Mode I of operation Cascaded H-Bridge model in which the voltage sources of all the two full bridges are on and provides a voltage of 3V at the load. In order to make this happen switches S1, S4, S5, S8, are switched ON.
2) Mode II: Mode II of operation Cascaded H-Bridge model in which the voltage sources of only one bridge (lower bridge) is ON and produces a voltage of 2V at the load. In order to achieve this, switches S3, S4, S5, S8, are switched ON.
3) Mode III:Mode III of operation Cascaded H-Bridge model in which the voltage sources of only one bridge is ON and provides a voltage of V at the load. To make this happen switches S1, S2, S6, S8, S10 and S12 are switched ON.
4) Mode IV:The load voltage will be zero when the switches S3, S4, S7, S8, are conducting. All the sources are disconnected from the load.
5) Mode V: When the switches S2, S3, S7, and S8 are turned ON, then the output voltage will become –V.
6) Mode VI: The switches S3, S4, S6, and S7 must be turned ON to provide an output voltage of -2V.
7) Mode VII: The output voltage -3V is produced by turning ON S2, S3, S6, and S7 where both the bridges operate.

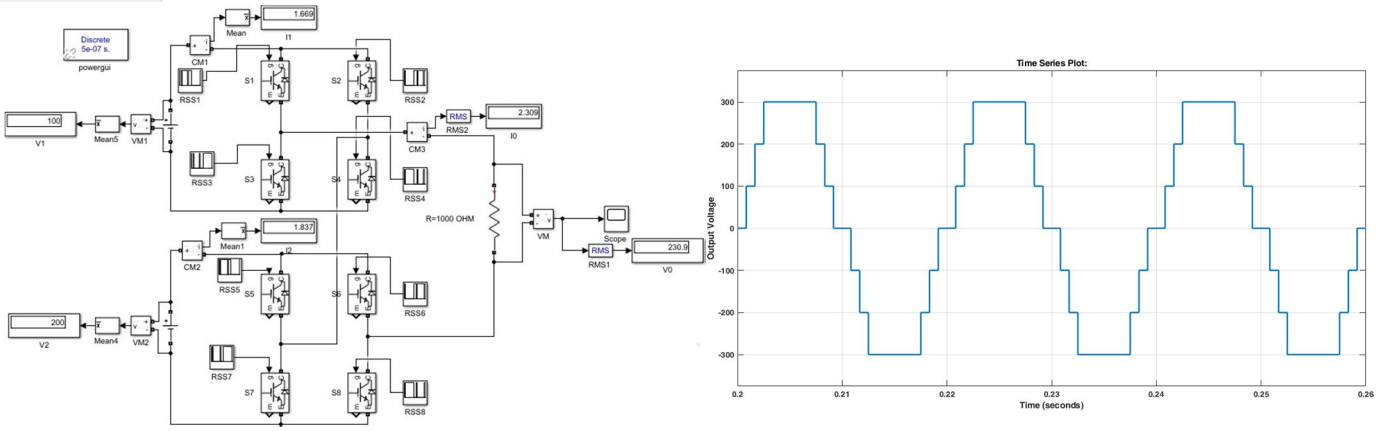


Fig.4(a): Simulation circuit diagram of Seven-Level (b) Output waveform

Because the transistors or switches in an asymmetrical inverter have an uneven switching pattern, the inverter's output waveform is usually non-uniform. Below is a general overview of what to anticipate from Fig.4: The waveform displays seven discrete voltage levels, which are attained by carefully utilizing MOSFETs or IGBTs. These levels' asymmetrical design reduces harmonic distortion and increases efficiency, which improves performance. The output voltage is shown in volts on the y-axis of the time series plot, while time is represented in seconds on the x-axis. The waveform shows the gradual transitions between various voltage levels that the inverter makes to generate an almost sinusoidal AC output. Using uneven voltage levels, an asymmetrical seven-level multilevel inverter performs better and provides effective power conversion with less harmonic distortion for a range of electrical applications.

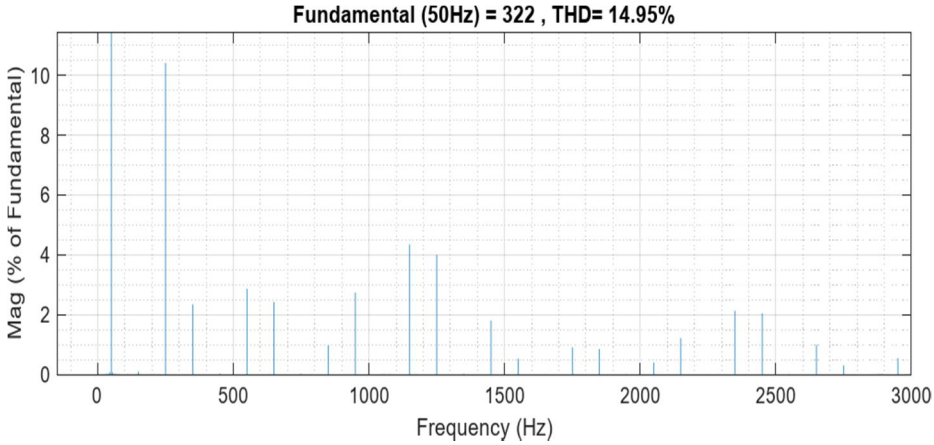


Fig.5: Total Harmonic Distortion of asymmetrical inverter output voltage

The output voltage and its total harmonic distortion (THD) of the asymmetrical seven-level multi-level inverter is shown in fig.5. As illustrated in fig.5, the asymmetrical seven-level multi-level inverter can generate a significant amount of harmonic content (14.95% THD). This harmonic distortion needs to be decreased in order to guarantee connected loads run effectively and to enhance power quality. This can be accomplished with the aid of better control strategies, harmonic filtering techniques, and component selection.

IV. SIMULATION RESULTS

The output waveforms of symmetrical and asymmetrical 7-level inverter given in the Fig.6 and Fig.7.The speed characteristics of an induction motor describe the relationship between the motor's speed and the applied load or operating conditions. The transient state performance of an induction motor with respect to speed characteristics refers to how the motor responds and stabilizes during dynamic events such as starting, sudden load changes, or disturbances.

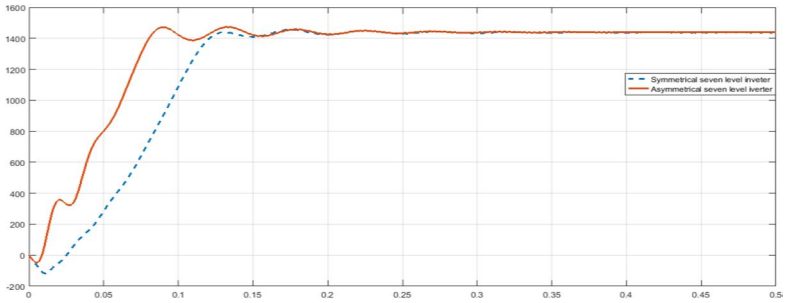


Fig.6 Transient State Performance of Induction Motor (Speed Characteristics)

The steady state performance of an induction motor with respect to speed characteristics refers to its behaviour and characteristics when operating under normal, balanced, and steady conditions. In this state, the motor has reached a stable operating point and operates at a constant speed, torque, and power output.

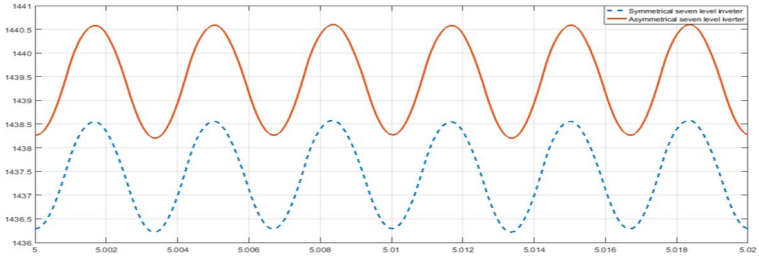


Fig.7 Steady State Performance of Induction Motor (Speed Characteristics)

V_1	I_1	V_2	I_2	V_3	I_3	V_0	I_0
100	1.835	100	2.002	100	1.502	224.4	2.244

Table 3. Source voltages and currents of symmetrical inverter

$$\%\text{Efficiency} = \frac{\textit{Output power}}{\textit{Input power}} \text{x}100$$

$$= \frac{(V_0 * I_0)}{((V_1 1 * I_1) + (V_2 * I_2) + (V_3 * I_3))}$$

$$= \%\text{Efficiency} = 94.316$$

From the calculation, the efficiency of the inverter is 94.316%.

V_1	I_1	V_2	I_2	V_0	I_0
100	1.669	200	1.837	230	2.3

Table 4. voltages and currents of asymmetrical inverter

$$\%\text{Efficiency} = \frac{\textit{Output power}}{\textit{Input power}} \text{x}100$$

$$= \frac{(V_0 * I_0)}{((V_1 * I_1) + (V_2 * I_2))} \text{x}100 \qquad \%\text{Efficiency} = 99.008$$

	symmetrical MLI	Asymmetrical MLI
%Efficiency	94.316	99.008

Table 5.The study compares the %Efficiency of asymmetrical and symmetrical MLIs.

An efficiency of 99.008% is attained by the asymmetric Multi-Level Inverter (MLI), demonstrating excellent power conversion with low losses. On the other hand, the symmetrical MLI has a little lower power conversion effectiveness, as evidenced by its lower efficiency of 94.316%. Despite its superior efficiency, the asymmetrical MLI may result in increased harmonic distortion and necessitate more intricate control techniques. The symmetrical MLI has lower efficiency but provides simpler control and greater waveform quality. Whether one prioritizes improved waveform quality and control simplicity over increased efficiency will determine which option is best.

V. CONCLUSION

In this paper, 7-level asymmetrical inverter, asymmetrical inverter with and without PWM are presented and compared based on THD parameters. Simulation results are computed using MATLAB/SIMULINK software. The eight switches are needed to produce the same output when the switches are asymmetrical. As the number of switches is reduced, switching losses also decreased which is why asymmetrical has higher efficiency. Table 5 gives the comparison of efficiency for asymmetrical MLI and symmetrical MLI. With an efficiency of 99.008%, the asymmetric Multi- Level Inverter (MLI) provides excellent power conversion at the cost of sophisticated management and possibly higher harmonic distortion. In contrast, applications that prioritize simplicity of control and waveform purity are a good fit for the symmetrical MLI, which has an efficiency of 94.316% and offers superior waveform quality and simpler control. Analysis of this paper comes to the point that asymmetrical inverter has excelled in the performance parameters showing better results which makes it ideal for various applications. From the fig.6 and 7 gives the information speed characteristics of the induction motor at two states (i) transient state (ii) steady state. For transient state the symmetrical inverter has less overshoot in the output and asymmetrical inverter has more over shoot in the output speed. From the fig.6 & 7 shows the speed characteristics of the induction motor at two main states (i) transient state (ii) steady state. For transient states the motor connected to asymmetrical seven level inverter have damping's and symmetrical seven level inverter has smooth operation in the transient state. In steady state operation the asymmetrical has less slip for the same load and the symmetrical seven level will operate in low speed.

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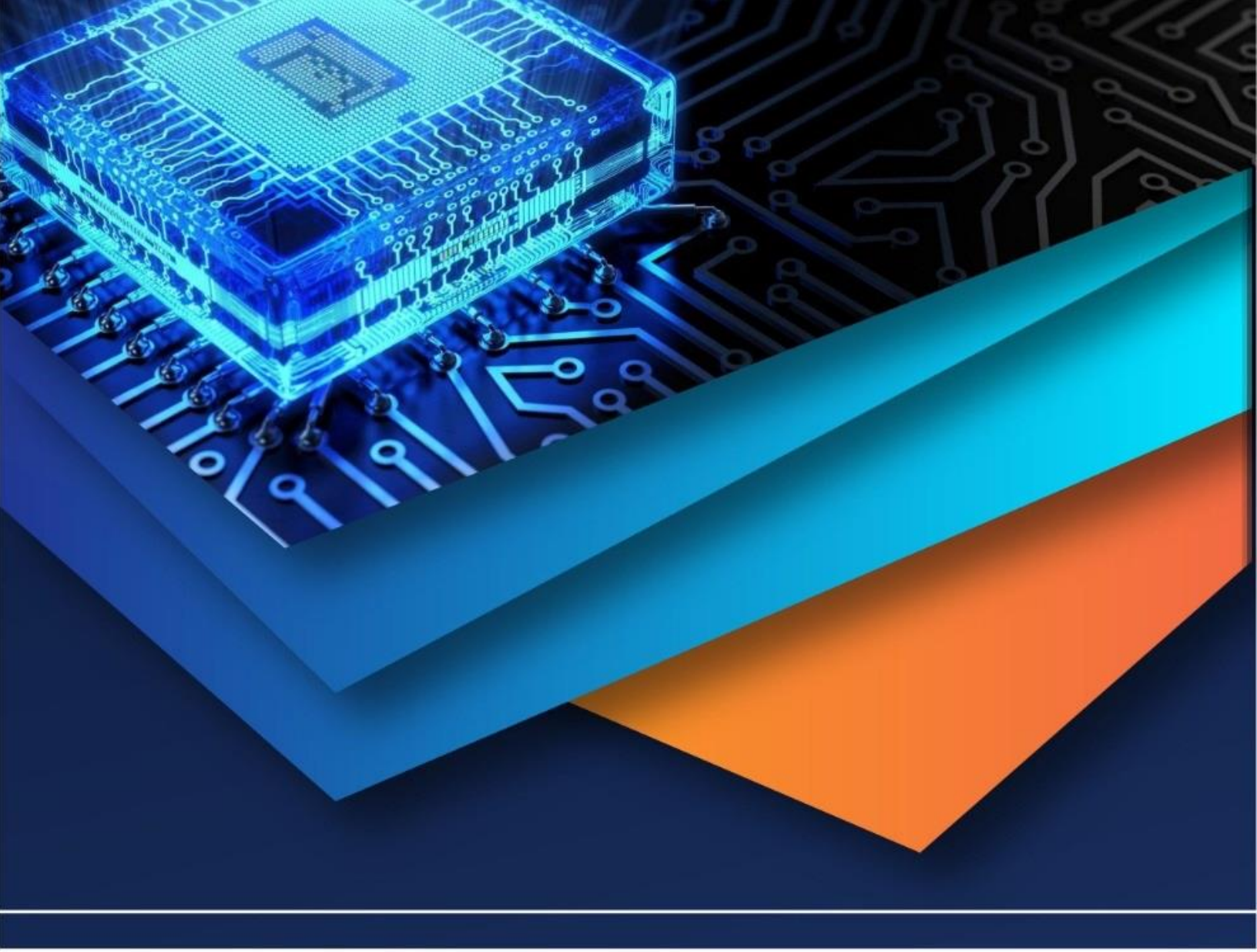

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