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Implementation of 2-bit Multiplier Circuit Using Pass Transistor Logic

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Abstract: ***In this paper, we implemented 2-bit Multiplier Circuit using Pass Transistor Logic. Pass Transistor Logic is used for high speed technology and is easy to build the basic gate structures. The developed circuit is an extension of pass transistor logic Ex-or gate. The proposed Multiplier circuit is implemented in 2x2 bit multiplier to achieve high speed, low area and less power dissipation. VLSI schematic tool and the analysis is done by using the LT Spice simulator. This paper aims at an optimization of power area and voltages of multiplier to show the better performance. The design is implemented in 0.18um CMOS technology and its functional parameters are compared and the best result is incorporated. Simulation results have been performed on LT Spice tool simulator at 1.8v and 2v supply voltage and simulations are carried out indicate the functionality of the proposed multiplier circuit compared with conventional design to verify the effectiveness and it shows the circuit has low power dissipation at high speeds.***

Keywords: Multiplier Circuit, Pass Transistor Logic, Ex-or gate, and LT Spice

I. INTRODUCTION

A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing the set of partial products, which are then summed together using binary adders. This process is similar to long multiplication, except that it uses a base-2 (binary) numeral system.

A. Binary Long Multiplication

The method taught in school for multiplying decimal numbers is based on calculating partial products, shifting them to the left and then adding them together. The most difficult part is to obtain the partial products, as that involves multiplying a long number by one digit (from 0 to 9). A binary computer does exactly the same multiplication as decimal numbers do, but with binary numbers. In binary encoding each long number is multiplied by one digit (either 0 or 1), and that is much easier than in decimal, as the product by 0 or 1 is just 0 or the same number. Therefore, the multiplication of two binary numbers comes down to calculating partial products (which are 0 or the first number), shifting them left, and then adding them together (a binary addition, of course):

This is much simpler than in the decimal system, as there is no table of multiplication to remember: just shifts and adds. This method is mathematically correct and has the advantage that a small CPU may perform the multiplication by using the shift and add features of its arithmetic logic unit rather than a specialized circuit. The method is slow, however, as it involves many intermediate additions. These additions are time-consuming. Faster multipliers may be engineered in order to do fewer additions; a modern processor can multiply two 64-bit numbers with 6 additions (rather than 64), and can do several steps in parallel.

A multiplier is a combinational logic circuit that we use to multiply binary digits. Just like the adder and the subtractor, a multiplier is an arithmetic combinational logic circuit. It is also known as a binary multiplier or a digital multiplier.

Where is the use of a multiplier?We use a multiplier in several digital signal processing applications. We use it to design calculators, mobiles, processors, and digital image processors.

How does binary multiplication work and how to design a 2-bit multiplier?

Binary multiplication works just like normal multiplication. There are four main rules that are quite simple to understand:

0 x 0 = 0
0 x 1 = 0
1 x 0 = 0
1 x 1 = 1

Suppose you have two binary digits A1A0 and B1B0, here's how that multiplication would take place.

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II. LITERATURE SURVEY

Literature survey is done on some papers firstly "A robust asynchronous 16×16-bit sub threshold multiplier using SAPTL Technique" [1] occupies more number of transistors hence there is a requirement of area optimization for the multiplier circuit. And another work is Systematic synthesis of approximate adders and multipliers with accurate error calculations [2]. Using this technology there is a need of power optimization in the design. A Hybrid 4-bit Radix-4 Low Power Booth Multiplier with High Performance [3]. No exact truth table simulation results observed in that work there is a need of timing analysis in the work. Another work ASIC Design of Reversible Multiplier Circuit [4] transistors used in the work is more hence there is a requirement of area optimization. Compressor Using Full Swing XOR Logic Gate [5]. In this work some glitches are observed in Output simulations and noise removal is required. In Design and Analysis of Approximate Multipliers For Error-Tolerant Applications [6] and in Design and Analysis of Wallace Tree Multiplier for CMOS and CPL Logic [7] and in Design of Low Power and Energy Efficient 5 X 5 Multipliers [8] needed Power dissipation to optimize.

Design of Low-Power and High Performance Radix-4 Multiplier [9] no simulation results are observed. In Design of Power Efficient Vedic Multiplier using Adiabatic Logic [10] glitches are observed in simulation results. In Low-Cost Design of Serial-Parallel Multipliers Over *GF*(*2m*) Using Hybrid Pass-Transistor Logic (PTL) and CMOS Logic [11] optimization of power is still needed. Modified Mac Unit for Low Power High Speed Dsp Application Using Multipler with Bypassing Technique and Optimized Adders [12] occupies more number of transistors hence there is a requirement of area optimization for the multiplier circuit

An ultra-low power multiplier using multi-valued adiabatic logic in 65 nm CMOS process [14] observed the circuit is complex and also having some glitches in the simulations results.

Hence there is a need of the multiplier circuit with less number of transistors occupies less space and fast operation and less power dissipation.

III. IMPLEMENTATION

A. Pass Transistor Logic

Pass transistor logic (PTL) in electronics refers to several logic families used in the design of integrated circuits. It reduces the number of transistors used to construct various logic gates by eliminating redundant transistors. Instead of being connected directly to supply voltages, transistors are used as switches to pass logic levels between nodes in a circuit. This reduces the number of active devices but has the disadvantage of decreasing the voltage difference between high and low logic levels at each stage. Each transistor in series has a lower saturation at its output than it does at its input. If several devices in a logic path are chained in series, a conventionally constructed gate may be required to restore the signal voltage to its full value. Conventional CMOS logic, on the other hand, switches transistors so that the output connects to one of the power supply rails (similar to an open collector scheme), so logic voltage levels in a sequential chain do not decrease. Circuit simulation may be required to ensure adequate performance.

B. Applications

Pass transistor logic frequently uses fewer transistors, runs faster, and consumes less power than fully complementary CMOS logic implementing the same function with the same transistors. If implemented with simple gates, XOR has the worst-case Karnaugh map and requires the most transistors of any function. By implementing the XOR using pass-transistor logic rather than simple gates, the designers of the Z80 and many other chips saved a few transistors.

C. Basic principles of pass transistor circuits

A periodic clock signal drives the pass transistor, which acts as an access switch to charge up or charge down the parasitic capacitance Cx depending on the input signal Vin. When the clock signal is active (CK = 1), the two possible operations are the logic "1" transfer (charging up the capacitance Cx to a logic-high level) and the logic "0" transfer (charging down the capacitance Cx to a logic-low level). Depending on the voltage Vx, the output of the depletion load nMOS inverter obviously assumes a logic-low or logic-high level.

D. Complementary pass transistor logic

Some authors use the phrase "complementary pass transistor logic" to describe a method of implementing logic gates that employs transmission gates made up of both NMOS and PMOS pass transistors. Other authors use the term "complementary pass transistor logic" (CPL) to describe a method of implementing logic gates that includes an NMOS-only pass transistor network followed by a CMOS output inverter.

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Other authors refer to "complementary pass transistor logic" (CPL) as a method of implementing logic gates that uses dual-rail encoding. Every CPL gate has two output wires, one for the positive signal and the other for the complementary signal, which eliminates the need for inverters.

Complementary pass transistor logic, also known as "Differential pass transistor logic," is a logic family that is designed for a specific advantage. This logic family is commonly used for multiplexers and latches.

CPL employs series transistors to select between the logic's possible inverted output values, the output of which drives an inverter. The CMOS transmission gates are made up of parallel nMOS and pMOS transistors.

E. Other Forms

There are static and dynamic types of pass transistor logic, with different properties in terms of speed, power, and low-voltage operation. The disadvantages of pass transistor logic become more apparent as integrated circuit supply voltages decrease; the threshold voltage of transistors becomes large in comparison to the supply voltage, severely limiting the number of sequential stages. Additional logic stages are required because complementary inputs are frequently required to control pass transistors.

In the above calculation, A1A0 is the multiplicand. B1B0 is the multiplier. The first product obtained from multiplying B0 with the multiplicand is called as partial product 1. And the second product obtained from multiplying B1 with the multiplicand is known as the partial product 2.

As the number of bits increases, we keep shifting each successive partial product to the left by 1 bit. In the end, we add the digits while keeping in mind the carry that might generate.

Based on the above equation, we can see that we need four AND gates and two half adders to design the combinational circuit for the multiplier. The AND gates will perform the multiplication, and the half adders will add the partial product terms. Hence the circuit obtained. Fig. 1 shows the calculation of 2-bit Multiplier circuit and Fig. 2 shows the Gate diagram of Multiplier Circuit and Table 1 is represented as truth table for the proposed circuit.

		A1	A0
		B1	B0
		A1B0	A0B0
A1B1		A0B1	X
A1B1+C		A0B1+A1B0	A0B0

Fig. 1 Calculation of 2-bit Multiplier Circuit

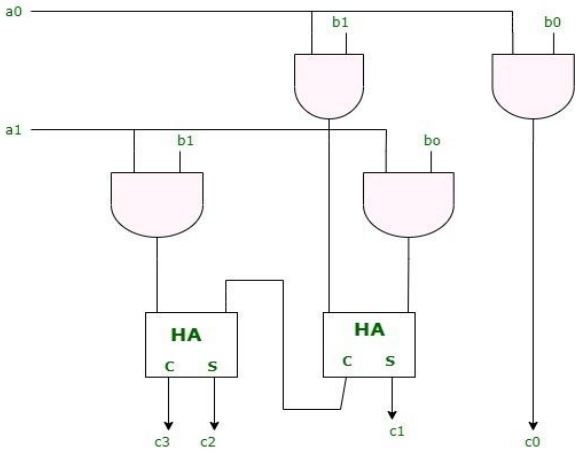

Fig. 2 Gate diagram of Multiplier Circuit

TABLE 1

Sl.No	B1	B0	A1	A0	m0	m1	m2	m3
1	0	0	0	0	0	0	0	0
2	0	0	0	1	0	0	0	0
3	0	0	1	0	0	0	0	0
4	0	0	1	1	0	0	0	0
5	0	1	0	0	0	0	0	0
6	0	1	0	1	1	0	0	0
7	0	1	1	0	0	1	0	0
8	0	1	1	1	1	1	0	0
9	1	0	0	0	0	0	0	0
10	1	0	0	1	0	1	0	0
11	1	0	1	0	0	0	1	0
12	1	0	1	1	0	1	1	0
13	1	1	0	0	0	0	0	0
14	1	1	0	1	1	1	0	0
15	1	1	1	0	0	1	1	0
16	1	1	1	1	1	0	0	1

IV. RESULTS

Experimental Results are shown below

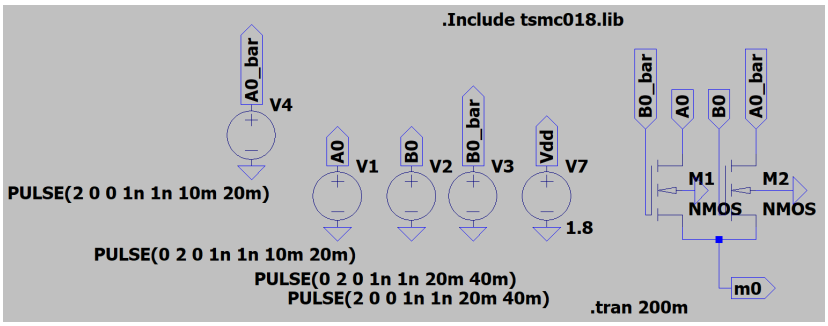

Fig. 3 Circuit diagram implementation for Ex-or Gate

Fig. 3 represents the circuit diagram for Ex-or gate Circuit.

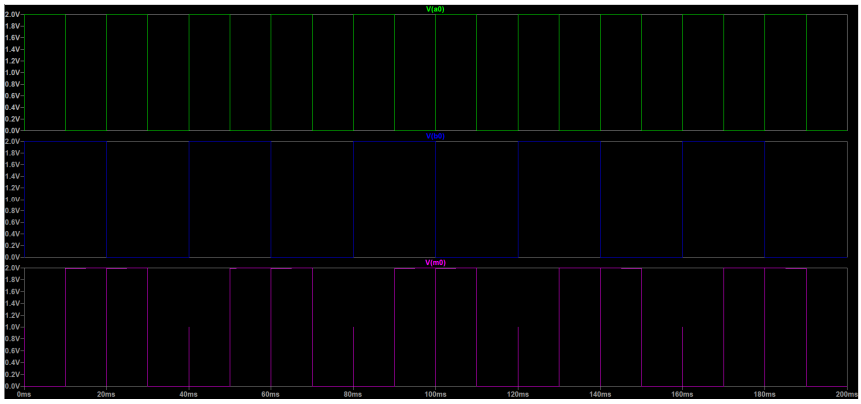

Fig. 4 Simulation results for Ex-or gate Circuit

Fig. 4 represents the result for the Simulation results for Ex-or gate Circuit.

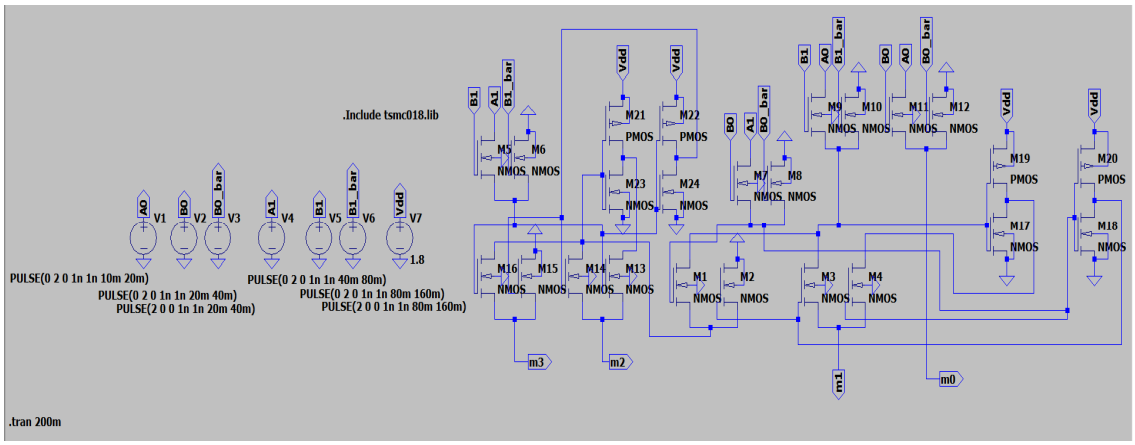

Fig. 5 Block diagram of proposed Multiplier Circuit using Pass Transistor Logic

Fig. 5 represents the result for the proposed Block diagram of Multiplier Circuit using Pass Transistor Logic.

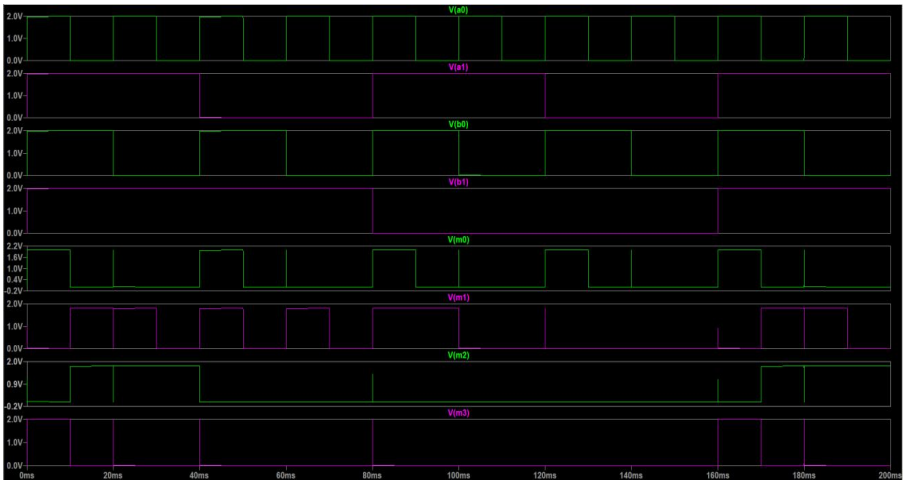

Fig. 6 Simulation results for the proposed Multiplier Circuit

Fig. 6 represents the result for the proposed Multiplier Circuit using Pass Transistor Logic.

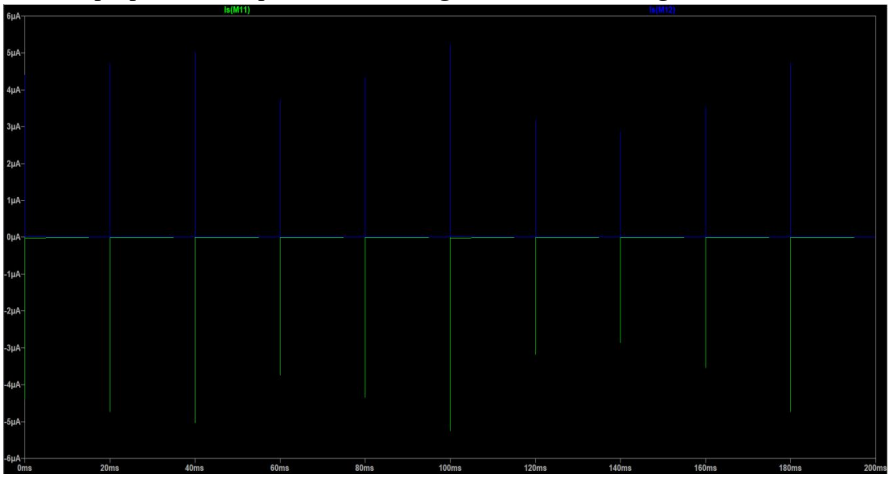

Fig. 7 Current calculation at m0 for Multiplier Circuit

Fig. 7 represents the current calculation at m0 terminal for Multiplier Circuit and observe that 5.5µA+5.5µA=11µA.

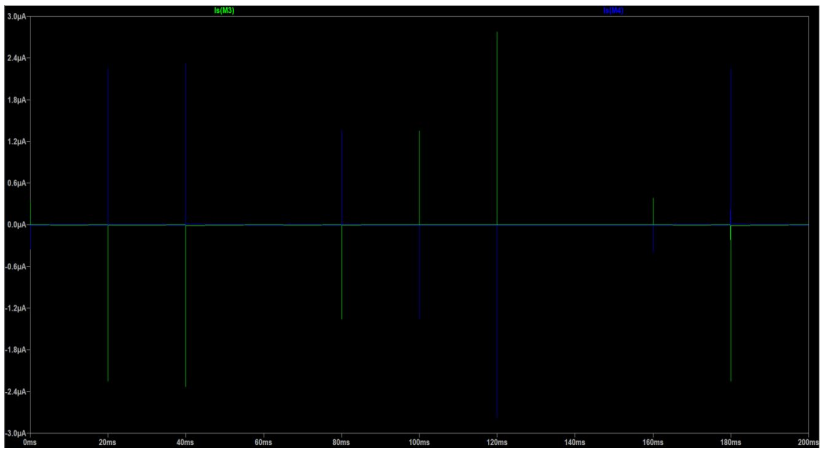

Fig. 8 Current calculation at m1 for Multiplier Circuit

Fig. 8 represents the current calculation at m1 terminal for Multiplier Circuit and observe that 2.8µ+2.8µA=5.6µA

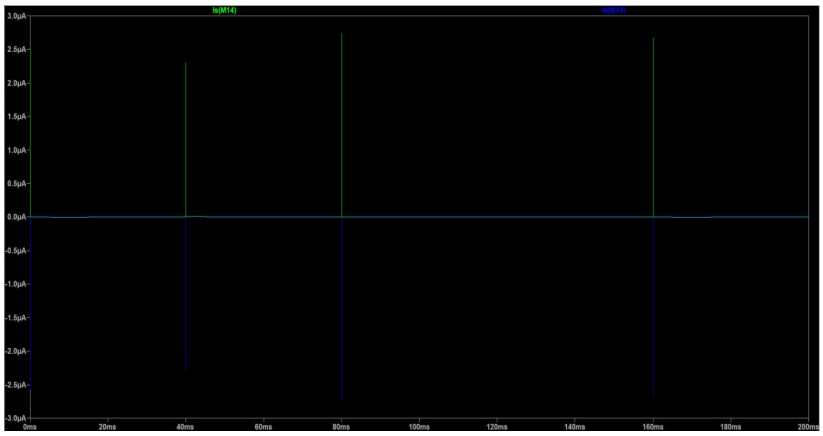

Fig. 9 Current calculation at m2 for Multiplier Circuit

Fig. 9 represents the current calculation at m2 terminal for Multiplier Circuit and observe that 2.8µ+2.8µA=5.6µA

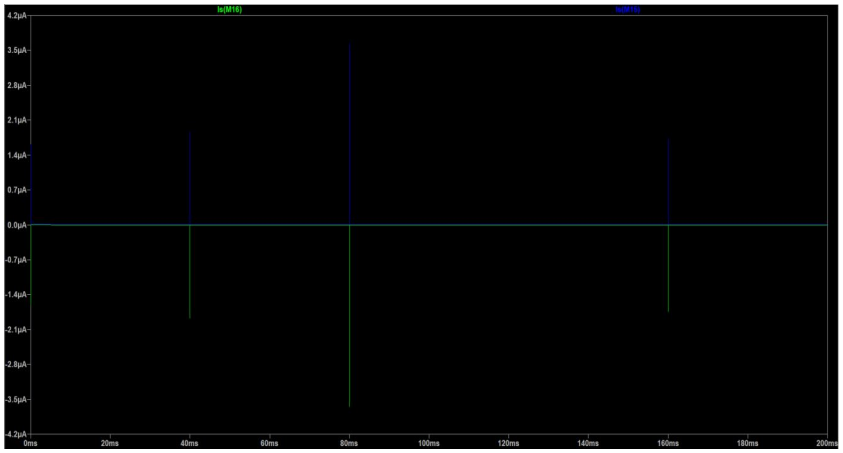

Fig. 10 Current calculation at m3 for Multiplier Circuit

Fig. 10 represents the current calculation at m3 terminal for Multiplier Circuit and observe that 3.8µ+3.8µA=7.6µA

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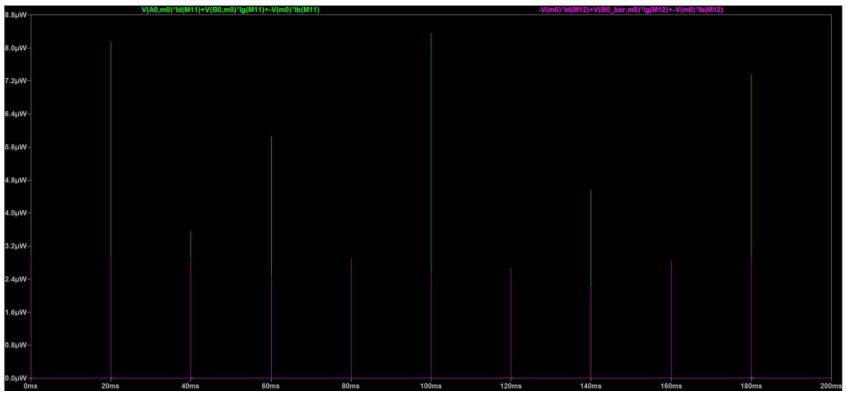

Fig. 11 Power dissipation at m0 for Multiplier Circuit

Fig. 11 represents the power dissipation at m0 terminal for Multiplier Circuit and it dissipates 8.3µWatts

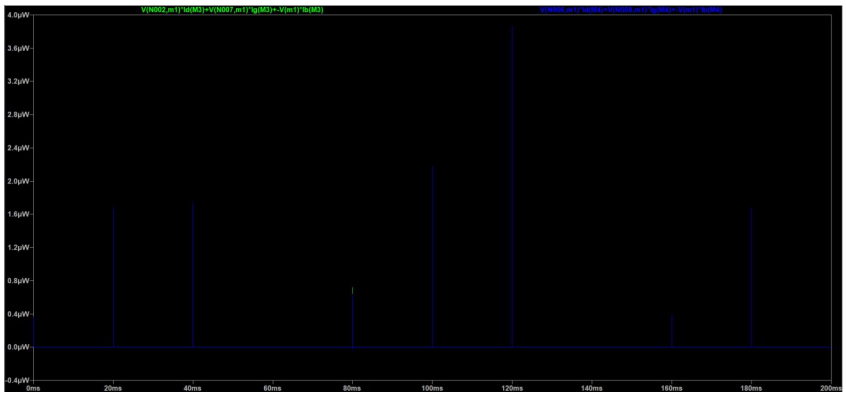

Fig. 12 Power dissipation at m1 for Multiplier Circuit

Fig. 12 represents the power dissipation at m1 terminal for Multiplier Circuit and it dissipates 3.8µWatts.

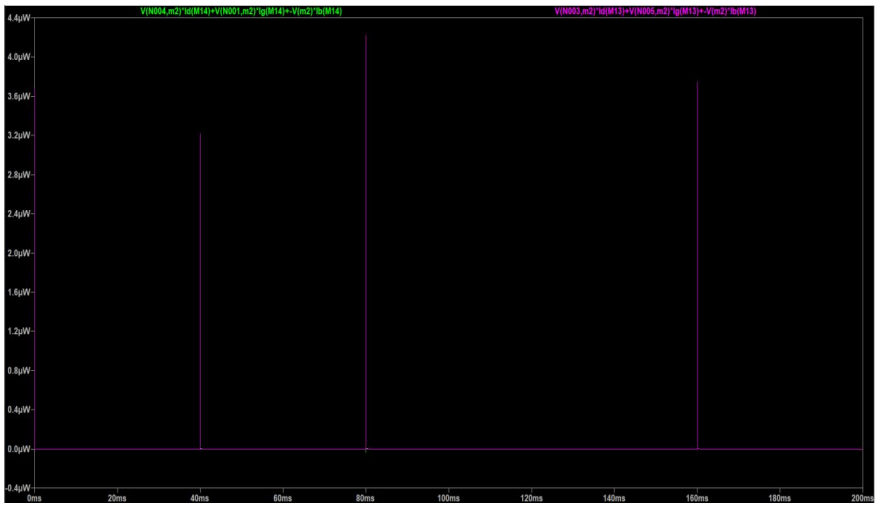

Fig. 13 Power dissipation at m2 for Multiplier Circuit

Fig. 13 represents the power dissipation at m2 terminal for Multiplier Circuit and it dissipates 4.2µWatts

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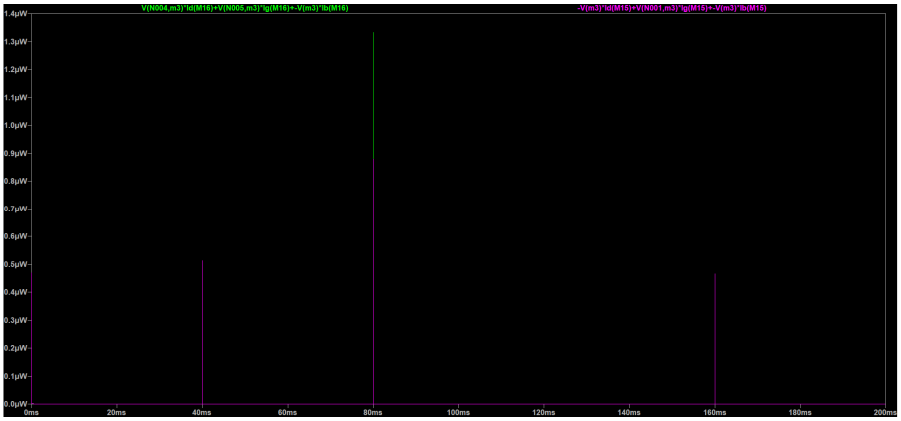

Fig. 14 Power dissipation at m3 for Multiplier Circuit

Fig. 14 represents the power dissipation at m3 terminal for Multiplier Circuit and it dissipates 1.35µWatts. the simulation results of the Multiplier circuit using pass transistor logic is observed and calculated and is submitted in this paper.

V. CONCLUSIONS

This paper provided a brief explanation of the design of a two-bit multiplier circuit using pass transistor logic. And the simulation results validated its functionality. By maximizing, the output voltage values of m0, m1, m2, and m3 can be reduced to logic values of other signals. The implemented circuits have a simpler design and are expected to perform better and consume less power than the existing full adder circuit models. Our proposed design has demonstrated a significant improvement in area, voltages, current, and power, and further improvements can be made to reduce these as well. Whereas the existing adders exhibit very little distortion. The implemented design is used for future analysis as well as 4-bit and 8-bit design Multiplier, however, the goal of this implementation is used to design the sub-blocks in ALU.

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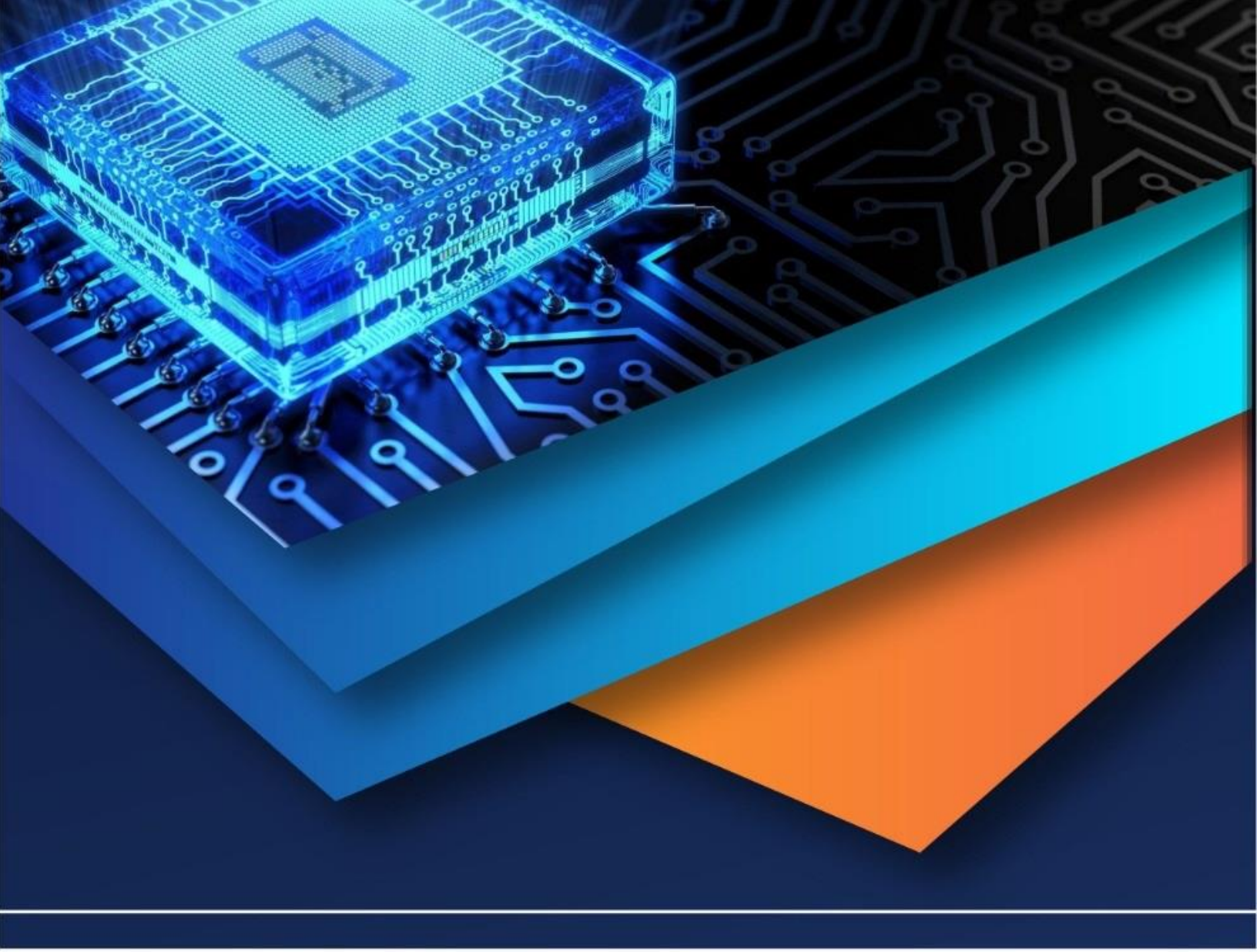

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