iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 12 **Issue:** IV **Month of publication:** April 2024

DOI: https://doi.org/10.22214/ijraset.2024.60486

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue IV Apr 2024- Available at www.ijraset.com

Low Drop-Out Regulator

Jagadish Shrishail Kalaghatagi[1], Sphoorti K. Kurandwad[2], Nikhita Jagadeesh Battur[3], Vyas R Murnal[4]
[1, 2, 3]*Student, Department of Electronics and Communication Engineering,* [4]*Assistant Professor, SDM College of Engineering and Technology Dharwad, India*

Abstract: ***The Low Dropout Regulator (LDO) is a kind of linear voltage regulator that uses transistors as variable impedance components to regulate the voltage and current. Due to its low noise and quick transient response, it is often deployed in portable equipment. We will develop, simulate, and analyse a low-dropout regulator in this project. The regulator is based on the traditional seven-pack approach, which reduces the number of components, simplifies the design, and also reduces power consumption. The system is developed and simulated in the cadence virtuoso environment at the 90 nm cmos scale of technology. It describes a three to five volt, 100 millivolt low dropout regulator. The experimental findings demonstrate that a minimal voltage drop may be achieved by combining a two-stage operational amplifier with a bandgap voltage reference, as well as a feedback element and a pass device.***

Keyword: LDO (Low Dropout), SoC (System on Chip), BGR (Bandgap Reference), CTAT (Complementary To Absolute Temperature), PTAT (Proportional To Absolute Temperature)

I. INTRODUCTION

Low dropout voltage regulator is basic building block of portable handheld electronic devices as well as automotive industry. The constant output voltage is generated by regulator by using a reference voltage. Reference voltage should be independent of process, voltage, and temperature variation. Increasing demand of portable handheld battery-operated devices forced the sub circuit to operate in low voltage high current efficiency condition for better battery lifetime. Battery life is determined by quiescent current. As VLSI technology is getting mature integrated power management for SOC is required. Miniaturized and fully on chip regulator voltage regulator should be stable for a wide range of load variation and have high PSRR over a wide frequency range. Basics of low drop out regulator, its market demand and motivation for the design is discussed in this paper. The design is defined to meet future regulator demand. A series low-dropout regulator (LDO) ensures a stable DC voltage [1], even when dealing with a low dropout voltage [2]. The dropout voltage refers to the difference between the input and output voltages at which the regulator ceases to effectively regulate. In this proposed work, a MOS transistor is positioned in series between the input and output, acting as a variable resistor to control the output voltage [3]. The feedback regulator monitors the output voltage and compares it with a reference voltage. Any difference detected generates an error signal in the comparator, which adjusts the impedance of the pass transistor, thereby regulating the output voltage.

For proper operation, the input voltage to the regulator must exceed the output voltage by at least the dropout voltage to remain within the regulation range. Additionally, the output impedance should be kept low [5] for optimal performance.

LDOs can be categorized based on various parameters, such as high power or low power, high dropout or low dropout, and output pole dominant or capless. Low-power LDOs typically offer maximum output currents in the range of mA, making them suitable for use in portable handheld electronic devices [4]. The different design options for LDO are mentioned below:

A. Voltage buffered LDO

After the error amplifier, a voltage buffer drives the gate capacitance of the pass element, increasing slew rate and providing excellent transient responsiveness.

B. LDO with Feedback Current Amplifier

The current amplifier is used in this LDO. The output current is sensed by the current amplifier, which generates extra current and raises the slew rate at the gate of the pass element.

C. LDO with Miller Capacitance

Miller capacitance is used in this design. We may enhance phase margin and hence stability by changing an exact capacitance value.

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue IV Apr 2024- Available at www.ijraset.com

II. SYSTEM DESIGN

The design of LDO in the proposed work is mentioned below:
We choose one of the best solutions based on how well it works and how simple it is to apply.

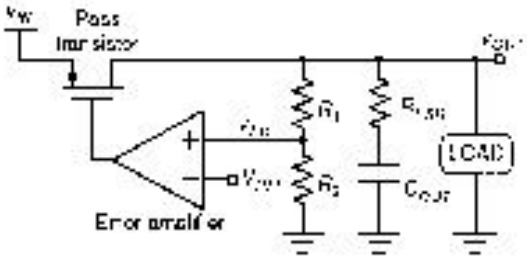


Fig. 1 LDO

The components that make up proposed Low Drop Out Regulator are as follows:

1) *Voltage Reference:* It is the beginning point of any regulator since it determines the error amplifier's operating point. A band-gap-type voltage-reference is often used since it allows for low supply voltage operation.
2) *Error Amplifier*: The primary criterion for the error amplifier's design is that it draw as little current as feasible. Because the pass transistor's gate capacitance is high, the amplifier's output resistance must be as low as feasible. One input of the error amplifier is the output voltage downscaled by the voltage divider network, whereas the other input is really the reference voltage.
3) *Feedback:* The error amplifier uses the resistive voltage divider feedback to scale down the output voltage so that it may be compared to the reference value.
4) *Pass Element:* The error amplifier in the feedback regulates the pass element in the LDO, which is responsible for moving current from input to load. As pass elements, MOSFETs (PMOS as well as NMOS) are often utilised. A typical LDO configuration with a PMOS pass element is shown in the picture below.

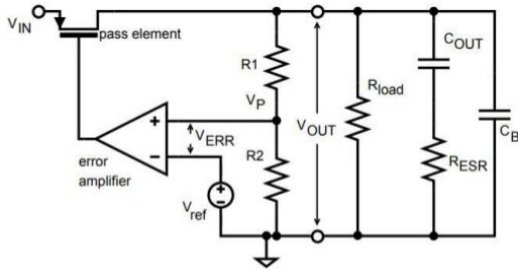


Fig. 2 LDO with PMOS pass element

The PMOS pass element's V_{GS} is linked to V_{dd}. The minimal drain-source voltage V_{ds} is the minimum voltage needed by the PMOS transistor to remain in saturation and regulate correctly. The PMOS pass element is not suitable for applications requiring extremely low voltage.[8]

A. *Parameters of LDO*

Some of the key steady-state and transient characteristics of an LDO Regulator are:
The Dropout Voltage of the regulator is the variation between the input and output voltages of the regulator. The regulator stops regulating when the input voltage reaches the output value. Quiescent Current, otherwise known as Ground Current, is the discrepancy between the input and output currents. Low quiescent current leads to optimum efficiency in low-power systems. The efficiency of an LDO Regulator is determined by the input-to-output voltage and the quiescent current. Efficiency is determined by the following factors:

$$Efficiency = \frac{I_o V_o}{(I_o + I_q)V_i} \times 100\%$$

For a load current step or an input voltage step, it is the greatest output voltage fluctuation. The output capacitor's ESR (Equivalent Series Resistance) determines the transient responsiveness.

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue IV Apr 2024- Available at www.ijraset.com

The capacity of a regulator to maintain a desired output voltage despite changing input voltages is known as line regulation. As the load current requirement rises, the output capacitor is in charge of providing the current. As a consequence, the output voltage varies, which the feedback network detects. The error amplifier compensates by allowing greater current flow via the pass transistor. The capacity of a regulator to maintain the correct output voltage despite changing load currents is known as load regulation.

III. IMPLEMENTATION DETAILS

A. Proposed Architecture

The Capacitor-less LDO design includes many components, including an error amplifier, a voltage reference, a pass element, and a feedback network as shown in figure 1.

B. Voltage References

Voltage reference energy sources offer an energy source that is unaffected by temperature or supply voltage variations. This BGR maintains a steady reference voltage with 1.2V and just a 5 percent fluctuation. A starting circuit is also included in this design, which keeps track of the zero situation. The error amplifier's negative terminal receives the output of BGR.[6]
The balancing equation incorporating PTAT and CTAT currents is used to construct this BGR.

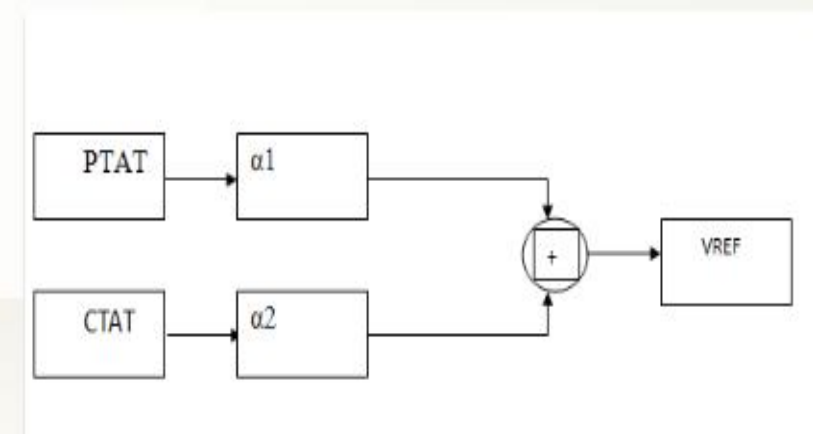


Fig 3 Block diagram of BGR

Table 1 Specifications of BGR

Sl. No.	Parameter	Calculated	Designed
1	Slope of CTAT	-1.79mV/K	-1.60mV/K
2	Slope of PTAT	86.25uV/K	85uV/K
3	Alpha1	18.82	18.82
4	Alpha2	1	1
5	Thermal Voltage(Vt)	26.06mV	26mV
6	Resistance (R2)	97.74Kilo ohm	90Kilo ohm
7	Reference voltage	1.2V	1.2V(approx.)

©IJRASET: All Rights are Reserved | SJ Impact Factor 7.538 | ISRA Journal Impact Factor 7.894 |

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue IV Apr 2024- Available at www.ijraset.com

C. Error Amplifier

One of the main blocks of an LDO is the Error Amplifier. The error voltage input, which is also the difference between the reference and feedback voltages, is amplified. A 7-pack Operational Amplifier is used as an error amplifier.[7]

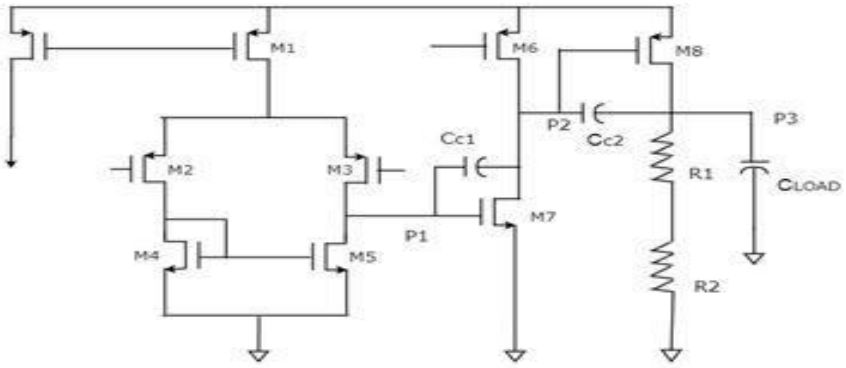


Fig. 4 Error Amplifier

Table 2 Specifications of error amplifier

Sl. No.	Parameter	Parameter symbol	Quantity
1	DC gain	Av	≥1000
2	Gain*Bandwidth	GB	30MHz
3	Power dissipation	Pdiss	≤1.2mW
4	Load capacitance	Cl	2pf
5	Slew Rate	SR	≥20V/us
6	Output Voltage range	Vint	± 2V
7	Input common mode range	ICMR	-2.5V to +2.5V
8	Positive voltage	Vdd	+2.5V
9	Negative voltage	Vss	-2.5V

D. Low Drop-Out Regulator

The proposed LDO is designed using the two-stage differential amplifier as the error amplifier, a voltage reference using the Bandgap Reference, a PMOS pass element, and a voltage divider circuit.

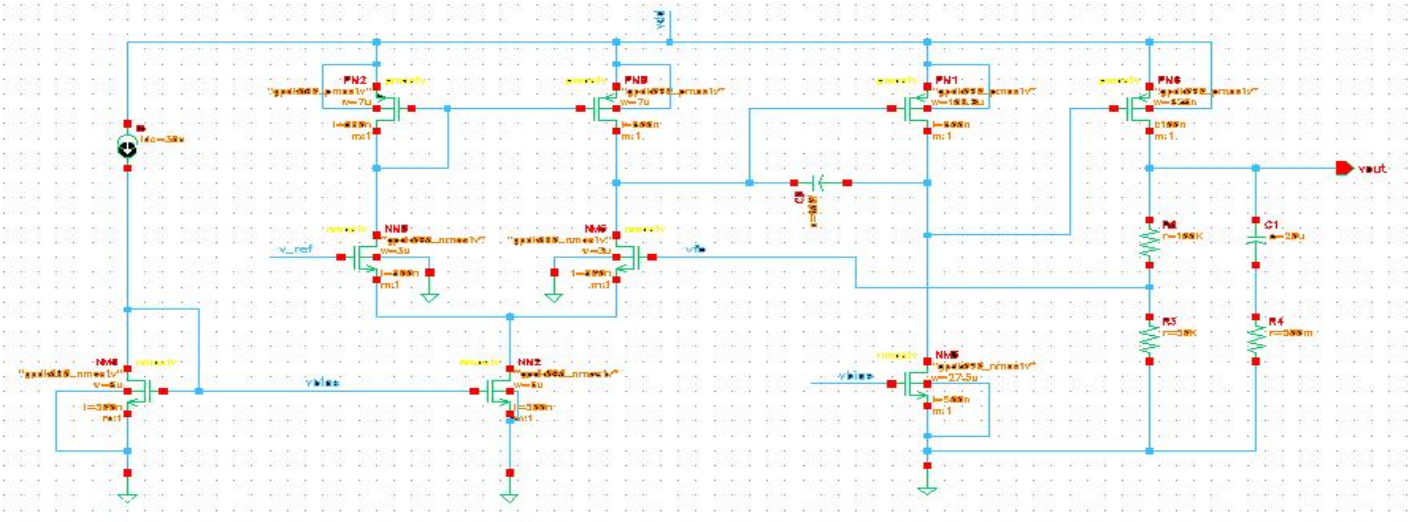


Fig. 5 Schematic of designed LDO

©IJRASET: All Rights are Reserved | SJ Impact Factor 7.538 | ISRA Journal Impact Factor 7.894 |

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue IV Apr 2024- Available at www.ijraset.com

IV. RESULTS

A. AC analysis of voltage Bandgap Reference

The AC analysis of the bandgap reference generator is shown in the figure 11. AC analysis is performed to observe the circuit output over a range of frequencies. It is observed that the output of the bandgap reference is almost constant with a 70dB gain and 0° phase for frequencies up to 500Hz. The bandgap reference generator is used as one of the inputs of the PMOS differential amplifier to bias the PMOS pass transistor at node VR. This is ideal for generating a reference voltage over a wide frequency range.

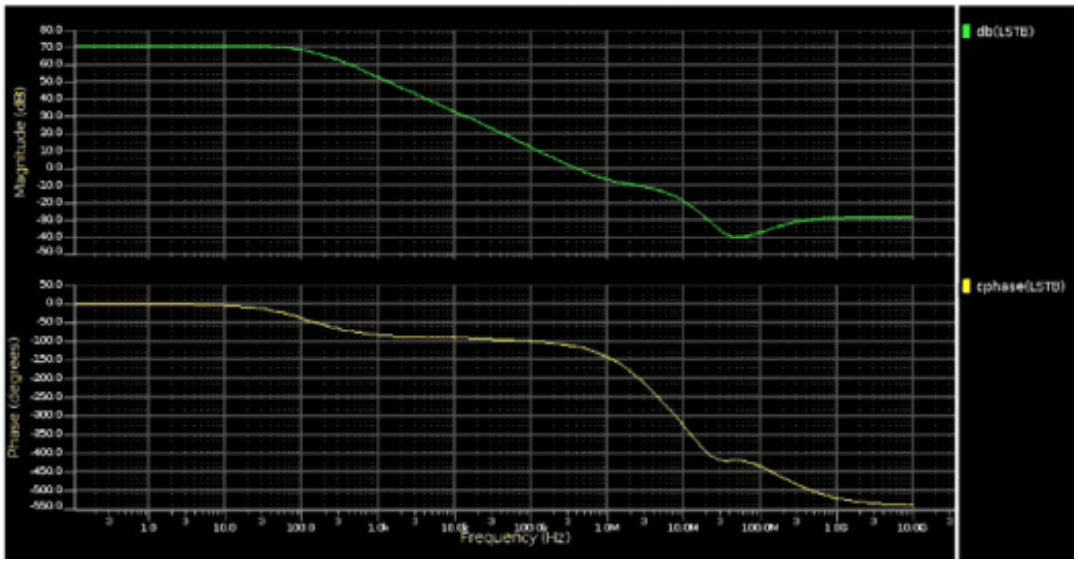


Fig. 6 AC analysis of voltage bandgap reference

B. Drop-Out Voltage

For a certain desired output voltage under certain loading conditions, different input voltages correspond to different operating regions, including the off region, drop-out region, and regulation region. Output performance varies significantly in different operating regions. The output voltage can be regulated within the allowable drop-out voltage in the regulation region. The drop-out voltage is estimated by the voltage difference between the input voltage and the output voltage when the output voltage deviates from its desired voltage by approximately 2%. Drop-out voltage is the voltage drop across the pass transistor in the regulation region.

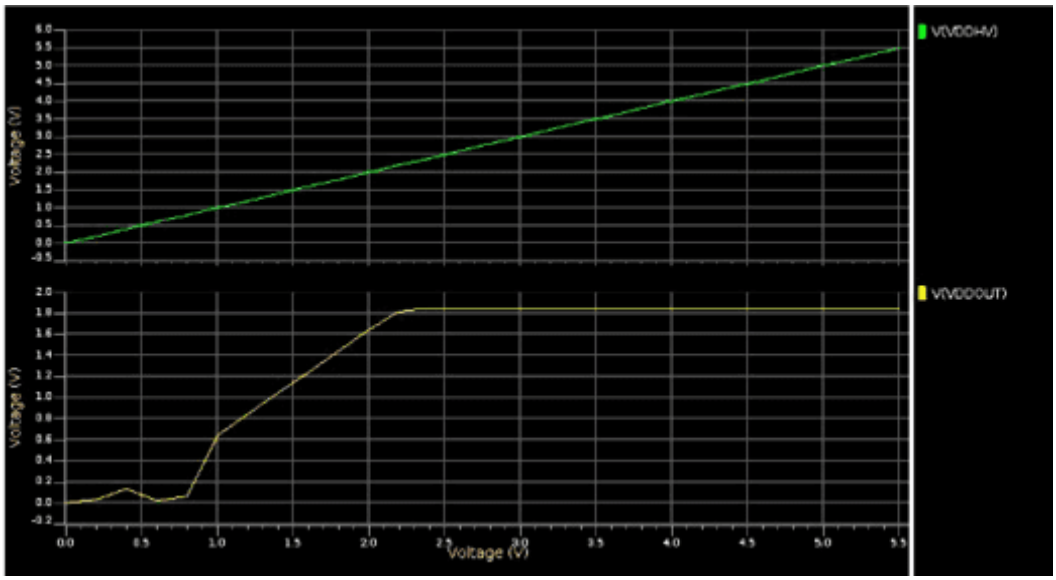


Fig. 7 Characteristic curve of input and output for Dropout analysis

©IJRASET: All Rights are Reserved | SJ Impact Factor 7.538 | ISRA Journal Impact Factor 7.894 |

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue IV Apr 2024- Available at www.ijraset.com

C. Load Regulation

The load regulation of the linear voltage regulator for a variation of load current from 0 to 80 mA in 100 nsec, with an on-chip output capacitance of 10 pF, is shown. With an increase in load current, more current flows through the NMOS pass transistor, hence the voltage drops across the output impedance will also be more, which can be observed from the plot. By varying the on-chip capacitor realized by a programmable capacitor bank from 1 pF to 100 nF, the output voltage variation decreases and becomes constant for higher capacitance. With an increase in output capacitance, the peak-to-peak output voltage variation reduces from 158 mV to 128 mV. Also, the settling time for overshoot and undershoot reduces to within 500 nsec.

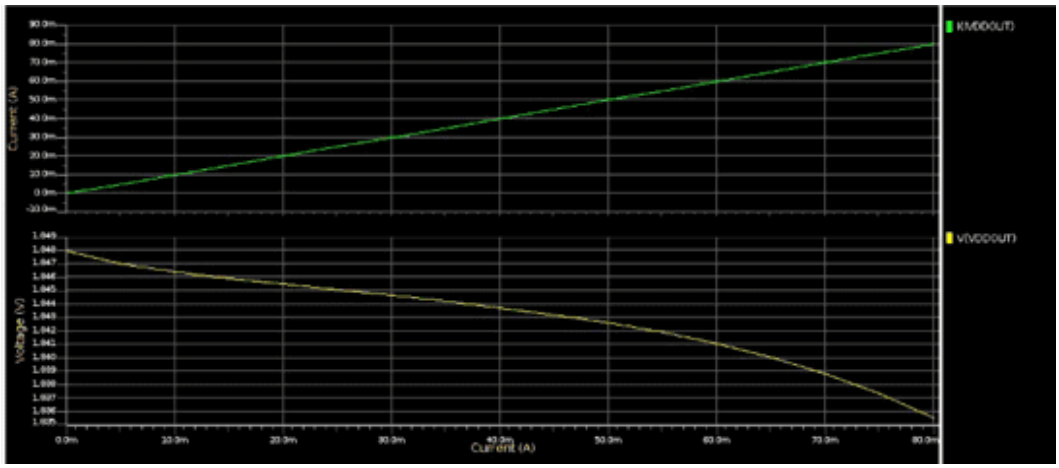


Fig. 13 Load regulation curve

D. Load Transient

To test the dynamic performance of the regulator, transient performance analysis is used. Load transient is defined as the output voltage variation corresponding to a step change in load current. Load transient mainly depends on the output capacitance associated with the regulator and its bandwidth. The load transient response of the sub-unity gain positive feedback linear voltage regulator for a step rise of load current from 0A to 75mA in 1µs, with an output capacitance of 1pF, is shown.

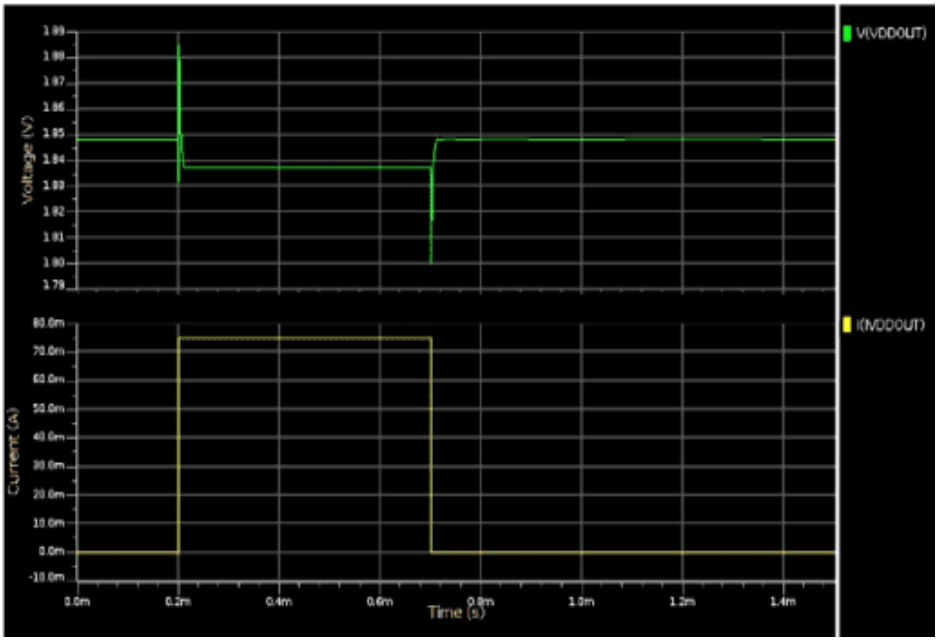


Fig. 8 Load transient plot for load current of 75mA

The worst case of output voltage variation occurs when the load current steps from 0 to the maximum rated value and vice versa.

©IJRASET: All Rights are Reserved | SJ Impact Factor 7.538 | ISRA Journal Impact Factor 7.894 |

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue IV Apr 2024- Available at www.ijraset.com

E. Line Transient

Like load transient, line transient is also a dynamic performance measurement of an LDO linear voltage regulator. Line regulation is the measurement of the regulator output voltage variation with respect to a step rise in input supply for a constant load current.

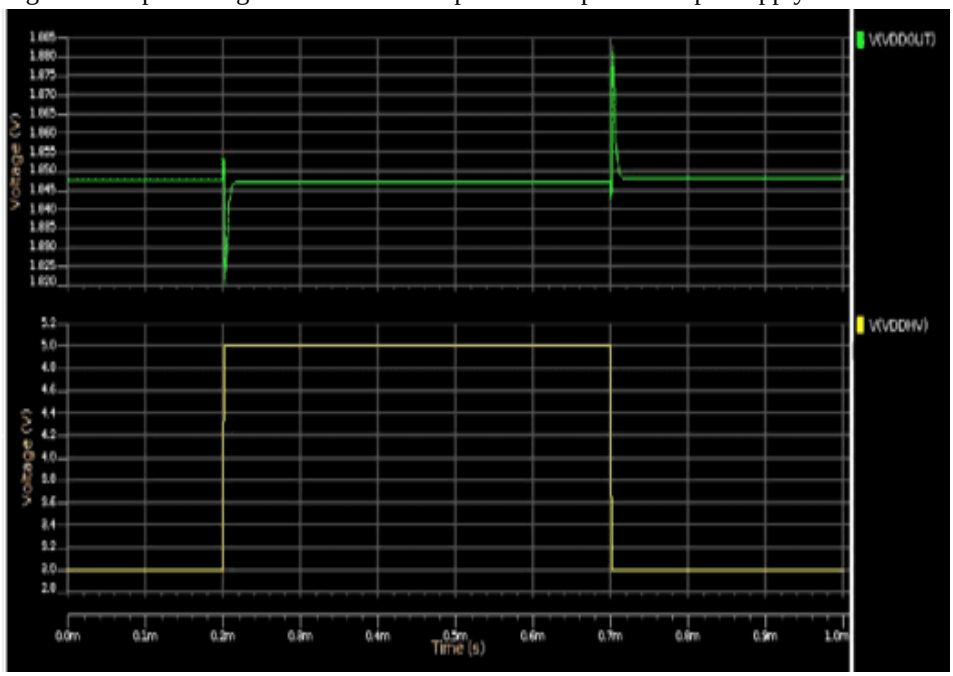


Fig. 9 Line transient plot for input voltage of 5V

F. Regulator Stability

Loop gain considering all parasitic capacitance is used for linear regulator stability analysis. From the output waveform, it can be observed that the system gain is less than 0dB for all frequency ranges under no-load conditions. Thus, the regulator is stable. As the regulator load increases, the system gain increases compared to the no-load condition. This is because, to regulate the output voltage, loop gain should increase. However, the gain is still below 0dB, so the system stability will not be affected.

As the frequency of operation increases due to intrinsic parasitic components, the system gain decreases, but overall system stability remains the same. Because of the connection of a ballast, the system gains increase, but that will not be a deciding factor for regulator stability.

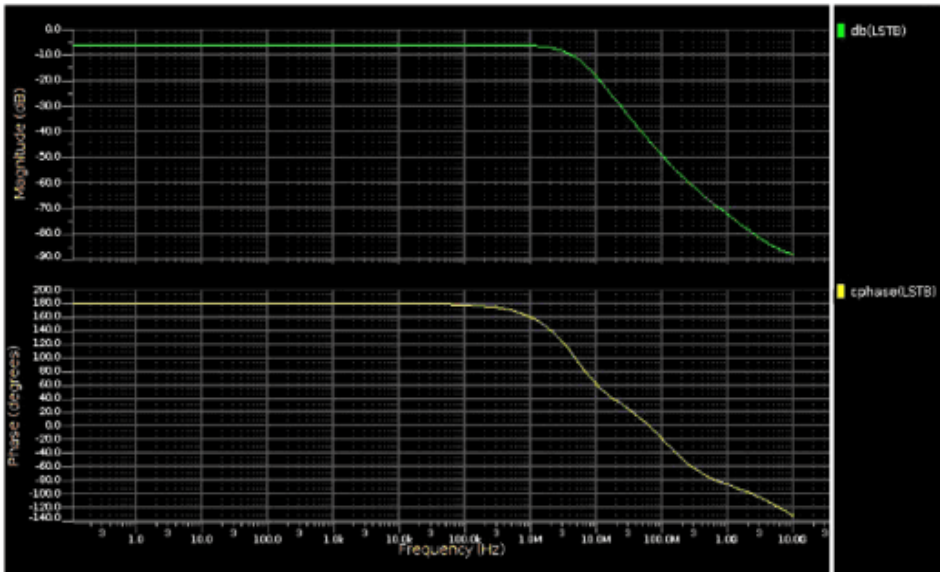


Fig. 10 Stability analysis of regulator for no load condition

©IJRASET: All Rights are Reserved | SJ Impact Factor 7.538 | ISRA Journal Impact Factor 7.894 |

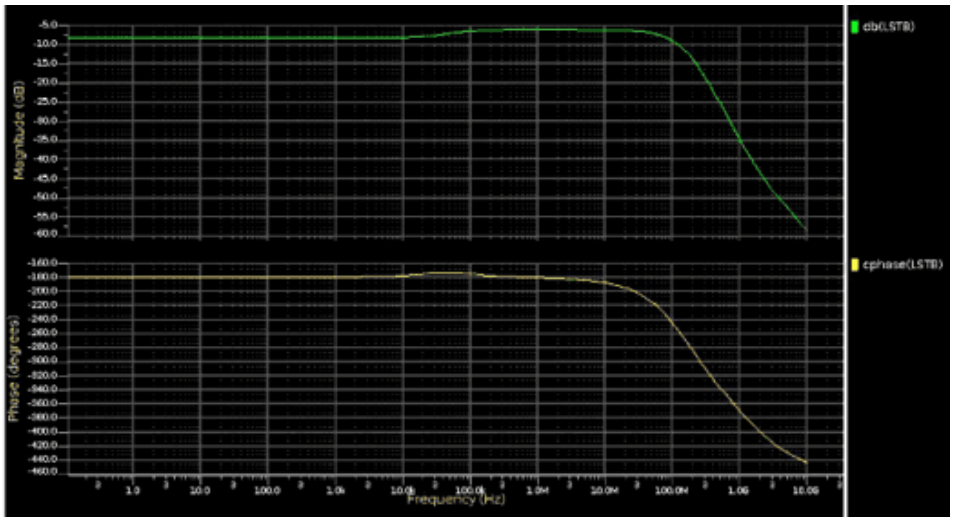


Fig. 11 Stability analysis of regulator for full load condition

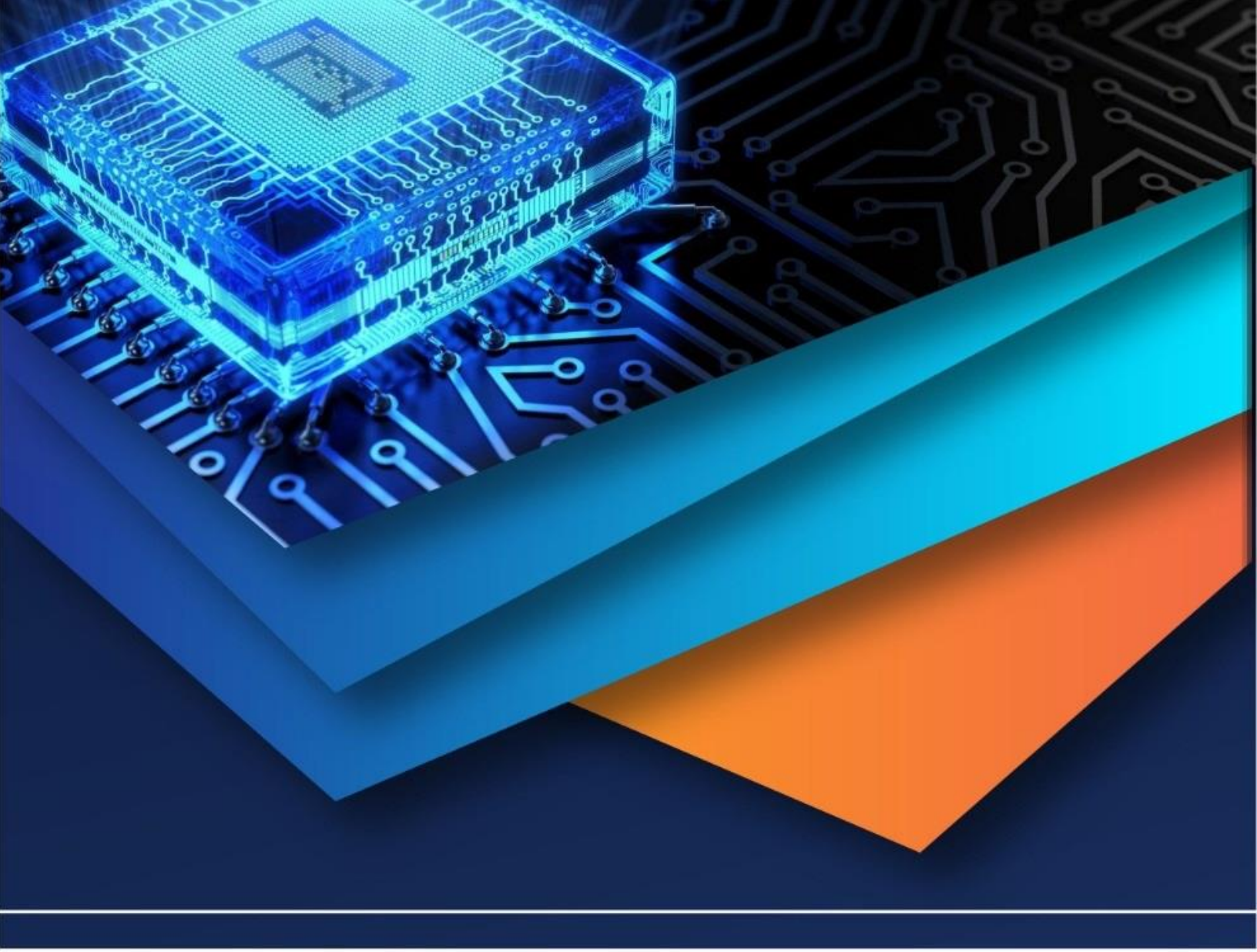
V. CONCLUSION

In the paper, initially, a brief introduction about Linear Low Drop-Out Voltage Regulator (LDO) is given along with why it is required, different topologies of linear voltage regulators, and their design considerations. After that, a brief overview of the voltage bandgap reference is given. It is observed that all nanometre linear voltage regulator design topologies are stable only for a certain output capacitor range. So, there is a great challenge to drive load blocks with different input parasitic capacitance. Any capacitor sub-unity gain positive feedback linear voltage regulator is the most efficient, effective, and stable design topology in nanometre design technology. It is observed that any capacitor sub-unity positive feedback linear voltage regulator is stable for any value of output capacitor, has a wide range of input voltage variation, small peak-to-peak output voltage variation, small chip area for the same load driving capability and output voltage. Although having all these advantages in any capacitor sub-unity gain LVR, it is observed that for the same load current, quiescent current increases, which is because of scaling down of process technology. It adversely affects the battery lifetime of portable electronic devices. But it is acceptable as both design and silicon are getting mature. Due to a small capacitor at the output and positive feedback, settling time increases. At high frequency, Power Supply Rejection Ratio (PSRR) drops, i.e., at high frequency, more noise appears at the output.

Overall, the design technique has comparable performance without any restriction on the output capacitor value. To overcome all these challenges, work is ongoing on new design topologies that provide better PSRR even at higher frequencies.

REFERENCES

[1] S. Franco, “Design with Operational Amplifier and Analog Integrated Circuits”, New York: McGraw-Hill Publishing company 1988.
[2] M. Mirovic, “Integrated Circuits: A User’s Handbook”, Reston, Virginia: Reston Publishing Company Inc 1977.
[3] P. R. Gray and R. G. Meyer, “Analysis and Design of Analog Integrated Circuits”, New York: John Willey & Sons Inc 1993.
[4] F. Goodenough, “Low Dropout Linear Regulator”, Electronic Design, PP 65-77 May 13, 1996.
[5] J H Mohammed Ismail, “CMOS High Efficiency on chip power management”, Springer Publication.
[6] Dr. Qadeer Ahmed Khan, “Power Management Integrated Circuits”, NPTEL.
[7] R. J. Milliken, J. Silva-Martínez and E. Sánchez-Sinencio, “Full On-Chip CMOS low-dropout voltage regulator,” IEEE Trans. Circuits SystI, Reg. Papers, vol. 54 PP. 1879-1890, Sep. 2007.
[8] “Power Management Technique for Integrated Circuit Design”, STMicroelectronics.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)