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Performance Analysis and Comparison of Different High-K Materials Used as Gate Dielectrics in DH-TMSG MOSFET

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Abstract: ***To overcome SCEs and provide better packing density and performance a device called Double Halo Triple Material Surround Gate MOSFET is introduced. The device is designed by the combination of gate engineering and channel engineering. The device uses a surround gate MOSFET with triple material gate employing gate material engineering which improves the gate transport efficiency by modifying electric field pattern and surface potential along channel, resulting in higher carrier transport efficiency and SCEs. To extend the use of CMOS technology beyond 14 nm node technology, new device materials are required that can enhance the performance of MOSFETs. The use of high-k materials in double gate (DG) MOSFET can triumph over the problem of power dissipation and leakage current. The further mitigation in device dimension becomes a challenging task due to the existence of unavoidable short channel effects. The introduction of gate stack and channel engineering in MOSFET devices open a new window for future generation devices. The gate dielectric materials have played a significant role in the design of novel and high performances at nanoscale of electrical devices. It can be observed that when approaching a higher value of dielectric constant, the on current increases while the subthreshold slope (SS) threshold voltage (Vth) and leakaga current reduced. The scaling of complementary metal oxide semiconductor (CMOS) transistors has led to the silicon dioxide layer used as a gate dielectric becoming so thin that the gate leakage current becomes too large.***
Keywords: FinFETs, High-K gate dielectric, Transconductance-to-Drain Current ratio; Subthreshold Swing, structure, nanotechnology VLSI, EOT, Gate tunneling, High-K Dielectrics, MOS Capacitor, Gate engineering, Dielectric engineering, DH-TMSG MOSFET

I. INTRODUCTION

This review paper points out i) Gate engineering technique and its influence on threshold voltage, transconductance to drain current ratio and sub-threshold behavior, ii) Dielectric engineering technique to reduce the leakage current, iii) Channel engineering technique to improve the mobility degradation and iv) conclusion of the study.

Various performance metrics like Transconductance-to-Drain Current ratio, Subthreshold leakage current, and Subthreshold Swing are derived to model the subthreshold behavior of the device. TFET device with cylindrical gate-all- around structure (Si-nanowire as channel and HfO2 as a high-k dielectric gate oxide) has been designed and simulated for the analyzing short channel effects. First, the effect of variation in channel lengths (100 nm to 180 nm) of the TFET is analyzed. the incorporation of Ge in the CMOS transistor structure has been employed to enable higher carrier mobility and performance.

This led to the replacement of SiO2 by a physically thicker layer of a higher dielectric constant or 'high- K' oxide such as hafnium oxide. Intensive research was carried out to develop these oxides into high quality electronic materials. To overcome SCEs and provide better packing density and performance a device called Double Halo Triple Material Surround Gate MOSFET is introduced. The device is designed by the combination of gate engineering and channel engineering. The device uses a surround gate MOSFET with triple material gate employing gate material engineering which improves the gate transport efficiency by modifying electric field pattern and surface potential along channel, resulting in higher carrier transport efficiency and SCEs. The gate material with highest work-function is used near the source and material with lowest workfunction is used near the drain end. This arrangement leads to an increase of charge carrier acceleration from drain to source end, thus can be used to reduce hot carrier effect.

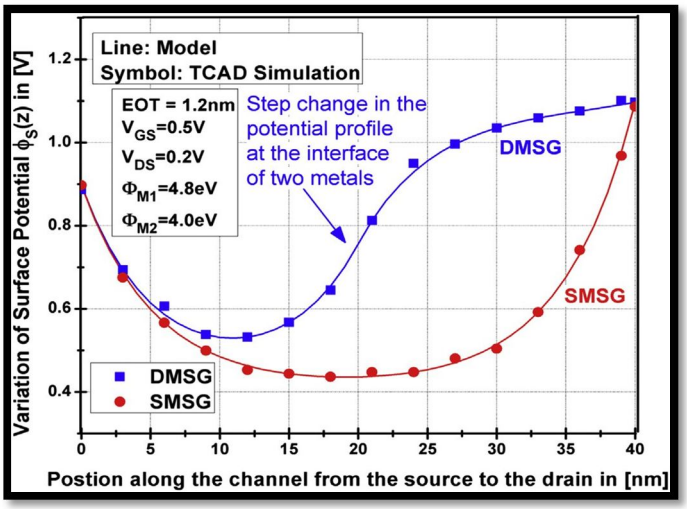
The high K oxides were implemented in conjunction with a replacement of polcryslliane Si gate electrodes with metal gates. The strong metallurgical interactions between the gate electrodes and the HfO_2 which resulted an unstable gate threshold voltage resulted in the use of the lower temperature 'gate last' process flow, in addition to the standard 'gate first' approach. In the ever-increasing need for higher current drive and better short channel characteristics, SOI MOS transistors are evolving from classical, planar, single-gate devices into three dimensional devices with multiple gates (double, triple, surround gate). In order to minimize the SCEs gate engineering or channel engineering or both are performed. The rapidly growth in semiconductor industry puts huge demand of scalable devices with low standby power for future VLSI chips.

A. Metal Oxide Semiconductors

Metal Oxide Semiconductors (MOS) transistors are the basic building blocks of MOS integrated circuits (IC). Very Large Scale Integrated (VLSI) circuits using MOS technology have emerged as the dominant technology in the semiconductor industry. The gate material with highest work-function is used near the source and material with lowest workfunction is used near the drain end. This arrangement leads to an increase of charge carrier acceleration from drain to source end, thus can be used to reduce hot carrier effect.

B. DH-TMSG MOSFET

The DH-TMSG MOSFET also involves channel engineering by introducing halo material with different doping concentrations on both drain as well as source ends. The halo implants are immediate next to the source and drain edges, such that they increase doping concentration. The three gate materials and two halo implants divide the device into 5 different regions in the present endeavour therefore, the author has attempted to investigate the different subthreshold metrics and characteristics Dual Halo Triple Material Surrounding Gate MOSFET emphasizing mainly on the design considerations. The entire investigations are distributed in various chapters that embody the present thesis.



The unification of new oxide material in the device enhances the immunity against SCEs and improves the gate leakage current. Dual-Halo Dual-Dielectric Triple Material Surrounding Gate (DH-DD-TM-SG) MOSFET has shown better performance with high dielectric constant materials. The device exhibits more value of Transconductance with high-κ dielectrics.

In addition, this review covers both scientific and technological issues related to the high-K gate stack - the choice of oxides, their deposition, their structural and metallurgical behavior, atomic diffusion, interface structure, their electronic structure, band offsets, electronic defects, charge trapping and conduction mechanisms, reliability, mobility degradation and oxygen scavenging to achieve the thinnest oxide thicknesses. Work function control by metal gate electrodes and by oxide dipole layers is discussed. The gate structure incorporates the effect of Germanium (Ge) and High-K gate dielectric material (Titanium Oxide) to combat the adverse effects imposed by the short channel. The subthreshold characteristics of Ge based JLTFET is compared with Silicon (Si) based TFET with SiO2 as gate dielectric. The results concede that the developed model is highly immune to hot carrier damage because of high transconductance-to-drain current ratio of 50 V-1, minimal leakage current, and subthreshold swing less than 40 mV/dec. The results of the proposed analytical model are validated using 2-D Sentaurus TCAD device simulator.

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C. Basic Element of Deposition

In this experiment, HfZrO was used as the High-K gate dielectric material which had a K-value of 15 at room temperature and 35 at high temperatures. This material was deposited by three types of depositional processes on MOS Capacitors placed on Si wafers, as High-K materials cannot be directly placed on Si due to lattice mismatch.

A MOS Capacitor (MOSCAP) is a simplified form of a MOSFET having only two terminals, namely, the gate and the substrate and has been used in this study for simplicity and better results. The following figure shows a MOSCAP deposited with a High-k layer.

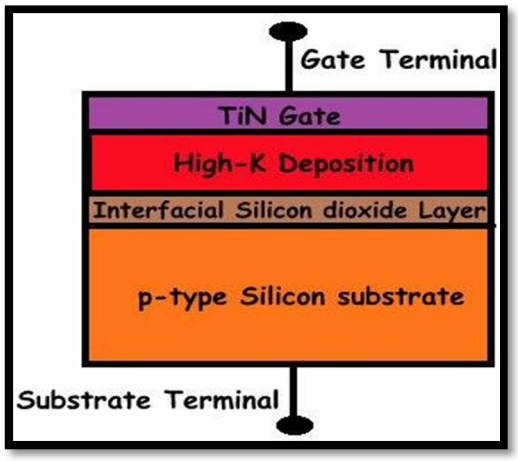


Figure 1: Basic structure of a 2-terminal MOSCAP with a High-K deposited layer

D. Regions of Operation of a MOSCAP

A MOSFET or a MOSCAP has three regions of operation: Accumulation, Depletion and Inversion.

Considering a MOS Capacitor having a p-type doped substrate, if a negative gate voltage V_G is applied (lesser than the flatband voltage V_{FB}), a negative charge is effectively deposited on the metal. In response, an equal net positive charge is observed to accumulate on the surface of the semiconductor. Since the formation of the charge-cluster is of the same type as that of the majority carriers in the substrate, carriers are said to be "accumulated" at the surface. Hence this region is known as the Accumulation Region.

Flatband Voltage (V_{FB}): The voltage at which there is no electrical charge in the semiconductor and therefore, no voltage drop across it; in band diagram the energy bands of the semiconductor are horizontal (flat).

Threshold Voltage (V_T): The minimum voltage in which the channel formation initializes. This structure includes double-gate (DG), triple-gate (TG) and gate-all-around (GAA) MOSFET which amends performance in comparison to traditional single gate MOSFETs [3 –5]. In double gate MOSFETs, two gates are present to control the channel current. But SCEs are still present in this device.

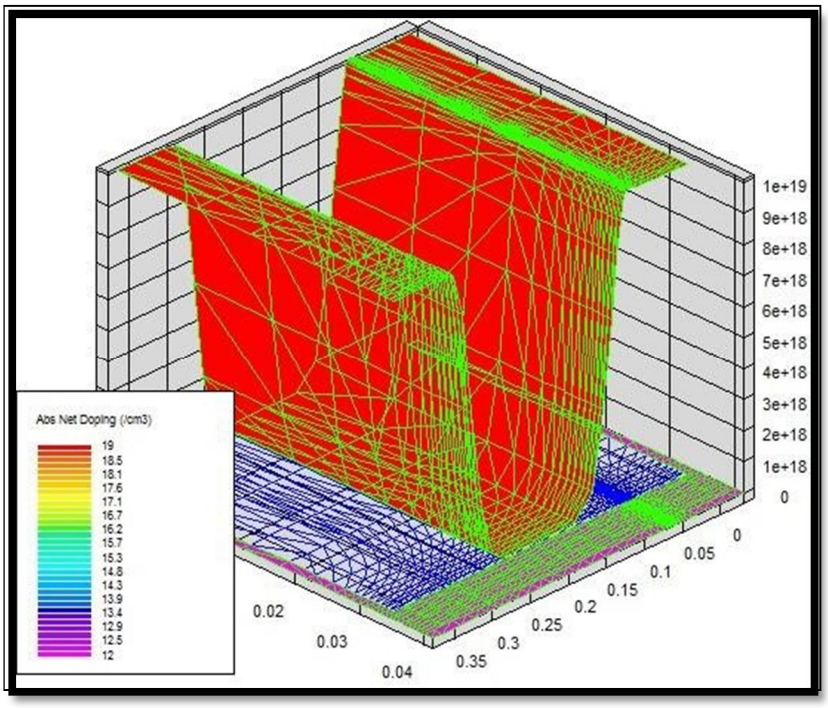
II. LITERATURE SURVEY

Microelectronics is much needed for better lifestyle standards and hence it must be developed for better performance of electronic devices in future. The fundamental component of any Integrated Circuit (IC) chip is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). It has been studied that with the reduction of the device size (mainly by 'scaling' down the size of the MOSFETs), its efficiency increases. With the scaling of the MOSFETs, more number of transistors can now be accommodated within the same IC and this has resulted in the dramatic decrease in the cost of electronic devices on the whole.

A. FinFET (fin-shaped field-effect transistor)

FinFET technology has been born as a result of the relentless increase in the levels of integration. The term FinFET was coined by University of California, Berkeley Researches (Prof. Chenming Hu, Tsu-Jae King-Liu and Jaffrey Bokor), to describe non planar, double gate transistor built on an SOI substrate. FINFET is named so because its structure contains the ultra thin vertical channel that resembles with fins of a fish surrounded by gate along its three sides. The first article on the double-gate MOSFET transistor was published by T. Sekigawa and Y. Hayashi in 1984.

The paper reveals that one can obtain significant reduction in short channel effects by sandwiching a fully depleted SOI device between two gates electrodes internally connected. SOI FinFETs with thick oxide on top of fin are called "Double- gate" and device with thin oxide on top as well as on sides are called "Triple-gate FinFET. There are two types of DG-FinFETs such as symmetric and asymmetric. The device with two gates of identical work function is known as symmetric DG-FinFET and device with two gates of different work function is known as asymmetrical DG- FinFET [11].



Gate oxide material plays an important role in determining the device performance and can meet the demand of low current while keeping power consumption under control. The semiconductor industry has made a tremendous effort to introduce high-k dielectric material in double-gate transistor manufacturing process. The 2010 ITRS (International Technology Roadmap for Semiconductor) update clearly explained that we are progressing towards high-k dielectric materials that will soon replace SiO_2 in the MOSFET. A new method must be found out to satisfy the high demands in the electronics world. Finally, a viable solution has emerged, with gate stack and channel engineering in the DH-DD-TM-SG MOSFET. Thisdevelopment in MOSFET has become the most suitable choice for the next generation devices. But, carry new challenges and opportunities for manufacturing and design. Gate stack structure is scrutinized with high dielectric materials to diminish leakage current [2, 3]. The Hafnium oxide is proposed as an alternate choice forgate oxide owing to its better thermal stability. Gate stack have equivalent oxide thickness (EOT) of 1.78 nm with insignificant leakage through gate oxide [4]. Researchers have advised numerous high-κ dielectric materials for gate oxide which consists of hafnium-based oxide and aluminum-based oxides [5]. The basic properties of good dielectrics are insulation and formation of capacitance.

The band offset value shouldbe more than 1ev to reduce the carrier injections in the bands. Good Thermal stability and high re-crystallization temperature should also possess by theoxide materials [6-8]. The density of interface trap charges diminishes with a narrow interfacial oxide layer in gate stack. The mobile communication and telecom sectors are the fastest growing fields. The customer demands high speed, small size, and low power consumption devices. But conventional MOSFET has reached its scaling limit due to existence of various short channel effects (SCEs) So, hafnium oxide is suitable material for gate stack structure along with silicon oxide. It shows higher degree of potential at higher temperature condition for MOSFET. Gate stack consist of two dielectrics which improves the sub-threshold behavior of the device. The symmetric dual halo doping is integrated into the structure which reduces the SCEs.

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B. Electric Field variation for DMSG and SMSG MOSFETs

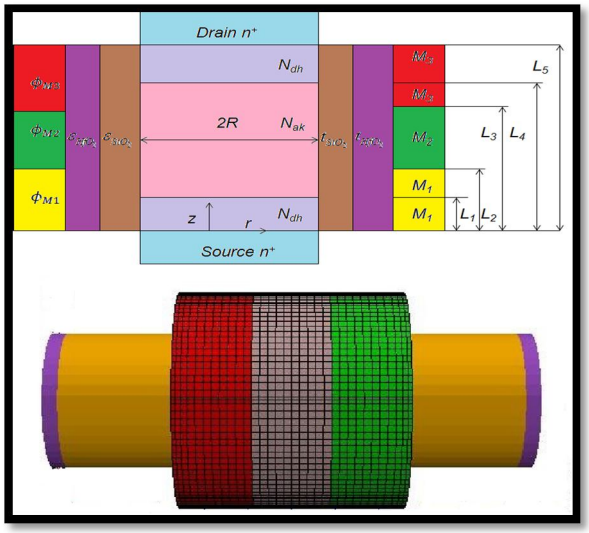


Fig. 2. (a) Cross sectional view of proposed device, (b) Simulated structure of the proposed device.

Device scaling has other benefits too. With smaller sized transistors, the size of the interconnects have got smaller and this has reduced the path length for electrons to travel, thereby decreasing the resistance offered by the path, circuit delays, power consumption and increasing the speed of device operation. With smaller devices, the gate oxide thickness is also small, so from the relation:

$$C = K\varepsilon_0 A/d$$

[where, C= capacitance, K= relative permittivity of the dielectric, ε_0= permittivity of free space (8.854 x 10^{-12} F/m), A= area & d= oxide thickness] the capacitance C is large and hence the device current is also large. This is essential for maximizing circuitspeed.
However, the disadvantage lies in the fact that with continuous scaling of the device channel length and the thinning of the gate oxide (SiO_2) beyond 20 ´, undesirable gate tunneling current and subthreshold leakage currents are observed. The electric field in the MOS device can be large enough to result to a dielectric breakdown at high temperatures. At 1.2 nm device channel, the leakage through SiO_2 has been found to be as high as 10^3 A/cm^2. If an IC chip contains a total of 1mm^2 area of the thin dielectric SiO_2, then the chip oxide leakage current is 10 A and this large leakage can discharge the battery of any cellular phone in minutes. This leakage current is a therefore a big challenge to continued scaling. The figure below represents the increase in the leakage current with the reduction of the oxide thickness.
Depending upon all these requirements, five dielectric materials are considered for the present investigation. In the literature, the suitable range of band gap is reported as 5.16 to 7.8 eV [10, 11]. The properties of various high-κ dielectric materials are reported by Nirmal et al. [12]. The band gap of silicon oxide is very high and for titanium oxide is very low in contrast to requirements. So, hafnium oxide is suitable material for gate stack structure along with silicon oxide. It shows higher degree of potential at higher temperature condition for MOSFET.
The manufacturing viability of proposed device using different approaches is available in literature. The triple metal has been fabricated by utilizing Molybdenum (Mo) acting as gate material as its work function can be change by varying N_2 implant. Cylindrical gate stack source and drain is formed by using deep trench etching. Dual dielectric is formed by deposition of oxide layers. Similartypes of devices were fabricated in the literature.However, fabrication of proposed structure has not yet done [13-16].
DH-DD-TM-SG MOSFET has been promising device for mixed signal applications due to cutback in SCEs and leakage current. Distinct high dielectric constant materials are utilized in the device and comparison has been carried out among their performances. Short channel behavior of proposed device has beeninvestigated and proposed device reveals outperform performance. Atlas device simulator is used for the simulation. We review that progress in this article, with an emphasis on the key developments in the high-K/metal gate stack process. We also summarize recent results on incorporation of Ge in the transistor, which appears to provide a viable route to higher performance technology.

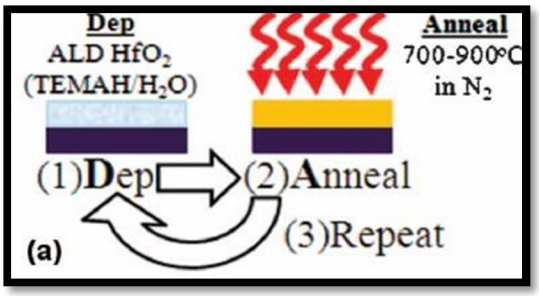
Next, if the positive gate voltage is continued to be increased (greater than threshold voltage), the majority holes in the substrate is repelled downward direction, while minority electrons from the p-type substrate get attracted towards the surface. This forms an "inversion layer" at the surface, inverting the conductivity type. This is known as the Inversion Region.

Where V_{Th1} and V_{Th2} are threshold voltages extracted at drain bias V_{DS1} 0.1 V and V_{DS2} 1.0 V. Fig. 8 shows the variation of ĐIBL as a funɛtion of channel length. Fig. 8 shows that DMSG device out- performs SMDG device due to the higher gate-controllability, increased screening of the threshold voltage defining region (Re- gion under M_1 near the source) from the variation of the drain bias caused by the step pattern in the potential profile. On the other hand, Fig. 9 shows that DMDG shows better performance than SMDG for the variation of DIBL as a function of radius R. From Figs. 6 and 3 it is evident that that thicker Si film exhibits higher VTh roll- off with a reduced gate-controllability indicating a reduced SCEs, thus justifying higher DIBL for increase in radius *R.*

It is more than a decade since high-K gate dielectric research for Si-based transistor technology was first reviewed [2,3]. We begin this review with a brief summary of the scaling issues that drove the incorporation of high-K dielectrics and metal gate technologies. We then discuss the materials chemistry of the high-K dielectrics employed in transistor fabrication. This is followed by a review of the current understanding of the high-K/semiconductor interfacial bonding. Defects, which play an important role in high-K dielectrics, are then discussed. Of course, the electrical performance of the transistor is paramount, and we review the recent developments, including work function control for the transistor gate stack.

III. DEVICE STRUCTURE AND SIMULATION DETAILS

The schematic structure of double gate FinFET used in the simulation work is shown in Fig. 1.



Over the past few decades, the technology is oriented towards the miniaturization of electronic components and transistors in integrated circuits (ICs). The main aim is to increase the chip density i.e. more transistors per unit area that can improve circuit performance without compromising device manufacturing cost. Gordon Moore in 1965 predicted that the no. of transistors in a chip doubles every two years [1], however, the reduction in the transistor dimension is obstructed by the short channel effects.

A. Three types of Depositional Processes

The three types of depositional processes used are:

1) DADA (Deposition-Anneal-Deposition-Anneal) in which the silicon wafer samples were subjected to the deposition of the dielectric followed by a thermal annealing in a cyclical manner until 44 such cycles were obtained for a given test wafer.

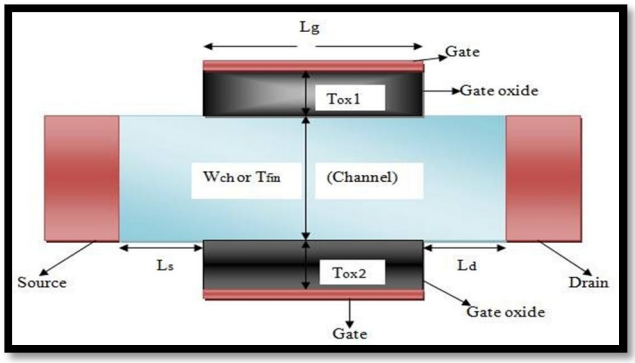


Figure 3: The DADA Process

2) DSDS (Deposition-Plasma-Deposition-Plasma) in which the samples were subjected to a similar cyclical process as that of DADA with the deposition of the dielectric and Ar plasma. As-Dep (As-Deposited) in which the dielectric for the samples was deposited without any other intermediate step.

B. Device Structure and Simulation

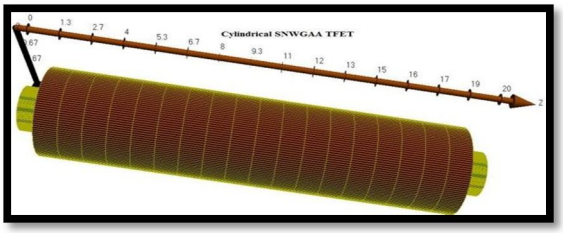
The cross-sectional views of DG and GAA nanowire are illustrated as in **Fig 1 (a)** and **(b)**. The blue colour is the oxide layer which is SiO_2 that will be change later to other high-k materials. The orange colour represents the channel (silicon-type), the purple layer is the conductor layer and red colour in GAA diagram is the polysilicon. The device simulations were performed using Atlas simulator in Silvaco TCAD tool. Both of DG and GAA are having the same parameter setting as shown in **Table 1**. In this study, SiO_2 is replaced with other different high-k dielectric materials. The high-k materials chosen in this study are Si_3N_4, Al_2O_3, ZrO_2 and HfO_2. **Table 2** shows the band offsets and dielectric constant for different dielectric materials (Chaudhary et al. 2018),(V. Kumar et al. 2011) used in this simulation.

C. Device Simulation

1) Structure Design

The device has been structured using the electronic simulator in the scales of dimension specified. After that, the contacts are set, and the constant doping profile has been selected of 1E+18 and 1E+14 for the source and the drain, respectively. Fig. 2. shows the three-dimensional structure after the successful meshing of the device. The generation and recombination rates of the device are modeled using band-to-band tunneling current. Both the processes compute the probability of tunneling in the simulator as a variation of Kane or Keldysh's equation and further analyze the subsequent meshed structure.

The different models make use a different analysis of the band structure because it significantly affects the amount and region of the predicted tunnel current. Simulators have two models, namely local and non-local tunnel model. The non-local tunneling model has been used in the designed TFET which keeps subthreshold slope up to 60mV/decade. The model is bound to the quantum-mechanical tunneling of the electrons from source to the channel using carrier transport mechanism.



2) Non Local Tunnelling Model

The tunneling is the process of transfer electron or hole crossing the junction. The tunneling causes pairs of electrons and holes; hence the electron and hole transfer rates are opposite and equal [15]. The model is based on Landauer's equation. The primary default parameters of the model are listed in Table I. The values specified for conduction and valence band effective masses MC or MV are used only when the METUNNEL or MHTUNNEL are not defined. The METUNNEL and MHTUNNEL are the effective mass of electron and hole calculated from two band tunneling model. As the tunneling is a process involving electron crossing the junction, the net current per unit area for an electron with longitudinal energy ε and transverse energy ε_t [27], can be written as

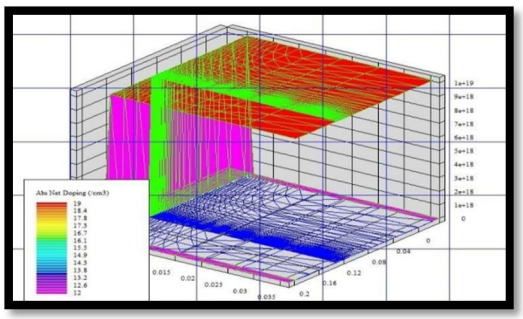


Fig. 4. Representation of non-local band-to-band tunnelling (Atlas, 2014).

In the band-tunneling model, tunneling current depends on the edge profiling along the entire path between the concentrations which suggests the field developing progressively at all the points in the tunnel and makes the tunneling a non-neighborhood. The net gap recombination rate for band-to-band tunneling by the electric field is shown in Fig. 4. When the positive gate voltage is applied, the dominant mode at the gate-source junction is band-to- band tunneling (BTBT). The non-local band to band electron energy rates at the ON and OFF states are shownFig. 4. For this structured device, BTBT generation rate increases when the device is ON and finds its maximum value at the source channel junction.

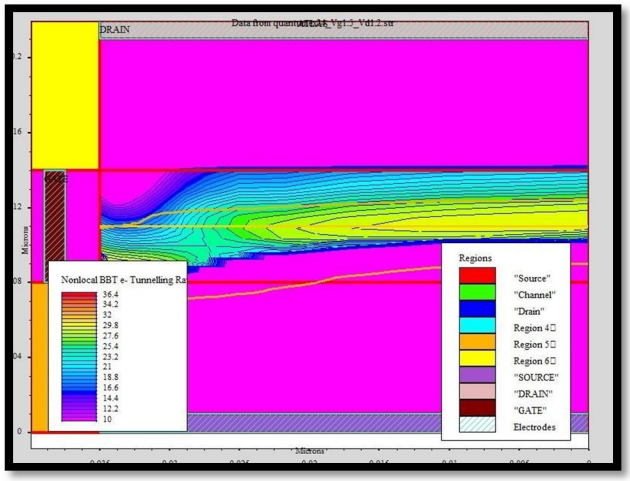
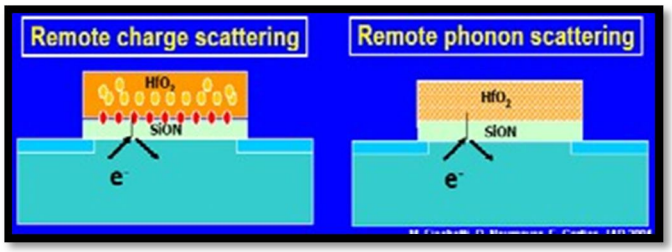


Fig. 5. Non-local BTBT electron tunnelling rate in the device.

Knowing the current mechanisms in the device makesit easier to understand the changes in performance based on variations in devices parameters. Fig. 5 (a) and (b) illustrate the electron distribution function trends concerning changes in the gate as a contour of visualized.

h is the Planck's constant, m_0 is the mass at resting of an electron, m_e/m_h is the effective mass of the electron or holes, and $\varepsilon_c/\varepsilon_v$ is the conduction or valence band energy. The tunneling current density at given longitudinal energy can be obtained by substituting these values in (2).The resultant current is injected into the simulation at x_1 and x_2 and iterated for every tunnel slice in the regions for energy level between $\varepsilon_{\text{lower}}$ and $\varepsilon_{\text{upper}}$. The field lines of non-local band-to-band tunneling of the simulated device are shown in Fig. 4.



The body factor is known as the gate control efficiencyon the channel potential which is equal to 1, at room temperature 300K) which makes to the value of SS=60 mV/decade. The gate does not just control the channel potential; it also depends on the length of the source to drain regions along with V_{ds} voltage.

The total channel length of the proposed device is cho- sen to be 12nm. The remaining device parameters used are: channel thickness (tge) is 2nm, gate-oxide thickness (tox) is 1nm and Vds = 0.3V. The length of the three gate metal regions is: L1= L2= L3=4nm.

D. Mathematical Modeling

The cross sectional view and structure of the 12nm Ge based Triple Material Gate-All-Around Junctionless Tunnel FET (Ge-TMGAA-JLTFET) is shown in Fig.1. In this structure, the gate electrode comprises of three materials M1, M2, and M3 with different work functions. These three distinct materials are deposited over the respective gate lengths L , L and L , with total gate length (12 nm) defined as L= L1 + L2 + L3.

The gate materials are chosen in such a way that □M1 > □M2 > □M3. The work function of tunneling gate metal M1 is □M1 = 4.8 eV (Au), gate material M2 with □M2 =4.6 eV (Mo), gate material M3 at drain side is with □M3 =4.4 eV (Ti). The proposed model has a 12nm germanium channel, which is heavily n-type doped at 1019cm-3. The formation of source and drain regions is without separate doping on the germanium channel.

From the table, it can be seen that the EOT is the least for the As-Deposited Sample and hence, it gives the best results out of the other two processes. The trapped oxide charge within the gate dielectric was also studied and a plot was obtained as follows.

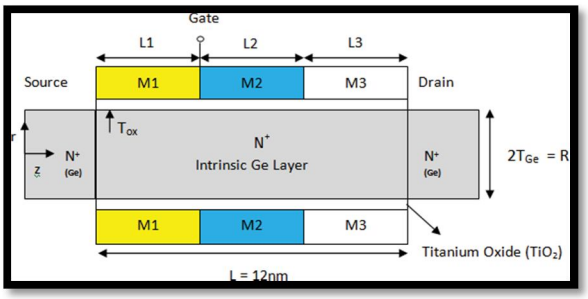


Figure 6: C-V curves depicting more trapped positive oxidecharge accumulation for DSDS sample as compared to As- Deposited

At the location of minsp , the sub-threshold leakage current starts in the device. So, it is very useful for modeling of the threshold voltage.

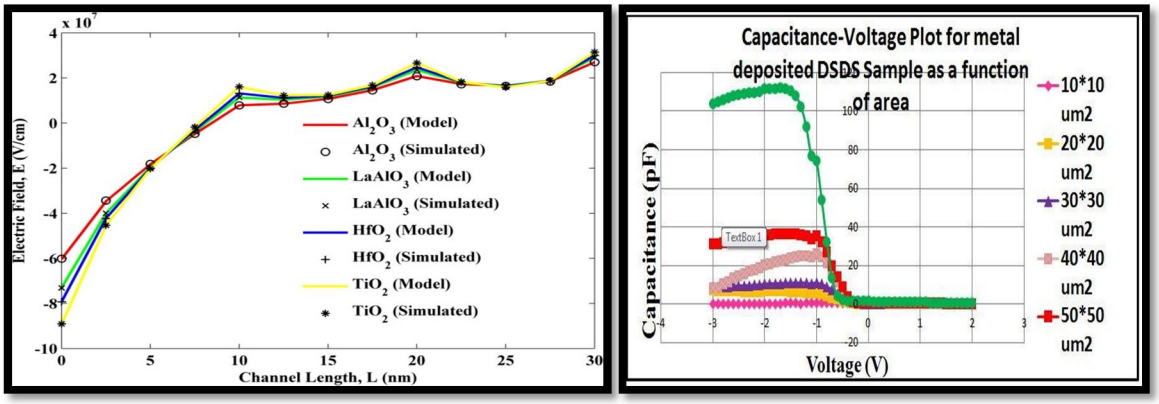


Figure 7: C-V curves showing the different values for MOSCAPsof different area ranging from 10 to 50 square microns

Hence from the given test wafers, it can be concluded that the As-Deposited sample is the most suitable depositional process of High-K materials on MOSCAPs and hence, can also be applied on MOSFETs for good results. In this way, a High-K will be deposited efficiently (as its direct deposition on Si causes mismatch of the different crystal lattices) by this process and in doing so, further device scaling will also be possible without adverse leakage effects.

For higher drain voltages, the peak electric field will be at the drain end. The high electric field leads to avalanche multiplication of carriers. These carriers in turn gain high energy and become “Hot” electrons. The hot carriers can easily get trapped into the oxide layer and cause severe reliability issues. But with the incor- poration of three different doping profiles in the gate region, the peak electric field at the drain side is sup- pressed effectively, shown in Fig.5.(b).

The plot of subthreshold swing along the channel length for various values of germanium thickness is shown in Fig.7. The proposed analytical model results are compared with Si based TMGAA-JLTFET and simu- lated using TCAD device simulator. It is inferred that the subthreshold swing has attained a minimum value of 35mV/dec, when compared to Si based JLTFETs having subthreshold swing less than 50mV/dec. With minimum germanium film thickness, the subthreshold degradation is also minimal.

This demonstrates that, with thinner gate oxide, the electric field component can pervade the channel region more easily. Once the electric field components are strong enough, then the gate controlling capability is reinforced and subthresh- old degradation in minimized. With lightly doped drain structure, the peak electric field at the drain end is sup- pressed and hence Drain Induced Barrier Lowering (DIBL) effect is also reduced tremendously.

E. Surface Potential

The present analysis is carried out for surface potential $\square sp$. The different metal work function produces step potential profile which minimizes the SCEs and screening of a channel province under high metal work function from the variation in the drain potential. The lower metal gate work function near to drain side absorbsthe extra drain bias variation which mitigates the DIBL [22, 23]. The difference in work function among theinterfaces of metals creates the step up in the potential profile. Fig. 3 shows that triple material structure has two step function profile which is a clear indication of a reduction in SCEs. These gradual steps function profile at the interface screens the higher metal gate M_1 work function region from the fluctuation of drain potential. Enhanced *VDS* is discarded across the lower metal gate M_3 work function region. It is noticed that the minimum surface potential $\square sp$ happens for DH-DD-TM-SG

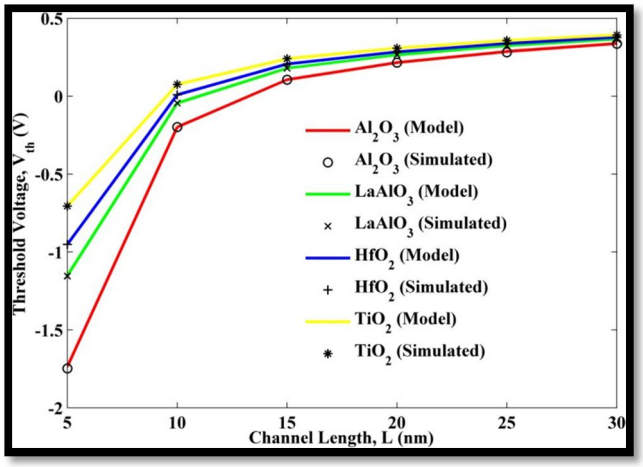


Fig. 8. Field of proposed device with various dielectricmaterials.

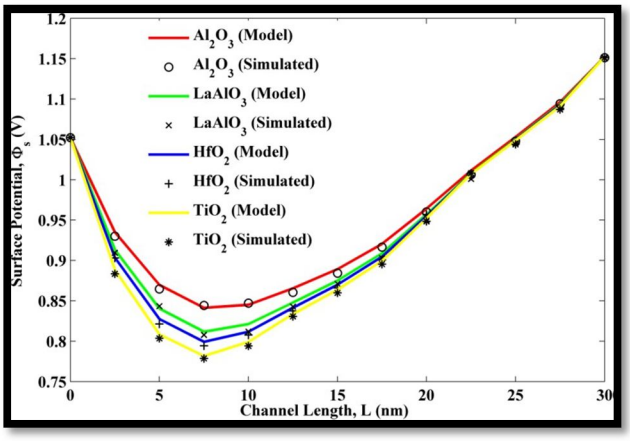


Fig. 9. Potential of proposed device with various dielectricmaterials.

MOSFET in the halo region. In this novel device, there are additional steps at the drain and source sides. Normally, there are two step function profiles in TM-SG but for dual halo, it is realized that the surface potential of DH-DD-TM-SG exhibits four step function profiles. So, this extra step profile further helps in scale down the short channel influence and improving the current driving capability. The analytical results are well in agreement with simulated results validating the model [24]. Fig. 3 highlights the potential of proposed device with different values of κ. The step rise in potential is observed in halo doped region of 1.05 V as compared to the rest of the portion which shows potential of 0.78 V which is due to sudden change in doping. The value of surface potential is more for Al_2O_3 as compared to other dielectrics due to its lower physical thickness. TCAD Silvaco is used for extracting the simulation data and MATLAB is used for plotting and solving mathematical equations [25].

1) Electric Field

Fig. 9 reveals the field of DH-DD-TM-SG MOSFET with various dielectric constants. It is also observed from the figure that the increase in κ values enhances the field in the channel. The extra peak of field is detected at the interfaces of metals. These peaks decrease the field at drain terminal which causes diminution in DIBL and hot carrier effects. These are the prime SCEs in MOSFET which reduces its performance at lower dimension.

2) Threshold Voltage

Fig. 10 shows the threshold voltage of DH-DD-TM-SG MOSFET. It is also observed from the figure that the increase in κ values enhances the threshold voltage. Lower value of threshold voltage of a device increasesthe leakage current and higher value of threshold voltage reduces the operation speed of a device. The proposed device has moderate value of threshold voltage as compared to its counterpart. It indicates improvement in gate controllability due to channel engineering. Hence,proposed device is worthy for low power applications.

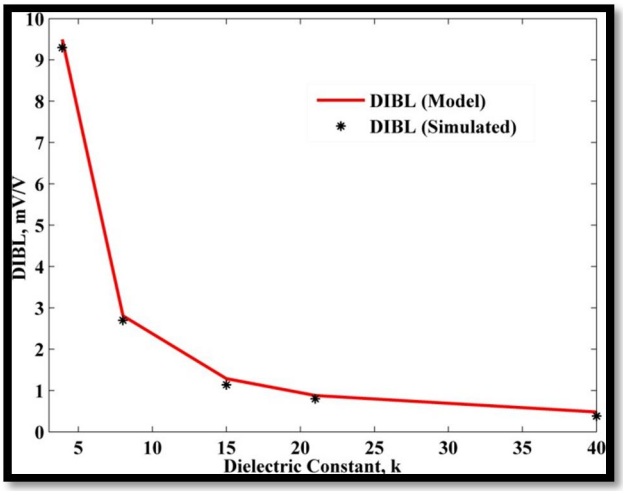


Fig. 10. Sub-threshold current of proposed device with variousdielectric materials.

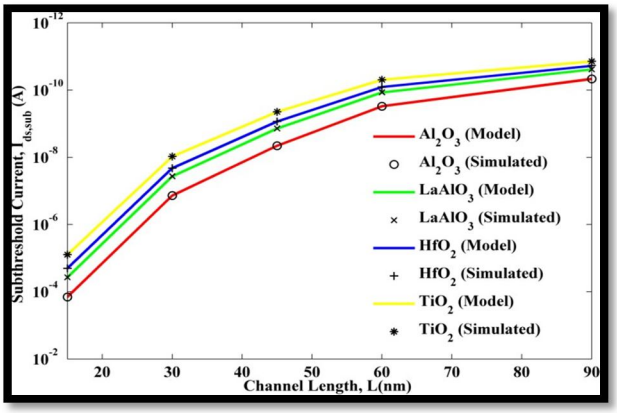


Fig. 11. DIBL effect of DH-DD-TM-SG MOSFET with variousdielectric materials.

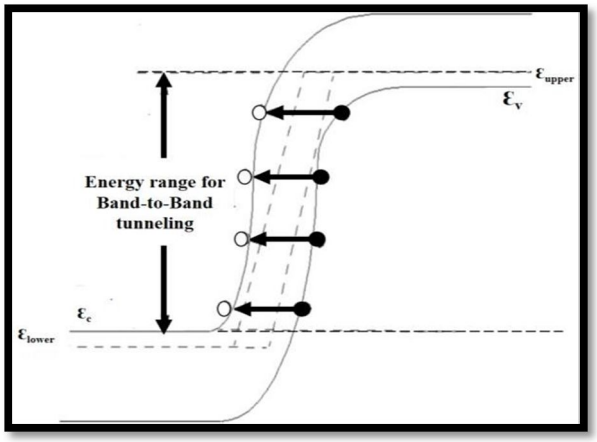
3) Sub-threshold Current

Fig.11 depicts the sub-threshold current with various dielectric constant. The leakage current of device with $LaAlO_3$ as dielectric is $0.369X10^{-9}$ A. $ID_{,sub}$ of HfO_2 is $0.210X10^{-9}$ A, which indicate significant reduction in leakage current of 42.94% as compared to others. It is noticed from the Fig. 6 that leakage current reduces exponentially with increase in dielectric value. The high- κ materials provide more physical thickness which diminishes the tunneling of carriers through the insulator.So, proposed device with HfO_2 as dielectric significantly mitigates the leakage current which makes devicesuitable for low power applications.

Hot carrier damage may affect the endurance of non- volatile memory. Hot Carrier Effect (HCE) refers to de- vice degradation or instability caused by hot carrier injection. This HCE being an important factor in the small-scale integrated circuits has to be reduced with the increase in the Electric Field near the junction of the two-metals, leads to an increase in the carrier transport efficiency. Moreover, from Fig. 4, a reduction of the Electric Field near the drain end for DMSG MOSFET is evident. In contrast, for SMSG MOSFET, an increased value of Electric Field as compared to DMSG MOSFET is also evident. A high Electric Field near the drain side may results in the formation of highly energetic and accelerated "hot-carrier", which under the influence of trans- verse Electric Field may tunnel into the oxide, gets trapped into the oxide region and damage the interface, thus causing concerns about device reliability. The reduction in the drain side Electric Field indicates a reduction in the deleterious Hot-Carrier Effects (HCEs).

TCAD simulation of the variation of subthreshold Drain current (IDS) as a function of the VGS for DMSG and SMSG MOSFETs. Fig. 7 indicates that DMSG provides higher IDS as compared to SMSG devices, owing to its higher carrier transport efficiency attributed by the increase in the average Electric Field produced by the gate-material engineering. The peak in the electric field profile leads to a rapid acceleration to the carriers at the interface of metals, resulting in enhanced carrier transport efficiency to supply more and more carriers to reach the drain terminal. However, it is worth mentioning that an increase in the subthreshold drain current causes an increase in the sub- thershold leakage current and a decrease in the subthershold swing, which needs to be minimized for ultra low power device applications.

The DG-FinFET structure can be characterized in terms of fin length (Lg) and fin thickness (Tfin or Wch). Here, the channel is of silicon material with N-type doping concentration of 1e+16 /cm3, whereas doping concentration of drain/source is 1e+16/cm3 and oxide thickness is 2 nm. The value of the gate contact work function is 4.6 eV and the band gap of Si is 1.12 eV at 300 K. The device simulations have been carried out using PADRE simulator from MuGFET, which is based on the drift-diffusion theory and provides self consistent solution to the Poisson and drift-diffusion equations.



Where, Φ_{ms} represents metal-semiconductor work function difference between the gate electrode and the semiconductor, Φ_f is the Fermi potential, Q_D is the depletion charge in the channel, C_{ox} is the gate capacitance and Q_{ss} represents charge in the gate dielectric.

4) Subthreshold Swing (SS)

One of the major parameters for a MOSFET device is subthreshold swing (SS) which determine the holding time in dynamic circuits and static power dissipation in static CMOS circuits. SS is a parameter for the calculation of leakage current and it can be expressed by the following equation [3]:

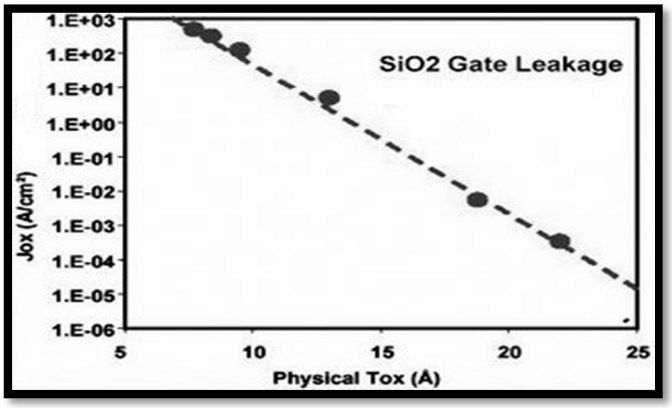
IV. DIBL EFFECT

A large bias at the drain causes DIBL in the MOSFET which degrade the device performance. The barrier height between source and channel becomes lowered [26]. Thus, control of gate terminal decreases over the channel. Fig. 7 illustrates the DIBL with varyingdielectric constant. It is observed from the figure that SiO_2 has highest value of DIBL which is 9.49 mV/V. As the value of κ increases then corresponding exponentiallydecrement in DIBL are observed. HfO_2 reveals DIBL of 0.88 mV/V which points out significant reduction in DIBL.

When DIBL of proposed device is compared with DIBL of Nirmal et al. [12] device it shows improvement of 26 %. Hence, proposed device provides betterreduction of SCEs. Threshold Voltage Roll-off Effect

The attenuation of threshold voltage with attenuationin channel length is called "V_{th}-roll off" [27, 28]. Fig. 8 depicts the roll-off of threshold voltage. The V_{th}-roll off has been calculated by finding the deviation in threshold voltage for small and long channel devices. It is observed from the figure that SiO_2 has highest value of V_{throll} which is -0.15 V. As the value of κ increases then corresponding exponentially increase in V_{throll} are observed. HfO_2 reveals V_{throll} of -0.09 V which points out significant reduction in V_{throll}.

A. Sub-threshold Swing



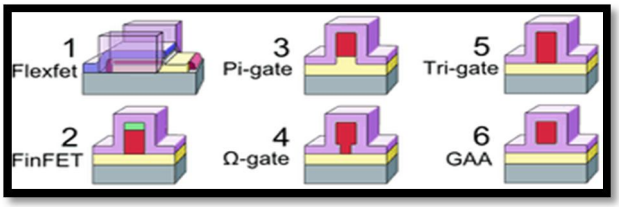
SS is the minimum voltage required to enter into the ON state from the OFF state. The ideal value of SS is 60 mV/decade. Fig. 9 shows the SS as a function of variation in dielectric constant. SS decrease with increasein value of κ. It is observed from the figure that HfO_2 shows an improvement of 15.34% as compared to SiO_2 due to reduce leakage current in former oxide.For a MuGFET, typical value for SS parameter is 60 mV/decade i.e. 60 mV change in gate voltage brings about a tenfold change in drain current.

B. High-k/Metal Gate Transistors

Until earlier this decade, the scaling and performance trends of the logic transistor were mainly the result of SiO2 gate oxide scaling as well as source–drain junction and channel doping engineering. Over a period of 15 years, the physical gate-oxide thickness was scaledfrom about 20 nm to only 1.2 nm in the 65 nm technology node. The nitrogen profile in the 1 nm thick nitride silicon oxide was carefully optimized to ensure that the dopant penetration from the doped polysilicon gate electrode was prevented by the nitrogen barrier and yet the scattering of carriers at the interface between the gate oxide and the channel was mitigated.

Further, various innovative gate oxide annealing and surface cleaning technologies were also introduced to improve the reliability and reduce defect density in the ultra-thin nitride silicon dioxide. As the thickness of the SiO2 gate oxide reached 1.2 nm, which is less than five atomic layers thick, the industry ran out of atoms to scale the gate oxide further, since any more reduction in physical oxide thickness will makethe gate leakage— due to quantum mechanical tunnelling of electrons and holes through the gate oxide— unacceptable for circuit operation and overall power consumption. To solve this problem, an alternative high-k gate dielectric is needed. The higher permittivity (k) of the high-k dielectric allows thedevice engineer to achieve the same or even lower electrical oxide thickness with a physicallythicker dielectric than silicon dioxide and reduce the gate leakage.

C. Multiple Gate Transistors



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The last decade has witnessed tremendous innovation in transistor architecture with the introduction of strained silicon channel, high-k/metal gate stack and non–planar 3D transistor architecture, marking the end of the era of the traditional planar transistor scaling.

While strained silicon and high-k/metal gate technologies will continue to play significant roles in advancing present CMOS technology, the need for further scaling of the transistors will require the transistor structure itself to evolve. For example, a transition for the present planar structure to non-planar, three-dimensional (3D) structures such as the tri-gate transistor,6 as shown in Fig. 3, is urgently needed to improve the short-channel performance and enhance scalability. This transition is inevitable since the high-k/metal gate stack with even low equivalent oxide thickness (EOT) is insufficient to control the source to drain leakage once the gate length is aggressively scaled and the source-drain extension regions approach each other.

This transition is inevitable since the high-k/metal gate stack with even low equivalent oxide thickness (EOT) is insufficient to control the source to drain leakage once the gate length is aggressively scaled and the source-drain extension regions approach each other. The tri-gate transistors, by design, are fully depleted so that the entire available silicon underneath the gate electrode is depleted of carriers before the threshold condition is reached. Such tri-gate transistors have shown significantly improved electrostatics in terms of sub-threshold slope (SS) and drain induced barrier lowering (DIBL)and hence better scalability than planar transistors. The key knob controlling the short channel effects in 3D transistors are given by the effective channel length (Leff) and the effective fin width (Weff) of the device.

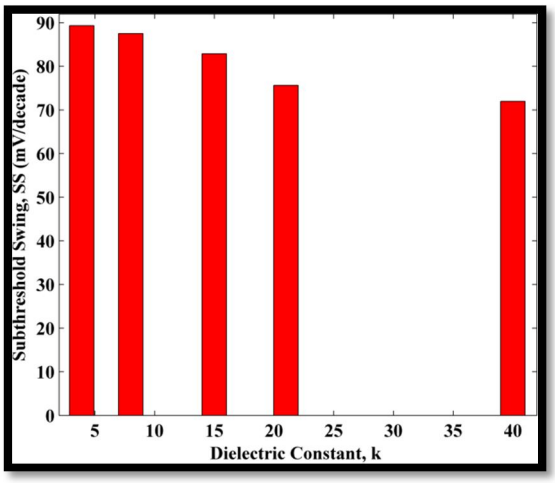


Fig. 12. Sub-threshold swing of proposed device with variousdielectric materials.

V. THRESHOLD VOLTAGE

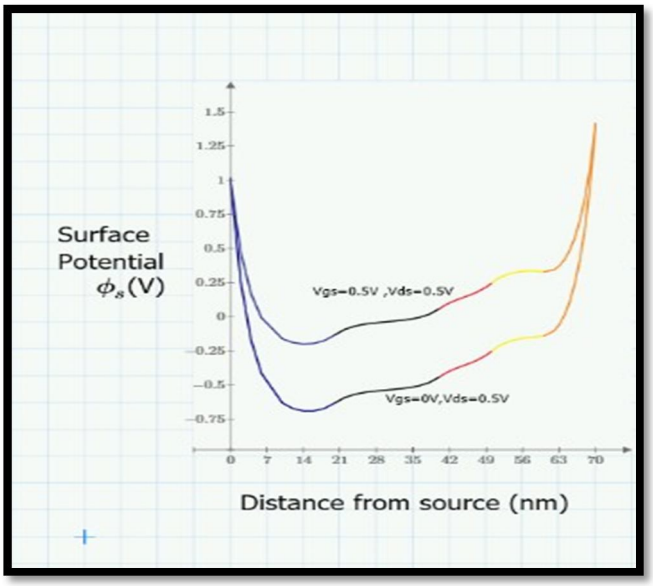
The threshold voltage, commonly abbreviated as V_{th}, of a field-effect transistor (FET) is the minimum gate-to-source voltage $V_{GS(th)}$ that is needed to create a conducting path between thesource and drain terminals. It is an important scaling factor to maintain power efficiency.

The threshold voltage VT of the MOSFET is a fundamental parameter in circuit design and testing, as well as in technology characterization, and should be used whatever the model adopted for the transistor. The classical definition of threshold, the gate voltage at which fs=2fFþV, which links the surface (fs), the Fermi (fF), and the channel (V) potentials is indeed'surface potential-based'.

A. Surface Potential

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi_i(r,z)}{\partial r}\right)+\frac{\partial^2\varphi_i(r,z)}{\partial z^2}=\frac{qNi}{\varepsilon si}$$

$$L_{i-1}\le z\le L_i,\ 0\le r\le\frac{t_{si}}{2}\ _{i=1,2,3,4,5}$$



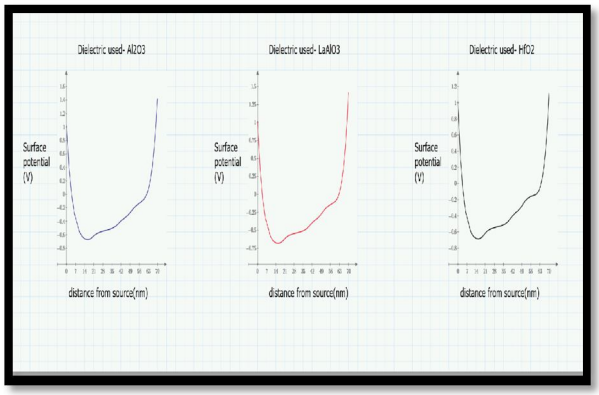
The design and time complexity of the proposed model is quite high because it involves both channeland gate engineering. In order to reduce the short channel effects, the proposed model involves complexity than the existing models. But usage of poisson equation and solution using boundary conditions make the method of designing quite easy and comfortable. Using the boundary conditions (3)– (9) the surface potential is determined using parabolic approximation method. DH-TMSG MOSFET

B. Analytical Model

To build up a 2D analytical model of DH-TMSG MOSFET, we are going to use 2D poisson equation. As the DH-TMSG MOSFET is of cylindrical symmetry along the silicon pillar, we are going to use cylindrical coordinate system with radial direction r, vertical direction z and angularcomponent θ. Where i represents the different regions, ϕi (r, z) represents the potential distributionN1 = Nh; N2 = N3 = N4 = Nc; N5 = Nh; L0 = 0

1) Analytical Model For Subthreshold Current (DH-TMSG MOSFET)

The model proposed is based on Virtual Cathode Concept. In ideal circumstances a device should be turned off when the gate overdrive voltage is belowthe threshold voltage of the device, but in practical situations a very small amount of current flow in the MOSFET. This current is subthreshold current and studying this makes us understand the subthreshold behaviour of the device.
Using the channel potential solution, the subthreshold current can be calculated. Since the current density flows predominantly in the z direction from source and drain, the electron quasi-Fermi potential is essentially constant in the r direction.



2) Surface Potential ComparisonBetween The Dielectrics

The figure highlights potential of proposed device with different values of k at two different gate voltages. The value of surface potential is more for Al2O3 as compared to other due to lower physical thickness

3) DH-TMSG MOSFET Analytical Model

To build up a 2D analytical model of DH-TMSG MOSFET, we are going to use 2D poisson equation. As the DH-TMSG MOSFET is of cylindrical symmetry along the silicon pillar, we are going to use cylindrical coordinate system with radial direction r, vertical direction z and angular component..θ.

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \varphi_i(r,z)}{\partial r}\right)+\frac{\partial^2 \varphi_i(r,z)}{\partial z^2}=\frac{qNi}{\varepsilon si}$$
$$L_{i-1}\le z\le L_i,\ 0\le r\le\frac{t_{si}}{2}\ _{i=1,2,3,4,5}$$

Where i represents the different regions, ϕi (r, z) represents the potential distribution
N1 = Nh; N2 = N3 = N4 = Nc; N5 = Nh; L0 = 0

4) Boundary Conditions

The boundary conditions considered for the proposed structure is given as:

a) The electric field is zero at the centre of the silicon

$$\left.\frac{\partial \phi_i(r,z)}{\partial r}\right|_{r=0}=0$$

b) The electric flux at the gate/oxide interface is continuous for metal gates:

$$\left.\frac{\partial \phi_i(r,z)}{\partial r}\right|_{r=t_{si}/2}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\times\frac{V_{gs}-V_{FBi}-\phi_i(r,z)}{t'_{ox}}$$
$$t'_{ox}=r\times\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)$$

c) The surface potentials at the interfaces of the dissimilar metals are continuous:

$$\phi_i(r,L_i)=\phi_{i+1}(r,L_i)$$
Where i = 1,2,3,4

d) The electric field at the interfaces of the dissimilar metals are continuous:

$$\left.\frac{\partial \varphi_i(r,z)}{\partial z}\right|_{z=L_i}=\left.\frac{\partial \varphi_{i+1}(r,z)}{\partial z}\right|_{z=L_i}{}_{i=1,2,3,4,5}$$

e) The potential at the source end is

$$\phi_1(r,0)=V_{b_1}$$

Where built in potential is given by

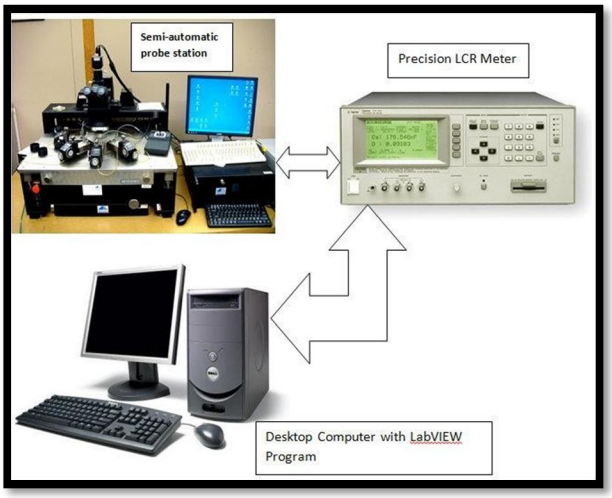
$$V_{b_i}=V_T\ln\left(\frac{N_iN_D}{n_1^2}\right)$$

Where, VT = kBT/q, kB is the Boltzmann Constant and T is the temperature (6). The potential at the drain end is

$$\phi_i(r,L_5)=V_{bi}+V_{ds}$$

5) Threshold Voltage (V_{th})

Maintaining higher threshold voltage is a key requirement for low standby power (LSTP) logic technologies and the main cause for threshold voltage rolls off is charge sharing. The threshold voltage (V_{th}) variations for various high-k dielectric materials are shown in Fig. 2. From the graph, it can be seen that the threshold voltage values for SiO_2, SiON,Al_2O_3, Y_2O_3, HfO_2 and La_2O_3 are 0.17 V, 0.32 V, 0.34 V, 0.38 V, 0.41 V and 0.42 V respectively. The higher value of V_{th} is obtained for La_2O_3, thereby, resulting in 147% improvement in comparison to SiO_2 as gate dielectric.



VI. RESULTS

In this section, we present various results pertaining to gate dielectric materials such as SiO_2, SiON, Al_2O_3, Y_2O_3, HfO_2 and La_2O_3 for Si based DG-FinFET. The simulated data of proposed model is calibrated with the simulated work [21] which validates the models used for the device simulation. Fig. 2 depicts that simulated results are well matched with the experimental results. Drift Diffusion (DD) model has been employed to model the carrier transport mechanism in device simulation. Also, to model the carrier concentration, Shockley-Read-Hall (SRH) recombination model combined with Auger re- combination model are used in the simulation.

VII. OBSERVATION

By using Atlas Silvaco TCAD tool, device design model and the simulation were performed to evaluate the electrical characteristics for DG and GAA MOSFET by using different gate dielectric material. It can be observed that towards higher value of dielectric constant, the on current and Ion/Ioff ratio, will increase while the SS, Vth and leakage current will reduce. An increased value of dielectric constant improves electrical device characteristics. Overall, HfO2 shows thebest performance compared to other simulated dielectric materials especially with SiO2 for both DG and GAA MOSFET even in smaller dimension. GAA has better leakage current, SS characteristics when using higher k material while DG has better Vth characteristics.

VIII. CONCLUSION

Performance analysis of DG-FinFET based on SiO2, SiON, HfO2, Al2O3, Y2O3 and La2O3 gate dielectrics for 12 nm node technology has been studied using numerical simulations. La2O3 demonstrates high transconductance, better threshold voltage, reduced SCEs such as sub-threshold swing and DIBL and is amongst the best when compared to the other gate dielectric materials.

IX. DISCUSSION

The DSDS and DADA devices seem to have more positive oxide charge in the dielectric as compared to As-Deposited device. Hence from the given test wafers, it can be concluded that the As-Deposited sample is the most suitable depositional process of High-K materials on MOSCAPs and hence, can also be applied on MOSFETs for good results. In this way, a High-K will be deposited efficiently (as its direct deposition on Si causes mismatch of the different crystal lattices) by this process and in doing so, further device scaling will also be possible without adverse leakage effects.

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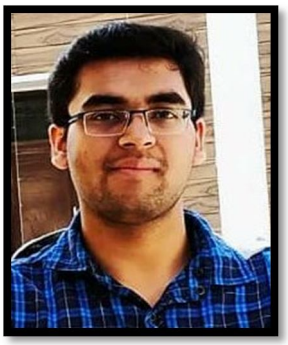

Prateek Gupta

Prateek Gupta is a Software Developer Engineer in Cognizant Technology Solutions. He is interested in Machine learning, Data Science along with research work applications on them & solving puzzles. He is regularly used to read new researches, upcoming technology in the field of Artificial intelligence.

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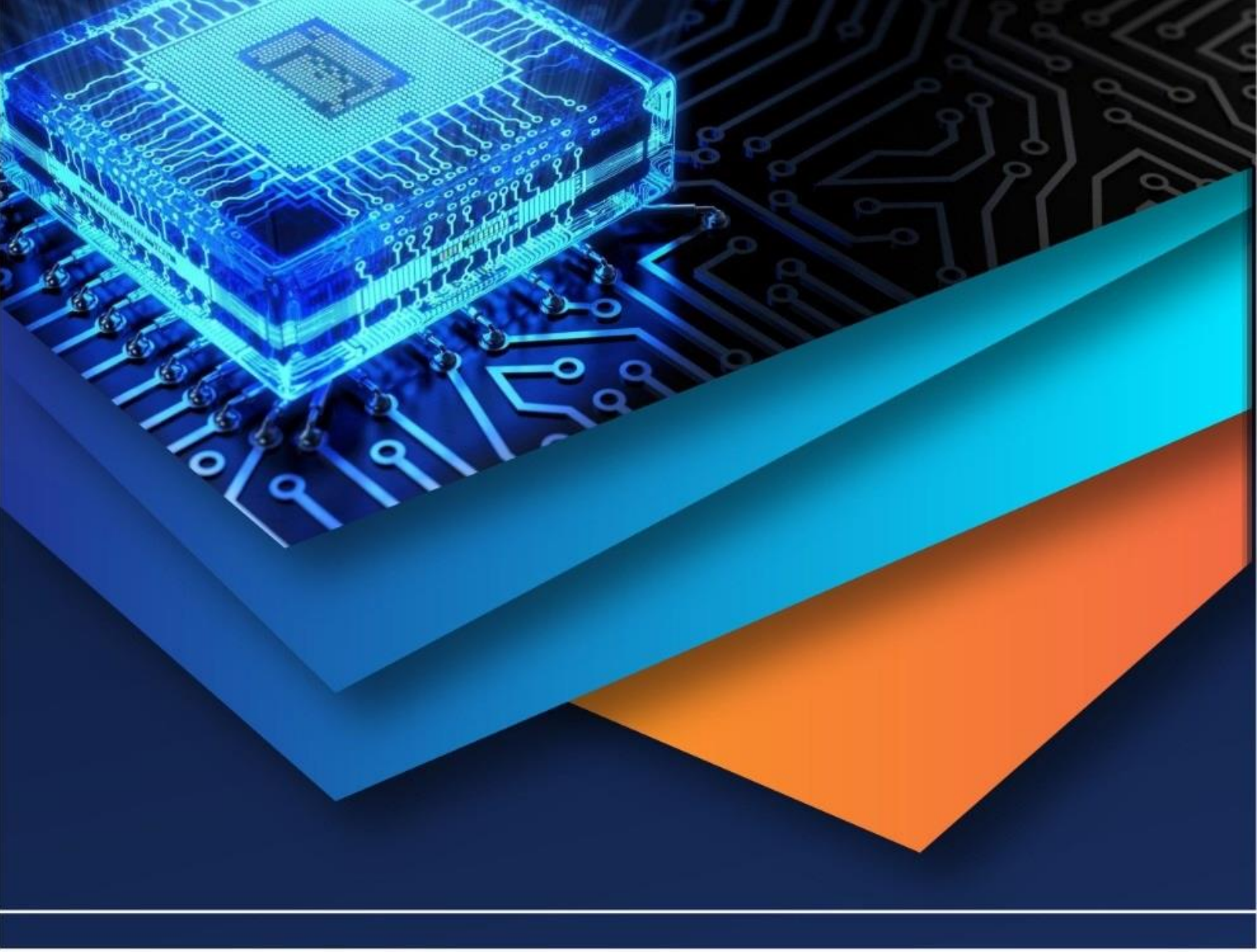
Dr. Avnish Kumar Upadhyay is a Senior Research Engineer at NKT. He experienced Semiconductor Device Engineer with Expertise in working on the development of mechanisms of charge transportation and homocharge accumulation inside the Low Density Polyethylene (LDPE) which is significantly used as the main insulating material in High Voltage Direct Current (HVDC) cables. He completed Postdoctoral Researcher from Chalmers University of Technology, Gothenberg Sweden & Research Scholar from Indian Institute of Technology, Ropar, IIT-R



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