iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 12 **Issue:** VI **Month of publication:** June 2024

DOI: https://doi.org/10.22214/ijraset.2024.63179

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue VI June 2024- Available at www.ijraset.com

PMOS Integrated Current Mirror for Biomedical Applications

Yerra Vivek Sai[1], Uppari Gopi Sagar[2], V. M. Sravan[3], Ms. S. Aruna[4]
[1, 2, 3]*Student,* [4]*Assistant Professor, Department of Electronics and Communication Engineering, Maturi Venkata Subbarao (MVSR) Engineering College, Osmania University, Telangana, India*

Abstract: ***This paper presents the design and implementation of a PMOS integrated current mirror tailored for biomedical applications. Current mirrors are fundamental building blocks in analog circuit design, finding extensive use in various signal processing stages, including amplification, filtering, and signal conditioning, critical in biomedical instrumentation. The proposed PMOS current mirror offers several advantages suited for biomedical applications, such as low power consumption, high input impedance, and compatibility with standard CMOS processes, ensuring seamless integration with other circuitry on a chip. The design focuses on achieving high accuracy and stability to facilitate precise measurement and processing of biomedical signals, essential for applications like biosensing, medical imaging, and neural interfacing. Simulation results demonstrate the efficacy of the proposed PMOS current mirror in meeting the stringent performance requirements of biomedical devices while offering robustness against process variations and environmental noise. This work contributes to advancing the state-of-the-art in integrated circuit design for biomedical applications, promising enhanced reliability and efficiency in next-generation healthcare technologies.***

I. INTRODUCTION

Numerous biomedical applications necessitate current sources and mirrors with substantial voltage compliance and high output impedance. For instance, in implantable micro-stimulators, precise current sources and sinks are crucial for finely controlling the injected charge during stimulation. The advancements in CMOS technologies have facilitated the integration of various functionalities, including radio-frequency circuits, baseband signal processing, and sensors, onto a single chip. Achieving ultra-low power consumption and operating at supply voltages of 1 V or lower is paramount to prolong battery life over extended periods. Recent deep sub-micron CMOS technologies have emerged as promising candidates for meeting these requirements. These technologies allow transistors to operate in weak inversion up to the GHz range with reasonable gain, thanks to their low threshold voltage. However, the decreasing supply voltage, coupled with the low output resistance of transistors in deep sub-micron CMOS processes, presents challenges in implementing current mirrors and sources or sinks with very high output impedance across a wide output voltage range.

II. LITERATURE SURVEY

1) M. Ghovanloo proposed the VLSI circuits for Biomedical Applications . He has presented the state-of-the-art overview of VLSI Circuit Design but it is applicable only for Biomedical technology.
2) J. RamirezAngulo, R. Carvajal and A. Torrabla rsented the Low Suply Voltage High -performance CMOS Current Mirror with Low input and output voltage requirements. They have achieved low input resistance but it has large Bandwidth.
3) B. Minch proposed the Low-Voltage Wilson Current Mirror in CMOS. He proposed the Current Mirror Concept which copies the Current accurtely but it requires Four active devices.

III. AIM, OBJECTIVES AND ADDITIVE CIRCUIT

A. Aim

The main aim of the project is using the current mirror concept in Biomedical applications for sensing and amplifying bioelectric signals using common source buffer circuit.

B. Objectives

The objectives of the project are

1) Designing and simulation of PMOS integrated Current Mirror in Cadence Virtuoso tool.
2) Measurement of parameters of the designed Circuit by connecting the common source MOSFET .

3) Analysis and comparison of results of the measured parameters of designed and simulated with already existing or proposed methods.

C. Additive Circuit

The Additive circuit that we are adding to the project is connecting a Common Source Buffer to the PMOS Integrated Current Mirror and Compare the Current , output Impedances and Gain of the Circuit after connecting the Buffer with the already proposed methoods like Basic Current Mirror ,Super-Wilson Current and PMOS current Mirror Circuits.

IV. SOFTWARE USED

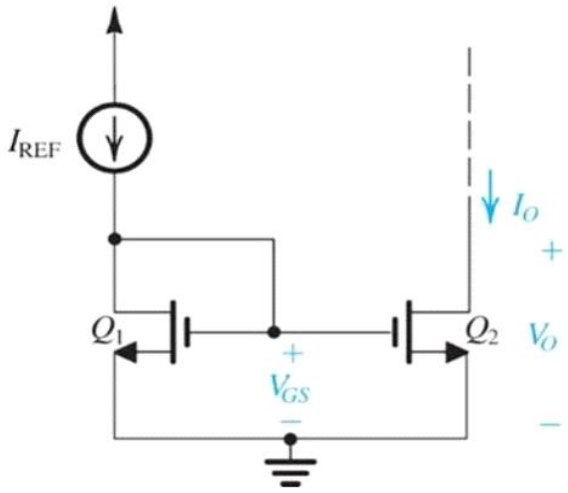
Cadence Virtuoso is a prominent Electronic Design Automation (EDA) solutions provider, offering a comprehensive suite of tools for analog, mixed signal and integrated circuit (IC) design. It provides a suite of tools and features that enable us to process the design from initial schematic capture to final layout and verification.

The Key features of Cadence Virtuoso are Schematic Capture, Layout Editor, Simulation and Analysis, Design and Rue Checking, Physical Verification, Parametric Analysis and Custom Design.

The main Advantages of Cadence Virtuoso over other platforms are:

High precision, Comprehensive toolset and Industry Standard.

V. BLOCK DIAGRAMS

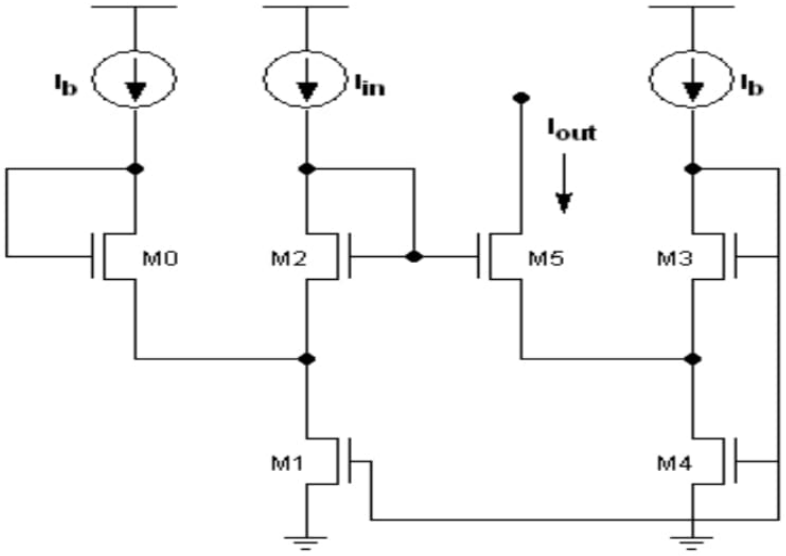


A. Basic Current Mirror

A basic current mirror is a fundamental analog circuit that replicates the current flowing through one transistor to another, typically using two or more transistors. In its simplest form, it consists of a master transistor, through which the reference current flows, and a matching transistor, which mirrors this current. By biasing the transistors appropriately, the mirrored current closely matches the reference current, making it useful for biasing circuits, current steering, and load balancing applications in integrated circuits. The ratio of the mirrored current to the reference current is determined by the geometry and operating conditions of the transistors, offering a straightforward means of current amplification or regulation.

In a basic current mirror circuit, when a reference current flows through the master transistor, it creates a voltage drop across a resistor. This voltage is then applied to the gate or base of the matching transistor, causing it to adjust its conductance to mirror the current, resulting in an output current that closely matches the input current. The matching transistor operates in the active region, ensuring a high output impedance and faithful replication of the input current within the constraints of the transistor characteristics and circuit design.

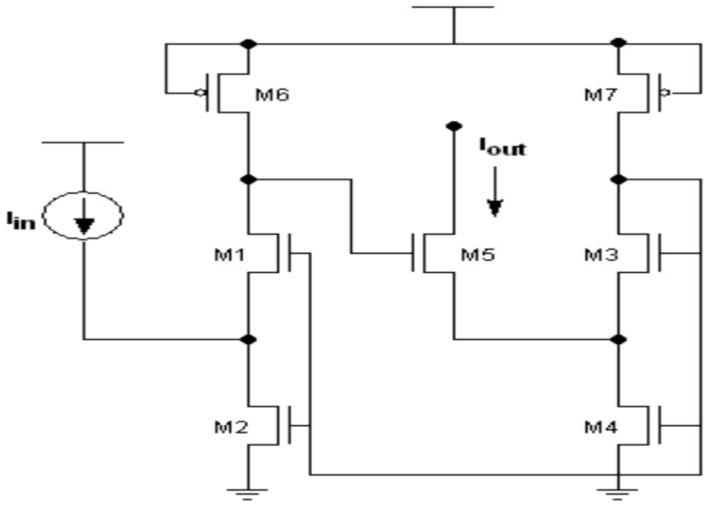
B. Super-Wilson Current Mirror



Super-Wilson Circuit

The described circuit adopts a high-swing super-Wilson configuration, leveraging negative feedback for robust output impedance, as illustrated in Figure 1. Through a network of transistors M1-M4, it establishes a current mirror, which monitors the output current (Iout) against the input current (Iin). Adjustments to the gate voltage of M5 occur based on the disparity between these currents, ensuring that Iout remains in parity with Iin. The output impedance (rout) correlates directly with the loop gain, determined by the interplay between the Common Source amplifiers M1 and the current source load. In this high-swing super-Wilson setup, rout can be approximated as gm1r01r05, where gm1 and r01 pertain to the transconductance and output resistance of M1 respectively, and r05 signifies the output resistance of M5. Additionally, a low-voltage current mirror configuration, as depicted in Figure 2, refines the super-Wilson structure by integrating a diode-connected transistor within the input current arm, bolstering gain as gmrout. Both configurations achieve drain symmetry for the current mirror transistor pair through the auxiliary current source.

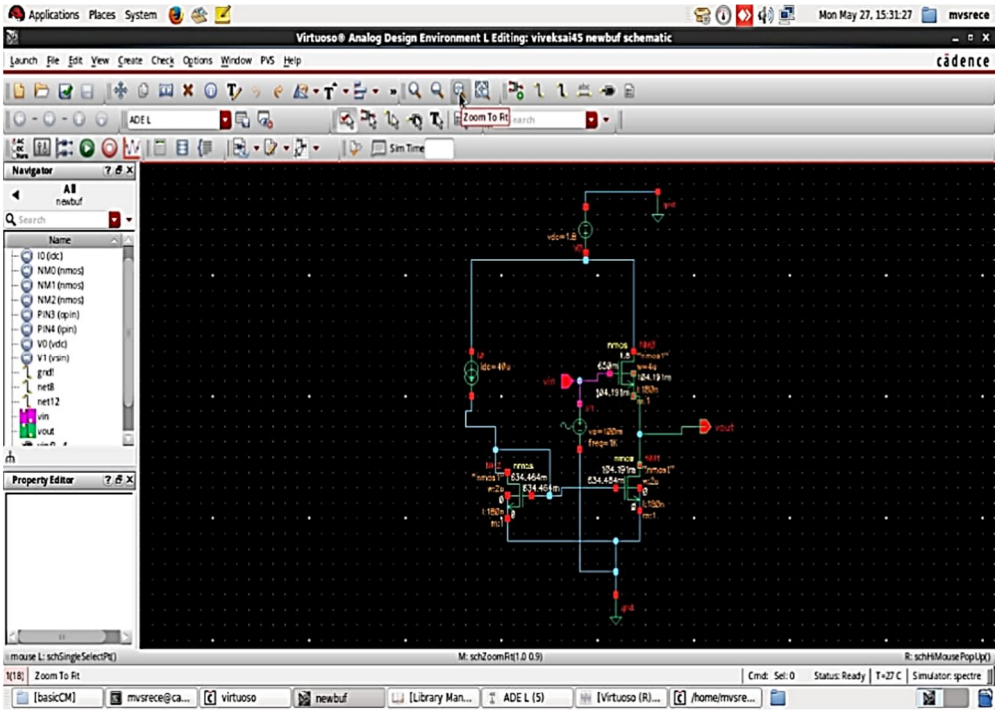
C. PMOS Integrated Current Mirror



PMOS Current Mirror Circuit

In the proposed design, achieving drain symmetry for transistors M2-M4 is innovatively accomplished without relying on an auxiliary current source. Instead, the auxiliary current source is replaced by a diode-connected PMOS. This substitution allows for a more streamlined and efficient circuit configuration. Transistors M2-M4, which are integral to the current mirror functionality, play a crucial role in achieving high output impedance, enhancing the overall performance of the circuit. Furthermore, the diode-connected transistor M1 is reconfigured to a cascode arrangement, optimizing its operation within the circuit. These design modifications facilitate the precise comparison of the output current (Iout) with the input current (Iin) by leveraging the behavior of transistor M5. Additionally, diode-connected transistors M6-M7 serve as active loads, contributing to increased output impedance and improved output current characteristics, thereby enhancing the overall functionality and efficiency

VI. SCHEMATIC DESIGN AND SIMULATION RESULTS

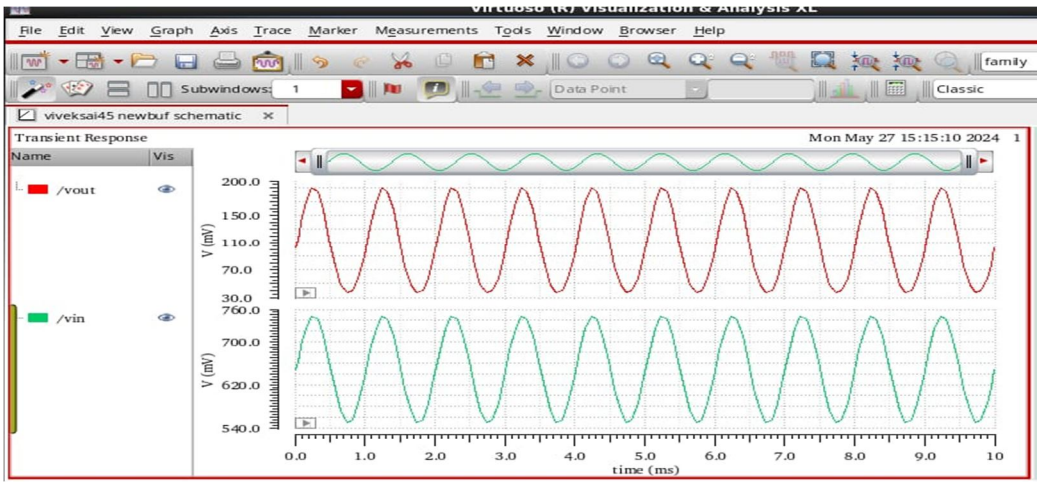


Basic Current Mirror circuit

AC Response

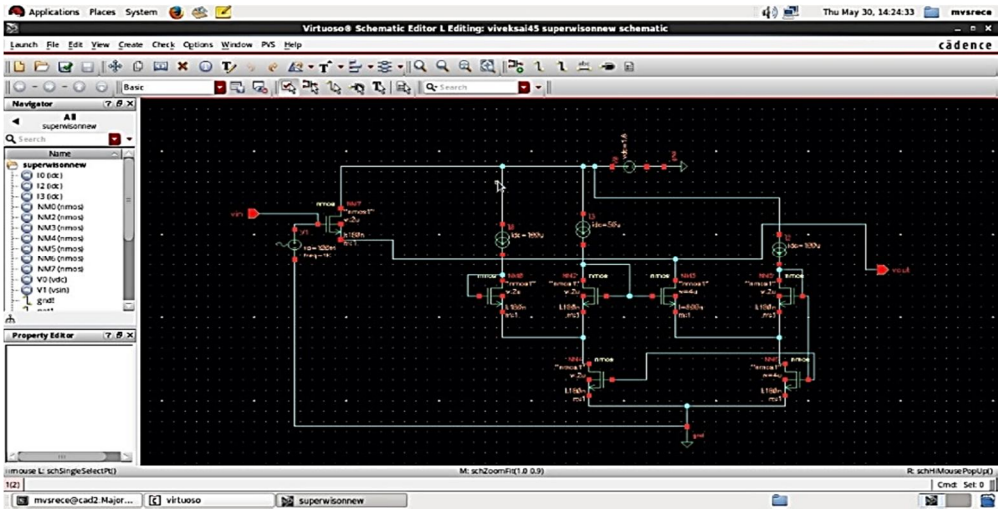
International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue VI June 2024- Available at www.ijraset.com

DC Response

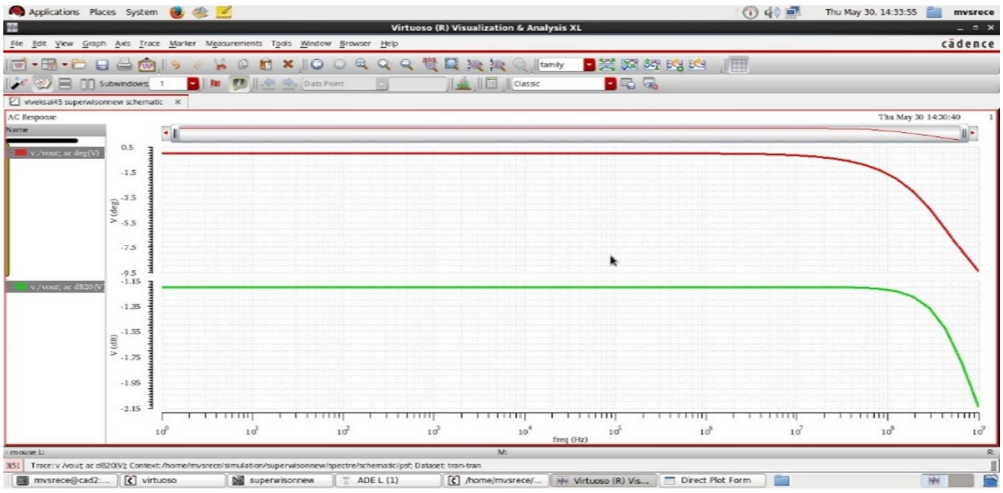


Transient Response

A. Super-Wilson Responses



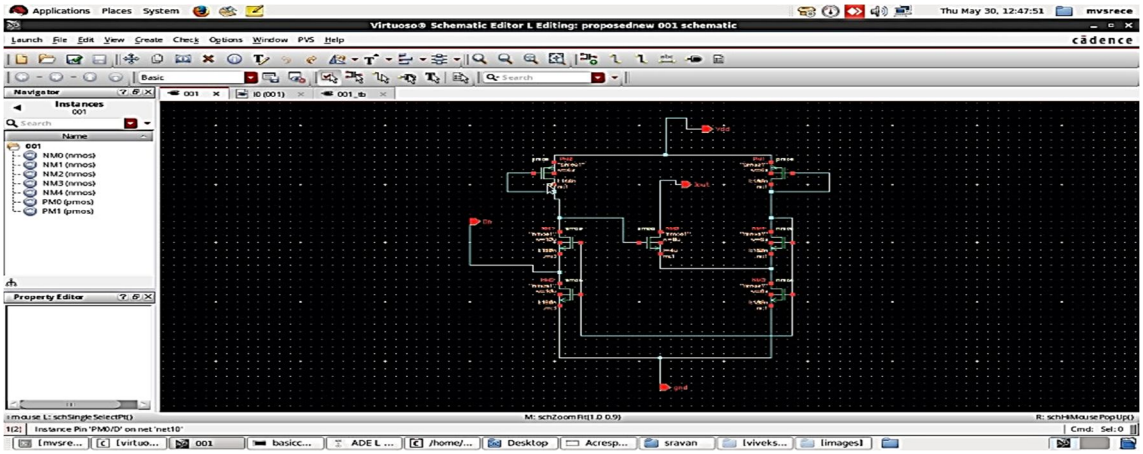
Buffer circuit using Super Wilson current mirror



AC Response

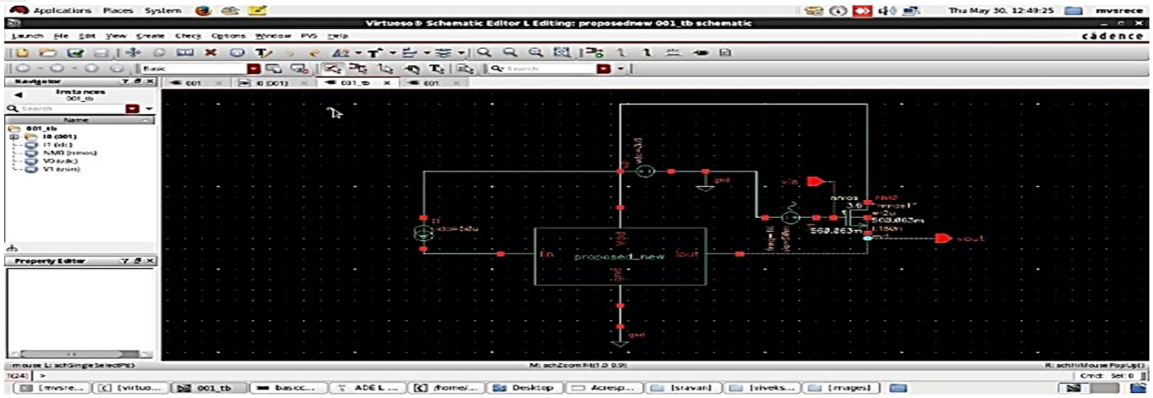
DC Response

B. Proposed Current Mirror Responses



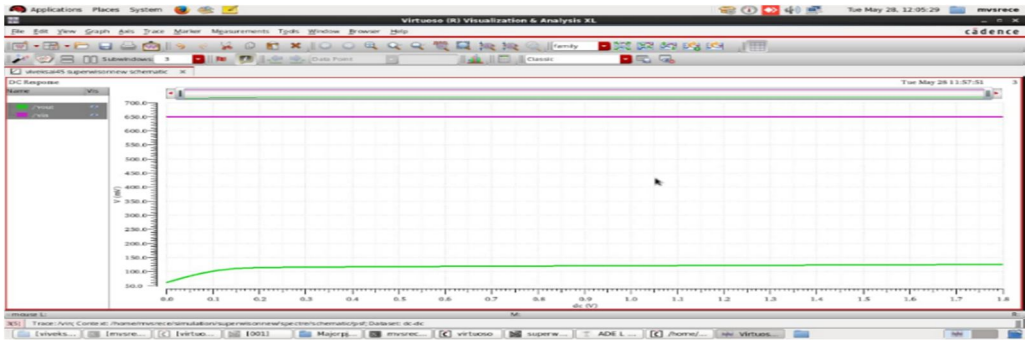
Proposed Current Mirror Circuit

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue VI June 2024- Available at www.ijraset.com

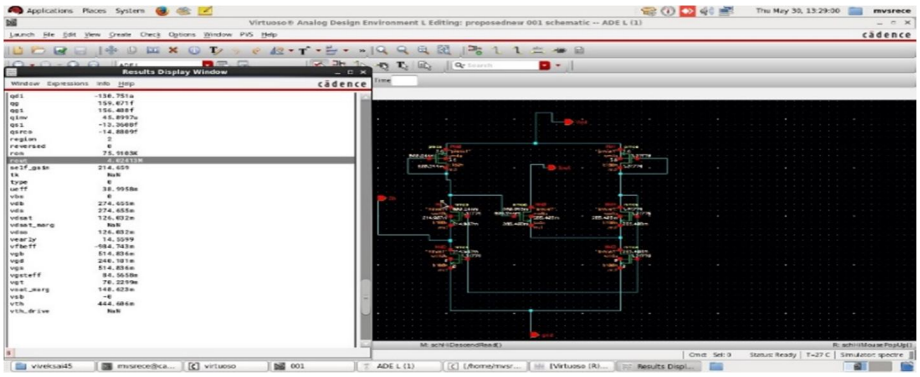


Buffer Circuit using Proposed current mirror

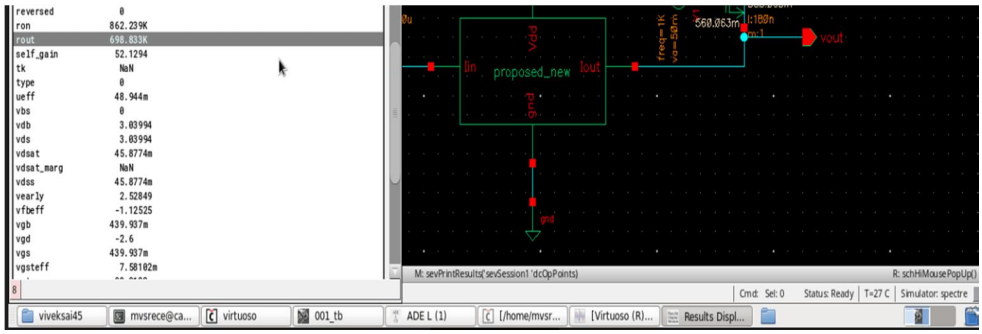
AC Response



DC Response



Load Impedance(R_L)



Output Impedance(R_0)

VII. EXPERIMENTAL RESULTS

S.no		CURRENT		NET OUTPUT IMPEDANCE(R_0^1)	GAIN
		I_{in}	I_{out}		
i	Basic Current Mirror	40uA	37.7uA	2.8k ohms	-0.4dB
ii	Super-Wilson Current Mirror	40uA	38.8uA	4.9k ohms	-0.36dB
iii	Proposed Current Mirror	40uA	39.2uA	595.427k ohms	-0.2dB

VIII. CONCLUSION

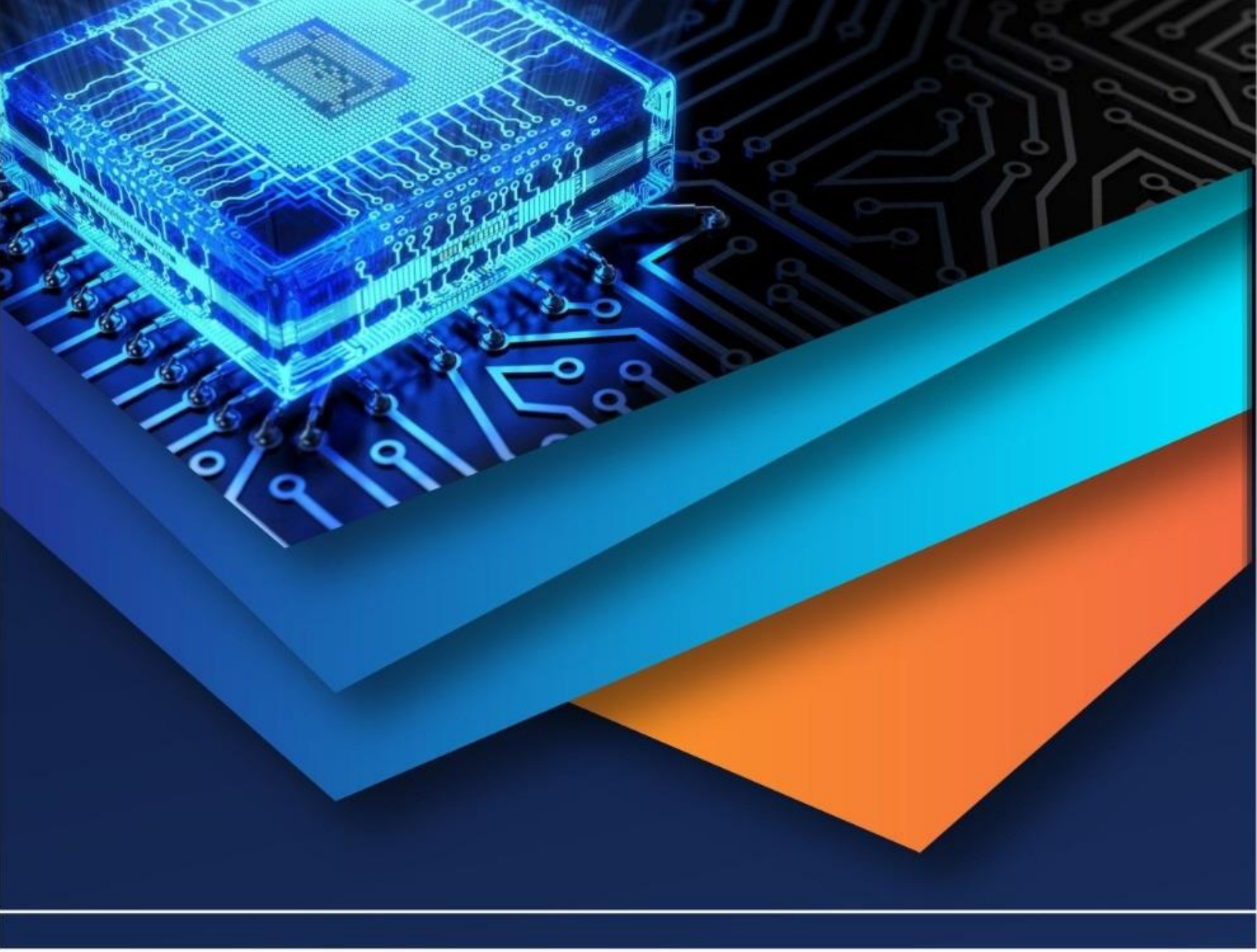
The proposed circuit features extremely high impedance due to the presence of PMOS transistors in both branches, without the use of any auxiliary biasing circuits. This makes it suitable for applications operating at very low currents. Additionally, the circuit can be adapted to achieve very high impedance in the weak inversion region, particularly useful for ultra-deep sub-micron technology. By omitting the auxiliary current source, negative leakage currents can be completely eliminated in the weak inversion region, thus minimizing noise interference in implantable chips.

IX. FUTURE SCOPE

The future scope of PMOS integrated current mirrors in biomedical applications is promising. These devices can be further optimized for low power consumption, making them ideal for implantable medical devices where energy efficiency is critical. Advances in technology could enable even higher impedance and lower leakage currents, enhancing performance in sensitive biomedical environments. Additionally, their ability to operate at very low currents makes them suitable for emerging applications in biosensing and neural interfacing, where precise and stable current regulation is essential. Integration with ultra-deep sub-micron technology could also lead to more compact and efficient designs, facilitating the development of next-generation biomedical implants and diagnostic tools.

REFERENCES

[1] M. Ghovanloo, VLSI Circuits for Biomedical Applications. Artech House, 2008, ch. 10, pp. 191–205.
[2] B. Gosselin, M. Sawan, and C. Chapman, “A Low-Power Integrated Bioamplifier With Active Low-Frequency Suppression,” Biomedical Circuits and Systems, IEEE Transactions on, vol. 1, no. 3, , Sept. 2007, pp. 184–192.
[3] L. F. Tanguay and M. Sawan, “An Ultra-Low Power ISM-Band Integer-N Frequency Synthesizer Dedicated to Implantable Medical Microsystems,” Analog Integrated Circuits and Signal Processing, 2007, pp. 1573–1979.
[4] J. Ramirez-Angulo, R. Carvajal, and A. Torralba, “Low Supply Voltage High-Performance CMOS Current Mirror with Low Input and Output Voltage Requirements,” IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. (USA), vol. 51, no. 3, 2004, pp. 124–129.
[5] B. Minch, “Low-Voltage Wilson Current Mirrors in CMOS,” in IEEE ISCAS, New Orleans, LA, USA, 2007, pp. 2220–2223.
[6] Louis-Franc¸ois Tanguay, Mohamad Sawan, and Yvon Savaria, “A Very-High Output Impedance Current Mirror for Very-Low Voltage Biomedical Analog Circuits,” Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference, 2008, pp. 642-645.
[7] A Very- High Impedance Current Mirror For Biomedical Applications Raguvaran F ,Deepak Prasath .N , Alexander J and Santhanalakshmi .M.
[8] G. R. Wilson, “A Monolithic Junction FET—n-p-n Operational Amplifier” IEEE Journal of Solid-State Circuits, vol. SC-3, no. 4, pp. 341–348, 1968.
[9] B. A. Minch, “A Low-Voltage MOS Cascode Bias Circuit for All Current Levels,” in Proc. ISCAS’02, vol. 3, Phoenix, AZ, May 2002, pp. 619–622.
[10] B. L. Hart and R. W. J. Barker, “D. C. Matching Errors in the Wilson Current Source,” Electronics Letters, vol. 12, no. 15, pp. 389–390, 1976.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY