iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 10 **Issue:** XI **Month of publication:** November 2022

DOI: https://doi.org/10.22214/ijraset.2022.47381

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue XI Nov 2022- Available at www.ijraset.com

Power Minimization by Designing Novel Architecture for Multimodal Biometric System

Mrs. Manasa M G[1], Dr. Gayathri S[2],
[1]*Assistant professor Department of ECE, MIT, MYSURU, Karnataka-571477, INDIA*
[2]*Associate Professor, Department of ECE, SJCE, MYSURU, Karnataka, 570006, INDIA*

Abstract: ***The reduction of power, area, and delay parameters are increasing as the range of sophistication of applications in VLSI circuit designs. Adders and multipliers play a vital role in VLSI circuit designs to minimize the power consumed by the circuit. The Finite Impulse Response Filter is widely used in Digital Signal Processing Applications, such as speech processing, loudspeaker equalization, echo cancellation, noise cancellation, arithmetic computations and, image-processing applications. In FIR filter, the adders and multipliers are the important components to reduce the power, delay and area. Therefore, this proposed method faced with more constraints: as minimal power as possible. This work proposes a design of low power Finite Impulse Response Filter using Carry Skip Adder.The recent electronics industry uses digital filters for various real time applications. A novel VLSI architecture is designed by using ALU based FIR filters for biometric system. Where in ALU includes adders and multipliers, comparing different adders for there better performance with respect to power and identifying carry skip adder will consume less power compared to other adders. power consumption of overall architecture by including carry skip adder is very less and we can use this same adder for multimodal architecture also.***
Keywords: multimodal biometric,carry skip adder, power minimization.

I. INTRODUCTION

Filters are one of the most important components of an architecture involving in authentication or certification. In digital signal processing filters usually define an impulse response and the input is convolved with the impulse response to produce the desired filtered output.

In computerized signal handling applications, advanced channels are the in particular utilized component [1]. Filters can take different forms and can be defined across various domains depending on the applications. The terminology given to these filters is used to describe the behavior based on the frequency response provided as an output at each stage. Biometric-based authentication also involves the use of filters in almost every stage of authentication. Effective VLSI engineering for FIR channel configuration utilizing altered differential development insect state advancement calculation is done in paper [3] an optimized VLSI filter architecture is proposed that and has minimal power dissipation for multimodal biometric systems. It centers around fulfilling the financial force usage and furthermore the determinations in the recurrence space.

Biometric systems are rapidly evolving and are replacing the traditional security systems that included passwords, pin codes, or printed IDs. It uses the physiological or behavioral characteristics of a person usually in the image form to identify and authenticate. It is being integrated into smartphones, smartwatches, laptops, etc. enabling biometric login to keep their phones or pieces of equipment from unauthorized intervention. The conventional biometric system uses a single physiological characteristic in an image format namely iris or fingerprint to face or voice recognition. However critical authentications may not restrict the verification method just to a single factor and may include multiple biometric features to be matched and verified before attestation. Highly sensitive research laboratories have ratified the use of multi-modal biometric systems to secure their eminent labs from any sorts of trespassers' uncertified entry. Any reliable biometric system has to be fast, accurate, and compatible.

Biometric systems take images of various distinguishing features of the human body as input and image processing is a decisive procedure in verifying the person based on the images produced. Image processing subject the input image into some of the adamant processes that could persistently use filtering techniques to achieve the required task. A biometric system consists of three steps – preprocessing, trait detection or feature extraction, and classification. The preprocessing stage consists of filtering techniques that perform shape creation, texture overlaying, image cropping, or wavelet transformation.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue XI Nov 2022- Available at www.ijraset.com

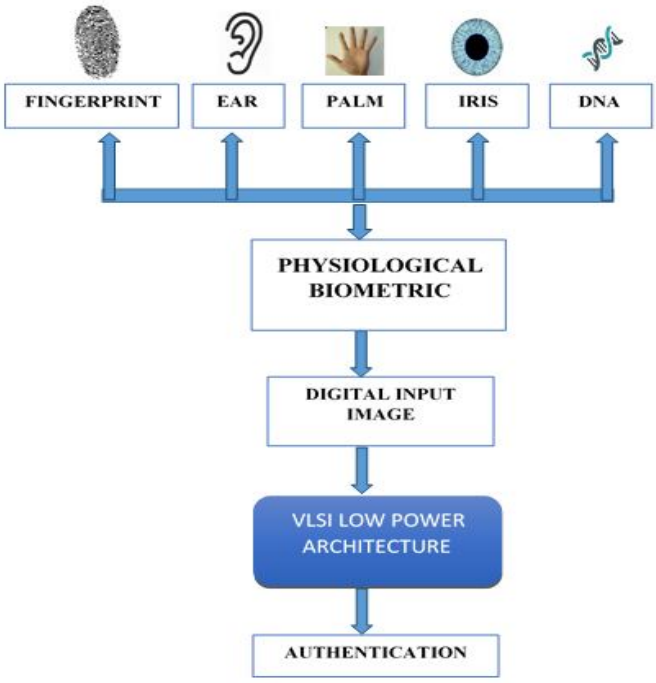


Figure 1: Flow diagram of multi-modal biometric system

Discrete wavelet changes or DWT is utilized to break down the given sign into a few sets, where each set addresses the time series of the coefficients portraying the time advancement of the sign in the comparing sets of the recurrence band. It ordinarily returns the vector that is of a similar length as the information signal. It utilizes a discrete arrangement of wavelet scales and interpretations which comply for certain characterized rules. All in all, the sign is decayed into a commonly symmetrical arrangement of wavelets.In [2], the authors use the wavelet transform for biometric systems based on the heartbeat. They perform wavelet denoising, for detection of peak heartbeat and feature extraction.

In [3], the creators propose an engineering that comprises of a DWT handling unit and a double memory regulator. The inward transports deal with perusing and composing activities between the processor. In this engineering, the peruse and compose activities happen in equal. The important equal and pipelining preparing is dealt with in the plan which makes the control plan less complex and proficient. The test seat of the DWT processor would comprise of the processor and the social model of the double port recollections. The creators have tried and mimicked the plan at each level of the plan cycle to check the usefulness prior to sending the calculation on FPGA. The register semiconductor rationale is depicted in equipment portrayal language and tried by recreation of the relating test seat. In view of the acquired outcomes, the originator can blend the plan and guide the got netlist to be changed over to door level plan.

In [4], authors creators configuration lifting-based DWT, utilized for delay effective lifting based DWT is to play out the entire activity with numerous preparing components in equal carried out with 45 nm innovation. In [6], the creators propose a productive Finite State Machine (FSM) based reconfigurable engineering for finger impression acknowledgment. The unique mark picture is resized, and Compound Linear Binary Pattern (CLBP) is applied to the finger impression, trailed by the histogram to get histogram CLBP highlights. Discrete Wavelet Transform (DWT) Level 2 provisions are gotten by a similar technique. The clever coordinating with score of CLBP is figured utilizing histogram CLBP provisions of the test picture and unique mark pictures in the information base.

In this paper, the VLSI architecture is presented for the wavelet transformation performed on these images by optimization of adders in the GPDK90 technology. Generally, any filter contains adders, and hence optimizing the adders to have minimal power dissipation can reduce the power dissipation of the overall architecture. In [5], The authors compare the power dissipation of different adder topologies in CMOS technology. With the use of microwind tool, 7 different adder topologies are compared and analyzed for Area, Delay, and consumption of power. Results show that with 288 gates, RCA (Ripple Carry Adder) consumed the least power. In [7], a clever 24 semiconductor Latch Adder (LA) is proposed.

It is approved utilizing the Wallace tree multiplier as a benchmarking circuit. Wallace tree multiplier is carried out utilizing the proposed lock snake and postpone lines in the inside hubs. Correlation is made with the multipliers developed utilizing different full snake setups accessible in the writing.

In this paper, we use the cadence virtuoso tool with the GPDK90 library to design and compare the adders concerning power consumption. Further, a VLSI architecture for the filter used in the multimodal biometric system is designed and simulated in the cadence tool by the use of optimized adders.

II. METHODOLOGY

Efficient Architecture for multimodal biometric system for low power system consists of D-Flip Flop, Shifter and adder as shown in Fig7. The proposed architecture is designed with carry skip adder as a main datapath block. In the architecture block, x[n] is the input to the architecture and the further steps continues with the Low power FIR filter.

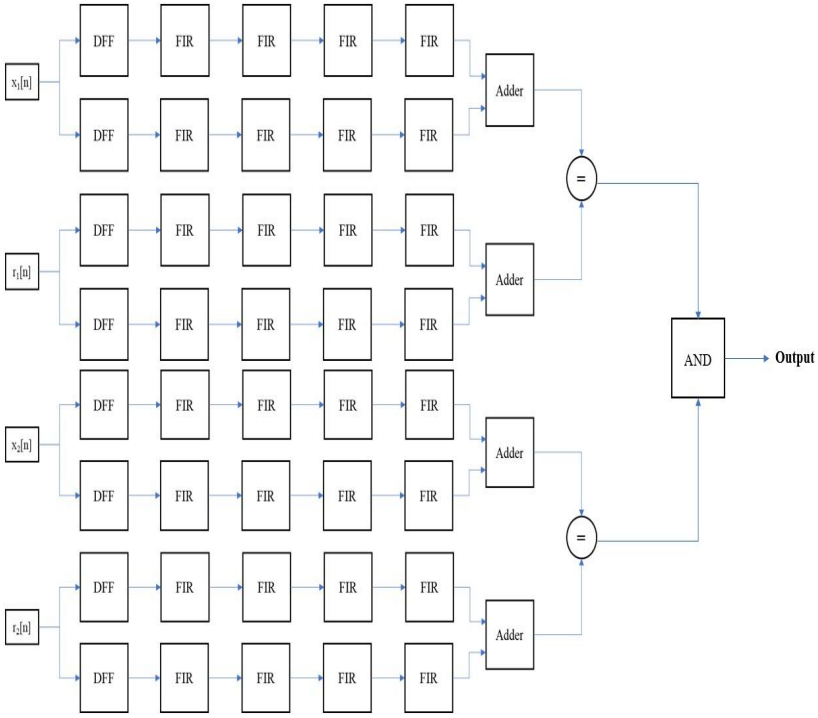


Figure 2: Block diagram of proposed multi-modal biometric system

The 2D array of Gray scale image is converted to 1 dimensional array by tracing method as shown in fig 5.The 1D DWT architecture comprises of the flip flops, adders and shifters implemented output. Once the ray tracing phenomenon is used to convert a two dimensional image into one dimensional image, this one dimensional image vector a subjected to DWT using the filter designed below. This architecture can be used for multimodal biometric as well. Series of filters are cascaded to produce the multiple authentications.

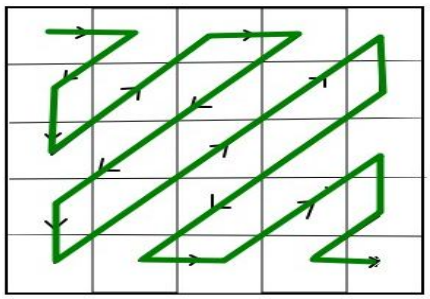


Figure 3: Tracing technique.

The converted 1D array is processed through the D Flip Flop of 8 bit at a time along with shifters and adders which is the actual work carried out in the research. The obtained 8 bit is processed to the datapath blocks present in the architecture as input. The general equation suggests the FIR filter to have coefficients multiplied with each shifted position to give the filtered output.
The adder used here is the carry skip adder for the 8 bit adds operation. From the preliminary analysis, it was noted that the CSA has lower power dissipation compared to the other adders which perform similar operation. The reduction of power is observed due to this optimisation of the adder operation.

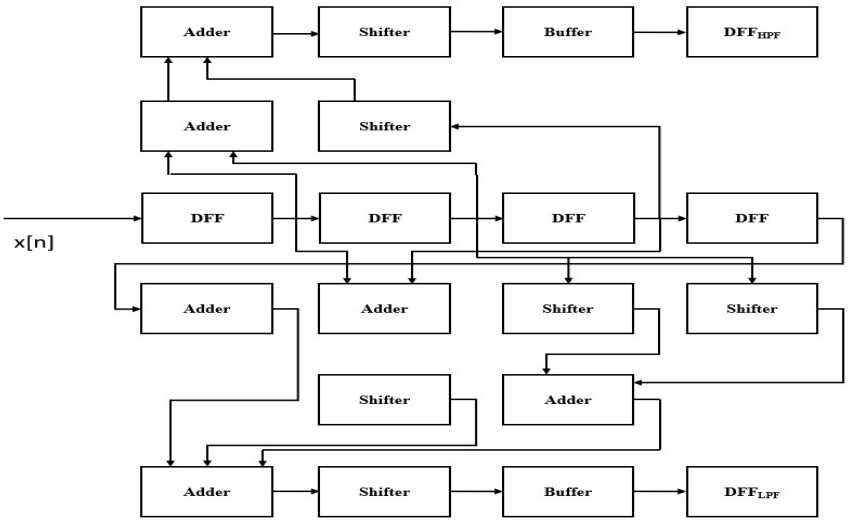


Figure 4: Reconfigured architecture for low power FIR filter

III. RESULT

All the three adder units designed in Cadence Virtuso with 90GPDK technology. The power analysis sya that the leat power consuming adder unit among three adders is the carry skip adder unit with peak pwer consumption of 551.55nW. Hence this result gave a reason to design the new architecture as mentioned below in the design.

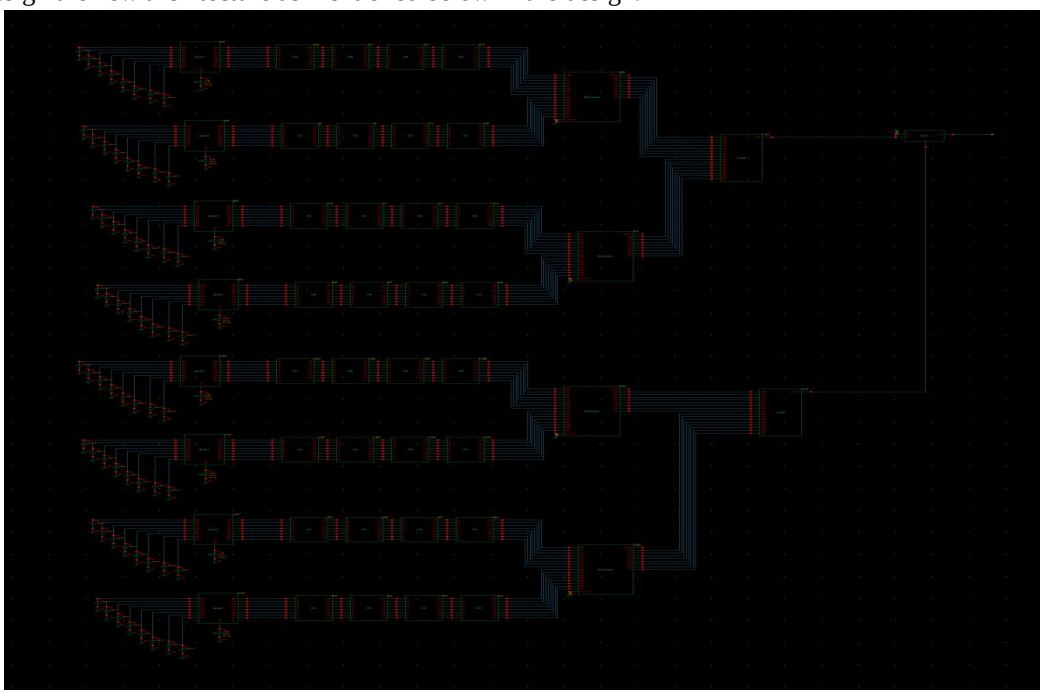


Figure 5:RTL schematic of proposed multimodal biometric system

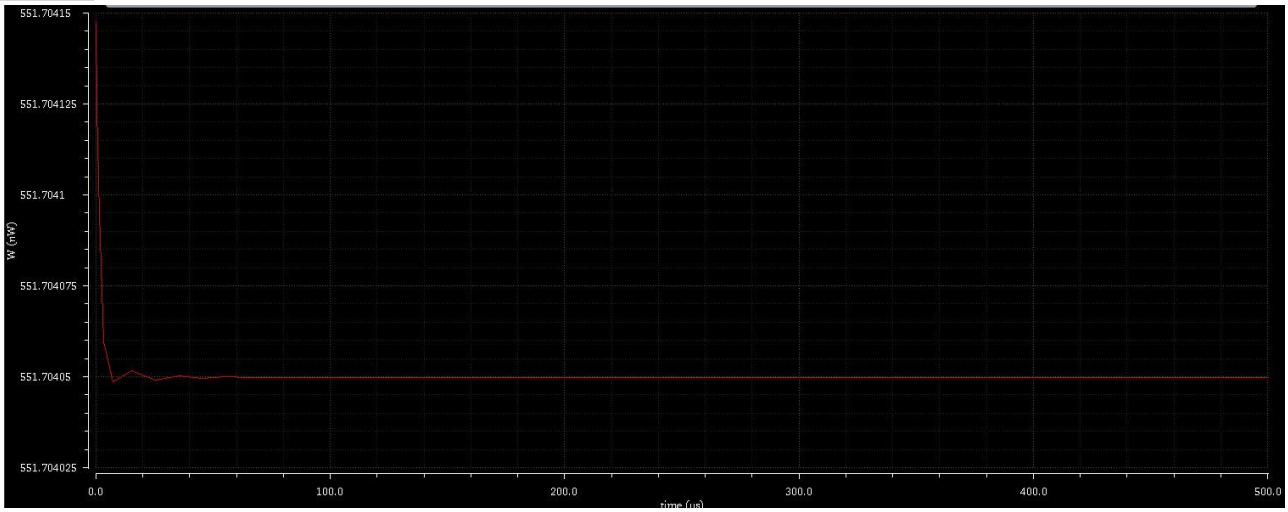


Figure 6: power dissipation of carry skip adder

REFERENCES

[1] "Performance Analysis of FIR Digital Filter Design Technique and Implementation" Mohd. SayeeduddinHabeeb and Zeeshan Ahmad, International Journal of Advanced Research in Electrical and Electronics Engineering Volume: 2 Issue: 2 14-Feb-2014.

[2] "Development of Heartbeat Based Biometric System Using Wavelet Transform" Chin Chee Yeen, Journal of Engineering Science, Vol. 14, 15–33, 2018

[3] "Efficient VLSI architecture for FIR filter design using modified differential evolution ant colony optimization algorithm", John, T.M. and Chacko, S. (2020), Circuit World,

[4] "Lifting-Based Fractional Wavelet Filter: Energy-Efficient DWT Architecture for Low-Cost Wearable Sensors",MohdTausif, Hindawi Advances in Multimedia Volume 2020, Article ID 8823689.

[5] "Area, Delay and Power Comparison of Adder Topologies", R.UMA, International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012.

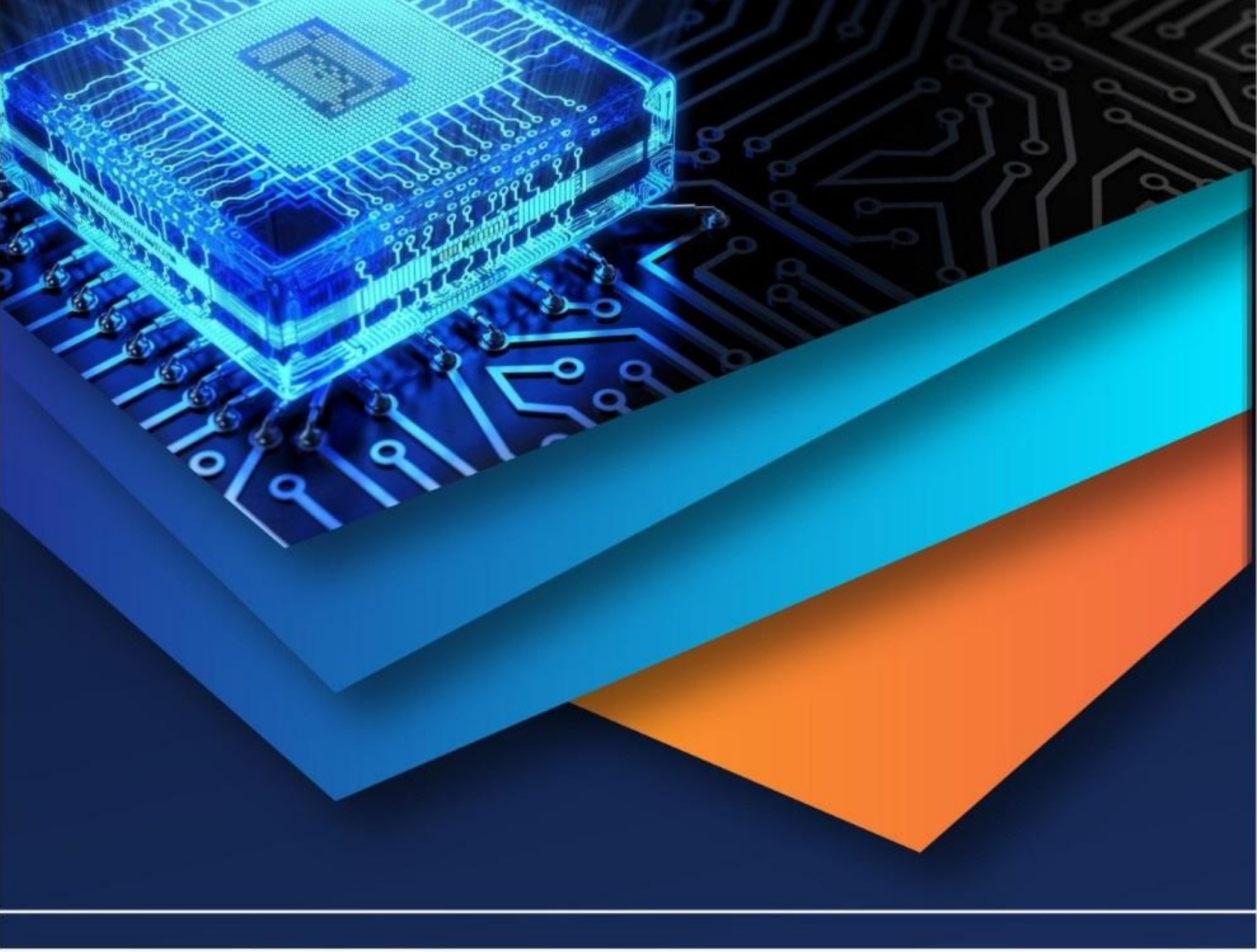
[6] "An Efficient Reconfigurable Architecture for Fingerprint Recognition", Satish S. Bhairannawar, Hindawi Publishing Corporation VLSI Design Volume 2016, Article ID 9532762.

[7] "A Low Power Multiplier using a 24-Transistor Latch Adder", Savio Victor Gomes, Indian Journal of Science and Technology, 2015.

[8] "A Design of Low Power and Area efficient FIR Filter using Modified Carry save Accumulator method", L Mohana Kannan1 , D Deepa2,Turkish Journal of Computer and Mathematics Education Vol.12 No. 7 (2021), 1735-1750.

[9] "Analysis And Design Of Fir Filter Using Modified Carry Look Ahead Multiplier", 1*S. Dhanasekaran, 2 T.Thamaraimanalan, 3 V.Anandkumar , 4A.Manikandan INTERNATIONAL JOURNAL OF SCIENTIFIC & TECHNOLOGY RESEARCH VOLUME 9, ISSUE 03, MARCH 2020 ISSN 2277-8616.

[10] "DESIGN AND IMPLEMENTATION OF AN EFFICIENT CARRY SKIP ADDER"JisneySussan Joy1, Premanand B 2,Volume: 04 Issue: 06 | June -2017 International Research Journal of Engineering and Technology (IRJET)



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY