iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 12 **Issue:** VIII **Month of publication:** August 2024

DOI: https://doi.org/10.22214/ijraset.2024.63869

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue VIII Aug 2024- Available at www.ijraset.com

Q-EDR Hybrid Boost Converter Operation For High Gain With Low Device Stress

K. Threyini[1], P. Bhavana[2], S.Vinay Kumar[3]
Department. of EEE, JNTU, Hyderabad, India

Abstract: ***The hybrid continuous-discontinuous mode (CCM-DCM) operation of non-isolated systems is proposed in this paper. boost converter with quadratic extended duty ratio (Q-EDR) for applications with high gain and low power. The inductors at the input while the EDR was in continuous conduction mode (CCM) The mode of operation of stage inductors is discontinuous conduction. (DCM) in order to reap the advantages of CCM and DCM operation. Interleaving's ripple in the low input current and low voltage The EDR stage switches' stress remains. With what is being half and half method of activity, the inductance worth of EDR stage significant decrease in the inductor. an additional decrease in switch voltage is accomplished during turn-on progress in the proposed activity, prompting huge decrease thus on exchanging losses. This lets the converter run at higher switching speeds. frequency, thereby reducing EDR inductors' size by 45 percent in this instance an experiment confirms the proposed idea. Simulink prototype for a two-phase Q-EDR operating at 30 V-40 V to 400 V output, a gain of more than 12 at duty close to 0.54. The converter has a peak efficiency of 95.5 percent. at a switching frequency of 135 kHz and 300 W for all silicon switches.***

Index Terms: ***extended duty ratio, quadratic boost, high gain boost, continuous conduction mode, CRM, non-isolated DC-DC, low device stress, intermittent conduction mode, and interleaved inductor, exchanged capacitor setup***

I. INTRODUCTION

Non-confined high increase DC help converters have been getting some decent momentum for sun powered and energy component applications as they can accomplish higher effectiveness with more modest size [1]-[3]. Most of the business PV microinverters require a lift converter to move forward the low voltage from PV boards (under 40 V) of the DC connect voltage of 400 V [4], [5], accentuating the need of a high increase converter. As of late numerous geographies are introduced in the writing which utilize a mix of exchanged capacitors [6], [7], exchanged inductor [8] and voltage multiplier (VM) cells [9] to accomplish the high voltage gain. Aside from these, DCM activity of a few converters has been investigated in writing as it gives higher addition at low obligation, decreases the inductor size and decreases the exchanging misfortunes [10]-[12]. Conventional quadratic boost converter (QBC) is a solitary switch geography which accomplishes quadratic voltage gain at the cost of significant conduction loss and high device stress [13]. QBC's operation and analysis in discontinuous mode (DCM) is presented in [11], which introduces four distinct modes. Among the four modes, DCL2 mode (which works as it were internal inductor in DCM) is guaranteed as a valuable mode for better execution analyzed than CCM. Conductance crucial mode (CRM) activity of QBC is introduced in [14], which works under fluctuating recurrence range with just transitional stage inductors in CRM, while input inductor actually running under CCM keeping up with lower input current wave and simultaneously achieving delicate exchanging activity. A fuel source in [15], application-based QBC is proposed, while another Between the junction of the intermediate capacitor and the high voltage side of the output, a storage element capacitor is added. It looks into the QBC's operation under various DCM variants in terms of operations of the inductor A boost converter with high gain and semi quadratics is presented in [16], where the second stage QBC inductor is substituted for a coupled inductor in order to achieve high gain in a semi quadratic form This gain is greatly influenced by the number of the coupled inductor's turns and its application is challenging. With cuk, a cascaded version of quadratic boost converter and voltage multiplier cells have been examined in [17], [18].

An interleaved inductor, exchanged capacitor coordinated converter is proposed in [19]-[20], to highlight high move forward voltage transformation proportion with a moderate obligation cycle. The converter geography is presented as extended duty ratio (EDR) support converter which can achieve high increase with lower current and across all devices, voltage stress. To broaden the voltage, gain in addition, a cascaded quadratic configuration with an EDR stage (QEDR) is suggested in [21], which is simple to achieve. super high increase with moderate obligation levels, while holding the benefits of using the EDR converter. The operation of DCM the in-depth analysis of the EDR converter and its benefits has been introduced in [12]. This inspires towards the recent investigation into the hybrid operational mode EDR quadratic DC-DC converters were proposed.

In this paper, a hybrid CCM-DCM activity of the Q-EDR architecture is suggested in which EDR inductors function in DCM while input inductors work in CCM. With this suggested methodology, the advantages of DCM in the quadratic stage and CCM in realized are the EDR stages. Higher gain over CCM, reduced device stress, low input current ripple, decreased switching loss, and nearly equal current stress in the switches are only a few of the main advantages of the suggested hybrid method. This plan lowers switch turn-on losses by clamping the switching node voltage to an intermediate capacitor voltage just prior to the switch turn-on transition. Additionally, compared to the CCM scenario, the DCM mode of operation for the EDR stage permits a considerable inductor volume decrease while maintaining extremely low input current ripple. The suggested procedure is confirmed.

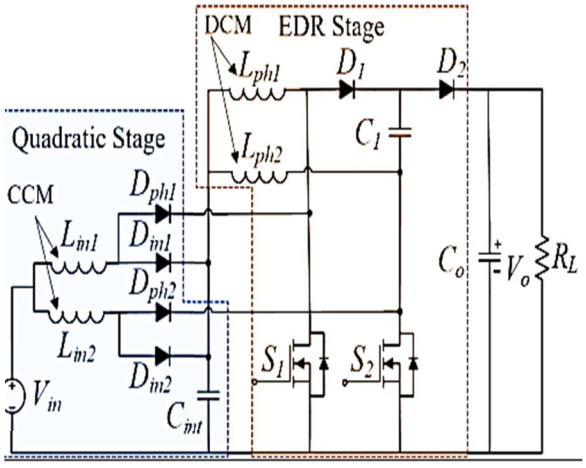


Fig 1. Proposed 2-Phase Q-EDR Converter for hybrid DCM-EDR Operation

II. DISCONTINUOUS MODES OF OPERATION OF Q- EDR

The quadratic converter in CCM is cascaded with EDR to yield Q-EDR topology; the details of this converter operation have already been covered in [21]. A two-stage Q-EDR converter Fig. 1 depicts an EDR converter with a 2-phase EDR stage and an interleaved quadratic stage. The converter is run at a duty of 0.5 and above, with the switches S1 and S2 phase-shifted 180 degrees. It has lower device voltage stress and intrinsic current sharing between the inductors in the EDR stage, just as the EDR converter. The converter can function in three different modes, which are explained below, each of which corresponds to the discontinuous conduction operation of the two sets of inductors (Lin and Ulph).

A. DCM-IN: Input Inductors in DCM

Only the input inductors (Lin1 and Lin2) in this instance are in the discontinuous conduction state. The converter functions and the EDR stage inductors run continuously in this instance, partial DCM. The boundary condition (1) between Lin's CCM and DCM may be obtained in a manner akin to that of traditional QBC. In this case, D′ is defined as the obligation D's complementary (D′ = 1−D). When comparing a 2-phase Q-EDR to a traditional quadratic boost converter, a factor of 2 in (1) is seen, which is in line with the Q-EDR's voltage gain expression in CCM. The critical value of the dimensionless parameter K1 for DCM operation may be found in (1). The worth of K1 is depending on the input inductance value, load resistor and converter switching frequency.

$$K_1 < \frac{DD'^4}{2}; \quad K_1 = \frac{2L_{in}}{R_L T_S} \qquad (1)$$

B. DCM-EDR: EDR Phase Inductors in DCM

In this instance, the input inductors function continuously while only the EDR phase inductors (Lph1 and Lph2) operate in discontinuous mode. The boundary condition between CCM and DCM for EDR stage inductors can be derived similarly to the preceding example and is provided by (2). In this instance, an additional dimensionless parameter K2 is defined, and its critical value for DCM operation can be found from (2). In this instance, the value of K2 is dependent on the EDR stage inductance value, load resistor, and converter switching frequency.

$$K_1 < \frac{DD'^2}{2}; \quad K_1 = \frac{2L_{ph}}{R_L T_s} \qquad (2)$$

C. DCM-IN-EDR: Both Input and EDR Inductors in DCM

In this instance, discontinuous conduction mode is used by the input and EDR stage inductors. Both of the requirements listed in (1) and (2) must be met for the converter to function in full DCM. ought to be fulfilled. The current flowing through each input inductor for Q-EDR in CCM is Iin/2, and the current flowing through the EDR stage of inductor is Iin
(1 − D)/2, where Iin is the net input current of the transform. Operating the converter in either the DCM-IN or DCM-IN-EDR mode will cause a significant current ripple across the input inductors due to the larger current flowing through them, which will increase the losses in the inductor core. This will also cause the net input current to ripple more, which is undesirable for many applications. However, for D ≥0.5, the current through the EDR stage inductors is less than 1/4 of the net input current, necessitating a high inductance value in order to operate these inductors in CCM for a wide range of output power.

As a result, using the converter in DCM-EDR mode is a desirable choice because it greatly lowers the inductance value and EDR stage inductor size. The input the ripple across the EDR stage inductors has no effect on current ripple. Additionally, there is a large reduction in switch voltage during the turn-on transition, which reduces the turn-on switching loss in this mode. This in turn offers the benefit of running the converter at a greater switching frequency, which reduces the size of the inductor even more. The advantages mentioned above lead to a detailed discussion of converter operating in only DCM-EDR mode in this paper.

III. CONVERTER OPERATION IN DCM-EDR CASE

The gain statement for the converter in the proposed DCM-EDR situation is (3). The gain of the converter is a function of load, inductor achieving DCM operation, and switching frequency. A dimensionless parameter α is defined for easy representation. The gain curve for the proposed DCM-EDR operation in comparison to CCM mode is shown in Fig. 2. From the figure, DCM-EDR mode has superior gain compared to CCM case in the entire duty range where the DCM-EDR operation criteria (2) are met, making it a viable option for high gain applications.

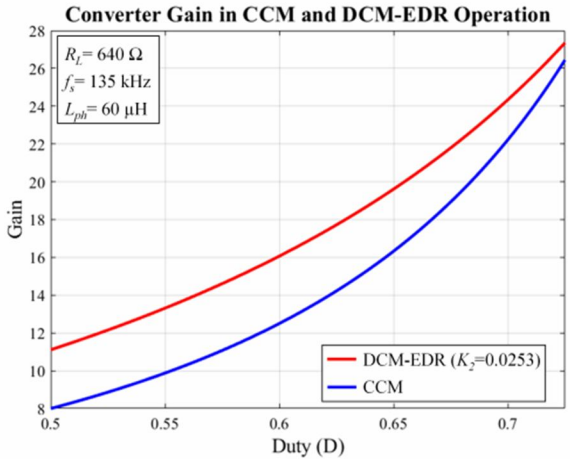


Fig 2.Comparison of gain versus duty for the proposed converter

$$M_{DCM-EDR} = \frac{V_o}{V_{in}} = \frac{\propto}{(1 - D)} ; \propto = \left[1 + \sqrt{1 + \frac{2D^2}{K_2}}\right] \quad (3)$$

If there should be an occurrence of an EDR converter working in DCM as talked about in [12], it be should be visible that during the OFF-stretch. The switch's parasitic drain source capacitance includes in non-ideal reverberation peculiarities and it leads in undesired ringing across the switch voltage causing more pressure and making noise inside the circuit. Using the suggested hybrid, whereas EDR inductors (Lphi) realize DCM with CCM's quadratic stage in operation. During the OFF-stretch, while the (Lphi) current drops down to nothing, and when the The switch drain-source voltage begins to decrease and is clamped. by connecting Dph,i to the voltage of the quadratic stage capacitor (Vcint). in the info circle. Hence, taking out any opportunities for ringing across the switch and the circuit's noise. This also helps. in diminishing the turning misfortune during turn-ON at lower voltage activity of the because it guarantees that it will turn on at a lower voltage. The activity of the Q-EDR converter in DCM-EDR mode is discussed in detail here. The converter activity in DCM EDR mode is like the CCM activity aside from a promotion additional state is added comparing to the broken conduction of the particular EDR stage inductors during the mood killer state.

The converter's various states in one exchanging cycle is summed up in Table. I. The various inductor current waveforms alongside switch voltage and current waveforms north of one exchanging cycle are displayed in Fig.3.The instantaneous circuit diagrams corresponding to Fig. 3. Converter inductor current and switch voltage and current simulation waveforms for the proposed converter in DCM-EDR operating at 32V to 400V at 250W. each interval of converter operation are shown in Fig 4.

1) *Interval I (t0 − t1, t3 − t4):* In this interval, the two switches are simultaneously ON and is same as the converter operation in CCM. Both the input inductors are in charging state and the net input current is equally shared between Lin1 and Lin2. Capacitor Cint discharges through the two EDR stage inductors in this interval. The switch current is equal to the sum of input inductor and EDR inductor of that respective phase.

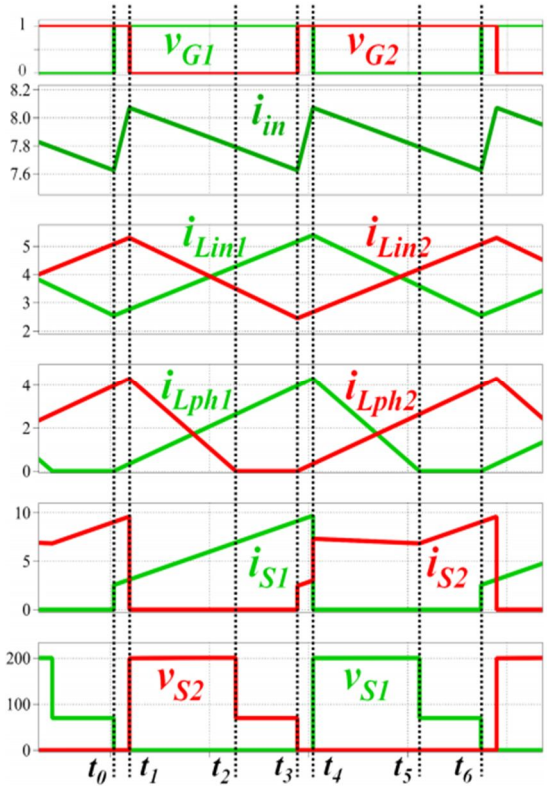


Fig. 3. Converter inductor current and switch voltage and current simulation waveforms for the proposed converter in DCM-EDR operating at 32 V to 400 V at 250 W.

2) *Interval II (t1−t2):* This interval starts with the turning OFF of S2. Lin2 discharges through Din2 to partially charge Cint. Cint still supports the current through Lph1 in this interval.
3) *Interval III (t2 − t3):* This is the discontinuous con duction state for phase 2 EDR stage inductor The current in Lph2 becomes zero resulting in D2 getting reverse biased. The switch node voltage of phase 2 of EDR stage gets clamped to voltage across Cint, thus lowering the voltage stress across S2 significantly just before the switch is turned -ON.
4) *Interval IV (t4 − t5):* In this interval, only S2 is in ON-state and Lin1 is in discharging state. Here, Cint is partially charged through iLin1 flowing through diode Din1 while simultaneously supporting the current through Lph2.
5) *Interval V (t4−t5):* This is the discontinuous conduction state for phase 1 EDR stage inductor. The current in Lph1 becomes zero resulting in D1 getting reverse biased. The switch node voltage of phase 1 of EDR stage gets clamped to reduce the stress caused by voltage across Cint significantly across S1 prior to its activation in the following interval. It can be seen from Fig. 3 that peak switch current stress in contrast to CCM, the switches in both systems are identical. Operation of Q-EDR. Also, the high current ripple across EDR stage inductors have no effect on the ripple of the input current. Because of interleaving as well, input current ripple is still low. CCM operation of the info stage inductors, thus, making it suitable for PV applications.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue VIII Aug 2024- Available at www.ijraset.com

TABLE I

CONVERTER OPERATION IN DIFFERENT INTERVALS OF DCM-EDR

Interval	Duration	Switch State	Inductor State*				Switch Stress			
			L_{in1}	L_{in2}	L_{ph1}	L_{ph2}	V_{S1}	V_{S2}	I_{S1}	I_{S2}
I	$t_0 - t_1$, $t_3 - t_4$	S_1-ON S_2-ON	↑	↑	↑	↑	0	0	$i_{Lin1} + i_{ph1}$	$i_{Lin2} + i_{ph2}$
II	$t_1 - t_2$	S_1-ON S_2-OFF	↑	↓	↑	↓	0	$\frac{V_o}{2}$	$i_{Lin1} + i_{ph1}$	0
III	$t_2 - t_3$	S_1-ON S_2-OFF	↑	↓	↑	DC	0	V_{Cint}	$i_{Lin1} + i_{ph1}$	0
IV	$t_4 - t_5$	S_1-OFF S_2-ON	↓	↑	↓	↑	$\frac{V_o}{2}$	0	0	$i_{Lin2} + i_{ph2} + i_{in1}$
V	$t_1 - t_2$	S_1-OFF S_2-ON	↓	↑	↓	DC	V_{Cint}	0	0	$i_{Lin2} + i_{ph2}$

* ↑ – Charging , ↓ – Discharging , DC – Discontinuous Conduction

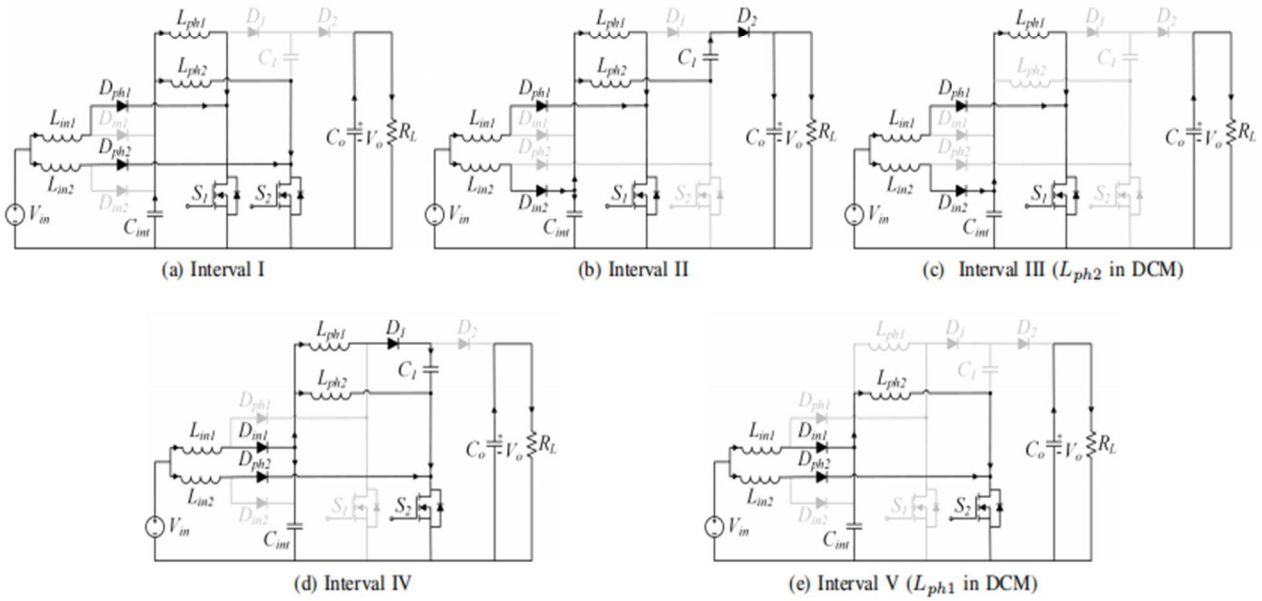


Fig. 4. Current path and conducting devices at various intervals during one complete switching cycle operation of converter in DCM-EDR mode.

IV. CONVERTER DESIGN

A. *Inductor Selection*

The inductance value for the input inductors (Lin, i) is dependent on the average current flowing through each of them as well as the peak-to-peak current ripple. The average current Through an input inductor, a portion of the network's input current can the converter. The specified current ripple across the input by (4). It must be avoided that the inductor enters. DCM is not meeting across the entire operational range. The criteria specified in (1). Other than this, the total current input ripple requirement is the major criteria for the design of input inductors and is given by (5).

$$\Delta I_{Lin} = \frac{V_{in}\, D}{f_{sw} L_{in}} \qquad (4)$$

$$\Delta I_{Lin} = \frac{V_{in}\,(2D - 1)}{f_{sw} L_{in}} \qquad (5)$$

ripple does not exist for the EDR stage inducers (Lph, i). any effect on the current flowing into the input for EDR stage inductors, they should be matched according to (2). To guarantee DCM operation, the inductors must be designed. of the converter across the entire load range. In the EDR stage inductors is given in (6). The ripple across the EDR stage inductors is given by (7).

$$I_{Lph} = \frac{V_{in}\,D}{2f_{sw}L_{ph}} \quad \frac{D(\propto -2) + 2D}{(\alpha - 2)(1 - D)} \qquad (6)$$

$$\Delta I_{Lph} = \frac{V_{in}\,D}{(1 - D)f_{sw}L_{ph}} \qquad (7)$$

B. Device Voltage and Current Stress

The steady-state voltage stress across different devices in EDR stage for DCM-EDR operation is the same as that of CCM operation of the converter [21]. The maximum volt age stress of main switches is equal to 1/2 times the output voltage (V out) enabling the use of low voltage devices. The voltage across intermediate capacitors C1 is also equal to half of the output voltage. For the EDR stage diodes, D1 has a voltage stress equal to the output voltage whereas D2 sees a voltage equal to half of the output voltage. The voltage stress across quadratic stage diodes and capacitor is slightly different in DCM-EDR operation compared to CCM operation. The quadratic stage devices still have very low voltage stress when compared to the output voltage. The intermediate capacitor Cint voltage is the same as that of Din and is given by (8). The phase diode voltage stress is also very low and is given by (9).

$$V_{Cint} = V_{Din\,1,2} = \frac{V_o}{\propto} \qquad (8)$$

$$V_{Dph\,1,2} = \frac{V_o(\propto -2)}{2 \propto} \qquad (9)$$

All the quadratic stage diodes have the same peak current stress equal to input inductor peak current. Both the switches have the same peak current stress equal to the sum of input inductor current and EDR stage inductor of the respective phase. The EDR stage diodes see a peak current stress equal to the EDR stage inductors. The switches and diodes are selected based on the peak voltage and current stress across

them. The different capacitors in the circuit as selected based on the voltage stress and RMS current flowing through them. The output capacitor selection has an additional criteria of voltage ripple similar to that of conventional boost converter.

TABLE II
HARDWARE PROTOTYPE SPECIFICATIONS

Parameters	Specifications
Rated Power(P_o)	300 W
Input voltage(V_{in})	30 V – 40 V
Output voltage(V_o)	400 V
Frequency(f_{sw})	135 kHz
Input inductor($L_{in1,2}$)	45 μH
EDR phase inductor($L_{ph1,2}$)	60 μH
Intermediate capacitor (C_{int})	6.8μF
EDR capacitor (C_1)	6.8μF
Output capacitor(C_o)	5μF

V. EXPERIMENTAL RESULTS

Through the simulation shown above, the proposed DCM-EDR operation of the two-phase Q-EDR boost converter is confirmed. The 300W type model is used to design both the input and EDR phase inductors for the DCM-EDR case. It operates at 30 V–40 V input, 400 V output, and switching frequency of 135 kHz. The converter's CCM operation is also experimentally tested to show that DCM-EDR operation reduces inductor size and value.

Simulation depicts the various inductors utilized for experimental verification. Because all of the inductors are externally connected, testing the converter for DCM-EDR and CCM operation is simpler. Only the phase inductors are altered in order to take into account the experimental results for the two cases, and the input inductor is the same drops to 83 V, which is the same as VCint, which is close to 1/5 of the output voltage. Additionally, the use of low-voltage diodes is made possible by the relatively low voltage stress across the quadratic stage diodes. Trial aftereffects of the converter working at high voltage gain. The converter can accomplish a voltage gain higher than 12 at a moderate obligation near 0.52. The converter misfortune breakdown for both DCM-EDR and CCM activity for 40 V to 400 V at 300 W is shown. There is a critical decrease in exchanging misfortunes in the event of DCM-EDR contrasted with CCM. In order to emphasize the reduction in switching losses, the phase inductors in DCM-EDR and CCM are designed to have a loss that is comparable. It is shown how efficient the converter is when the output power changes. The converter can accomplish its productivity is higher than 95% in the DCM-EDR operation with change in the result power. The converter eff-ectiveness with changing information voltage is displayed in Fig. 8. For 40 V to 400 V operation in DCM-EDR, the converter efficiency at 300 W is 95.48 percent, while for CCM, it is 94.72%. The converter can accomplish higher effectiveness in DCM-EDR contrasted with CCM activity for the whole scope of converter activity.

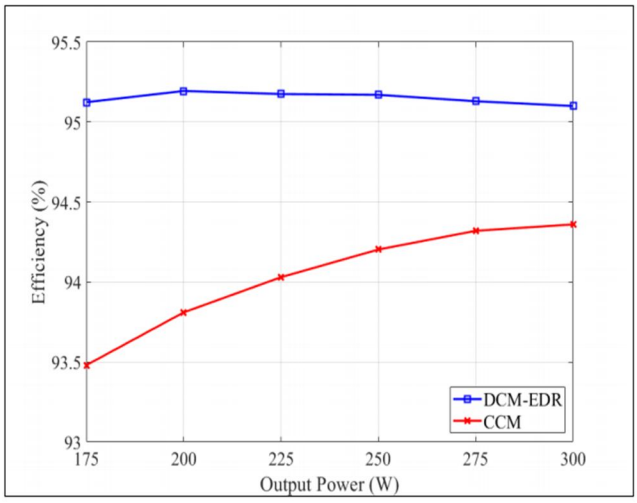


Fig. 5. Proposed DCM-EDR and CCM efficiency results for 36 V to 400 V.

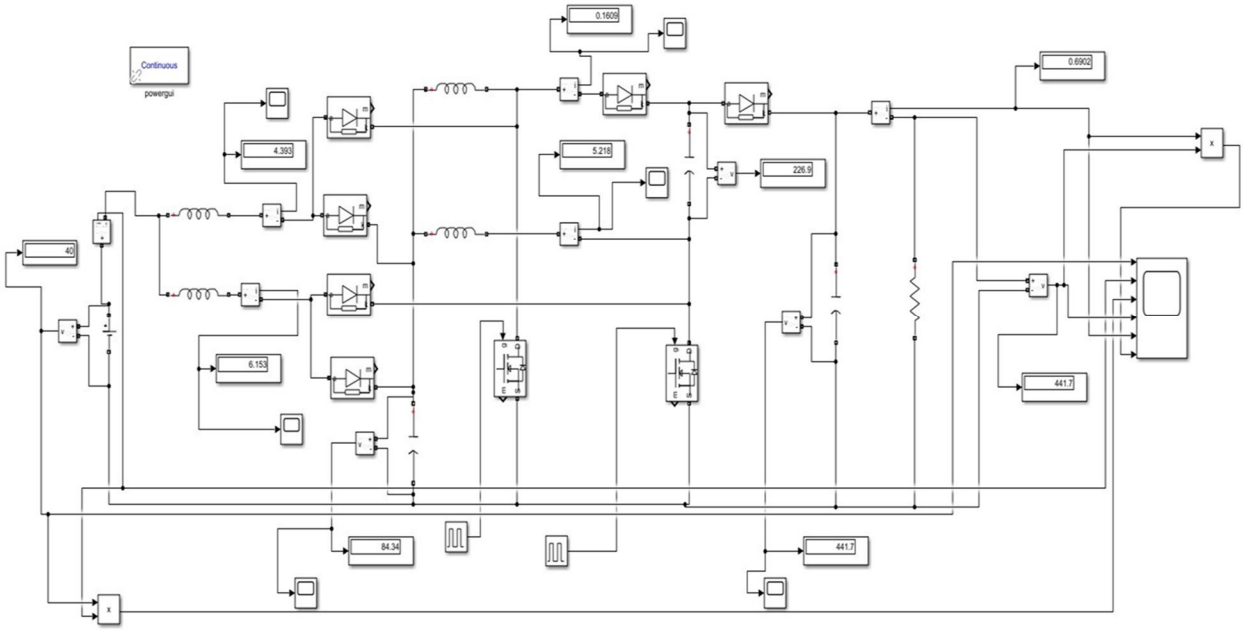


Fig 6 simulation diagram of proposed converter

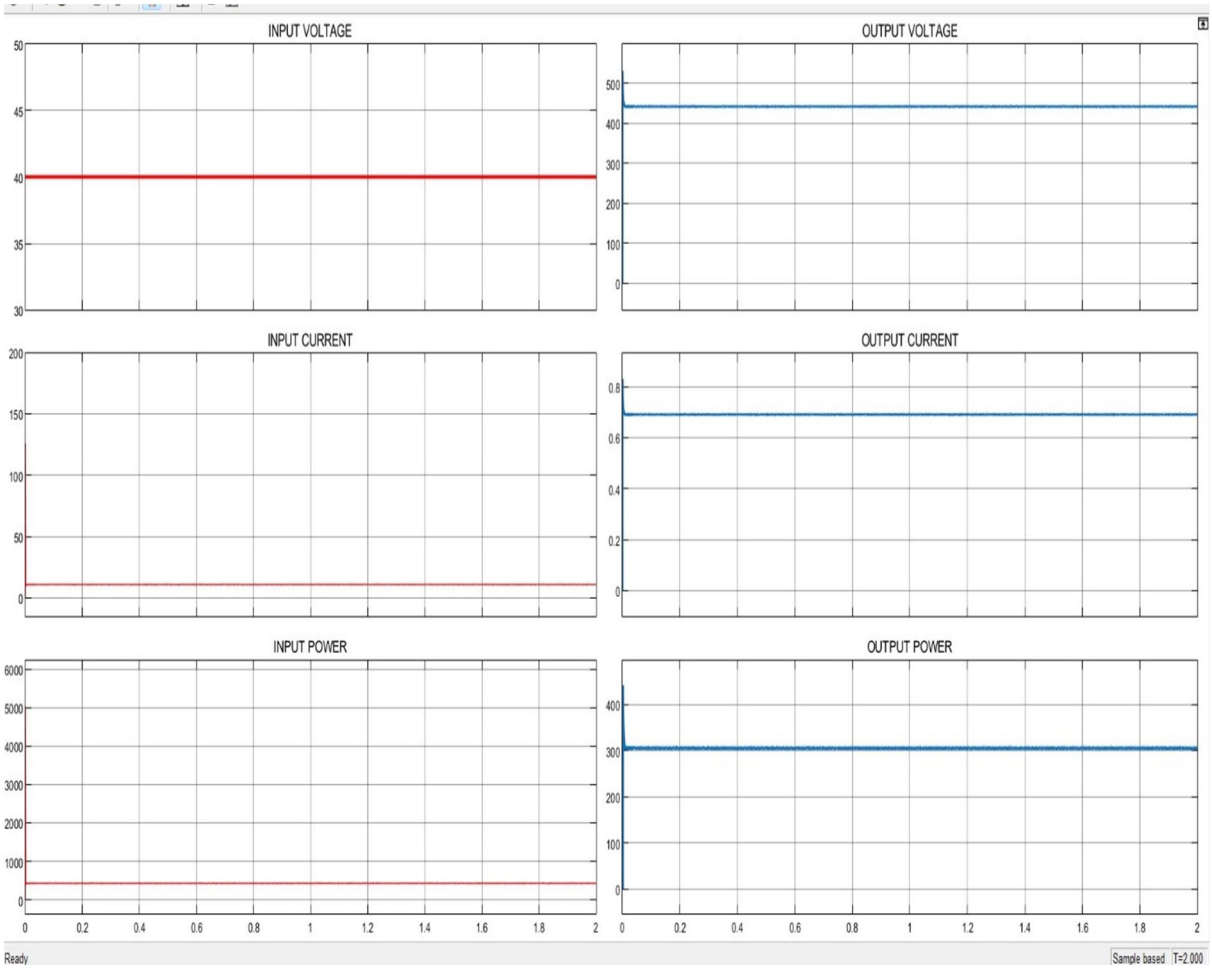


Fig 7. Simulation Results of Converter

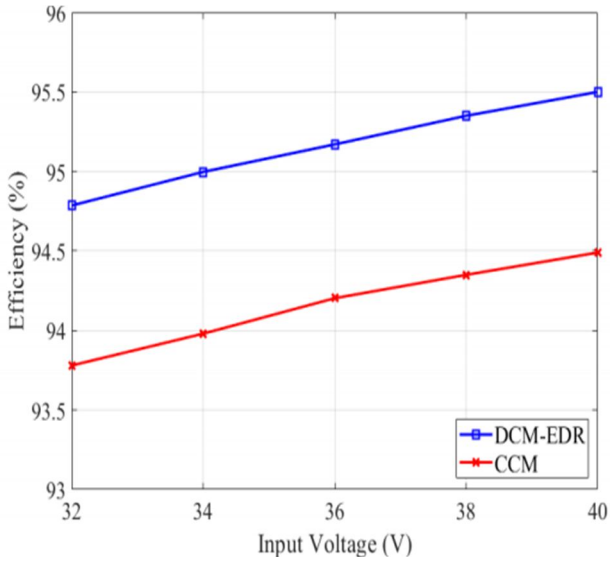


Fig.8 Proposed DCM-EDR and CCM efficiency results for varying input voltage at 400 V output, 250 W at 135 kHz.

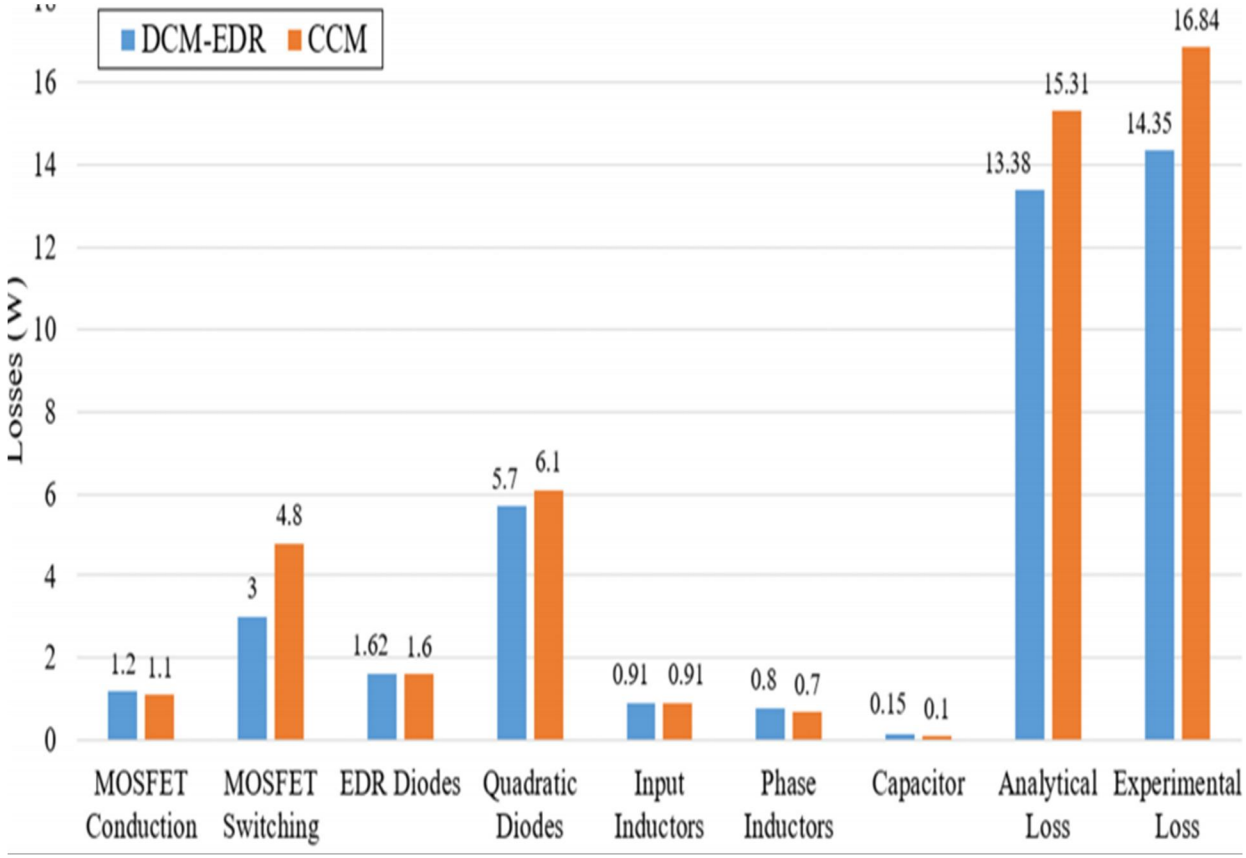


Fig. 9. Converter loss breakdown in both DCM-EDR and CCM operation for 40 V to 400 V, 300 W.

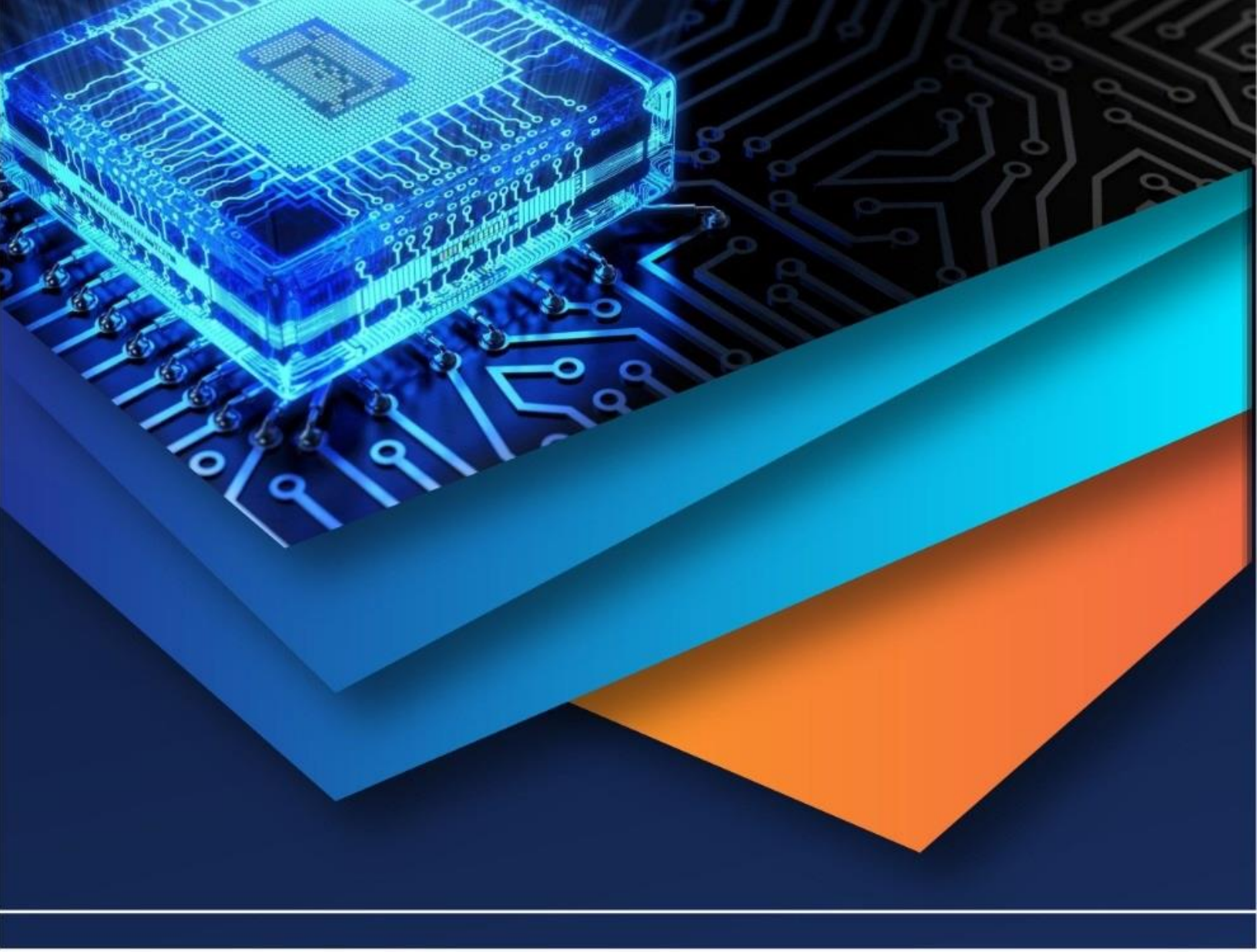
VI. CONCLUSION

The QEDR converter's various discontinuous operation modes are discussed, and the most advantageous hybrid mode DCM-EDR is chosen based on its numerous benefits. The converter's operation in DCM-EDR mode is thoroughly discussed. With the proposed DCM-EDR mode, the converter can achieve voltage gains greater than 12 at duty ratios close to 0.54. Additionally, switch turn on losses are reduced as the turn-on switch voltage drops to one fifth of the output voltage. This also makes it possible to operate at a higher switching frequency, which reduces the inductance value even further. When compared to CCM, the DCM-EDR case's EDR inductor size decreases by 45 percent, while the inductance itself decreases by 80 percent. A hardware prototype with a 300 W output and a voltage range of 30 V to 40 V and 400 V is used to test the proposed converter's operation. A misfortune breakdown with examination of the traditional CCM and DCM-EDR mode is introduced to feature the benefits of the proposed conspire. When all of the silicon switches are in use, the converter can operate at 300 W with a peak efficiency of 95.5 percent. Consequently, we use this hybrid CCM-DCM operation of a quadratic boost converter with an extended duty ratio to achieve high gain at low device stress.

REFERENCES

[1] J. Carrasco, L. Franquelo, J. Bialasiewicz, E. Galvan, R. PortilloGuisado, M. Prats, J. Leon, and N. Moreno-Alfonso, “Power-electronic systems for the grid integration of renewable energy sources: A survey,” IEEE Transactions on Industrial Electronics, vol. 53, no. 4, pp. 1002–1016, 2006.
[2] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula, and D. d. S. Oliveira Junior, “Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter,” IET Power Electronics, vol. 8, no. 10, pp. 2044–2057, 2015.
[3] W. Li and X. He, “Review of non-isolated high-step-up dc/dc converters in photovoltaic grid-connected applications,” IEEE Transactions on Industrial Electronics, vol. 58, no. 4, pp. 1239–1250, 2011.
[4] IQ 7 Micro and IQ 7+ Micro, Enphase Energy, Aug. 2020, rev1.0.
[5] QS1 Microinverter, APsystems, Aug. 2021, rev3.1.
[6] M. D. Seeman and S. R. Sanders, “Analysis and optimization of switched-capacitor dc–dc converters,” IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 841–851, 2008.

[7] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched capacitor/switched-inductor structures for getting transformerless hybrid dc–dc pwm converters," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, no. 2, pp. 687–696, 2008.
[8] O. Abdel-Rahim, M. Orabi, E. Abdelkarim, M. Ahmed, and M. Z. Youssef, "Switched inductor boost converter for pv applications," in 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2012, pp. 2100–2106.
[9] L. Schmitz, D. C. Martins, and R. F. Coelho, "Comprehensive conception of high step-up dc–dc converters with coupled inductor and voltage multipliers techniques," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 6, pp. 2140–2151, 2020.
[10] D.-H. Kim, G.-Y. Choe, and B.-K. Lee, "Dcm analysis and inductance design method of interleaved boost converters," IEEE Transactions on Power Electronics, vol. 28, no. 10, pp. 4700–4711, 2013.
[11] O. Lopez-Santos, L. Martinez-Salamero, G. Garcia, H. Valderrama Blavi, and D. A. Zambrano-Prada, "Steady-state analysis of inductor conduction modes in the quadratic boost converter,"IEEE Transactions on Power Electronics, vol. 32, no. 3, pp. 2253–2264, 2017.
[12] J. Roy, A. Gupta, and R. Ayyanar, "Discontinuous conduction mode analysis of high gain extended-duty-ratio boost converter," IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 372–387, 2021.
[13] D. Maksimovic and S. Cuk, "Switching converters with wide dc conversion range," IEEE Transactions on Power Electronics, vol. 6, no. 1, pp. 151–157, 1991.
[14] N. Korada and R. Ayyanar, "New crm topology for zero voltage switching in quadratic high gain boost converter," in 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 4794–4801.
[15] M. A. B. Kumar and V. Krishnasamy, "Quadratic boost converter with less input current ripple and rear end capacitor voltage stress for renewable energy applications," IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1–1, 2021.
[16] S. Hasanpour, Y. P. Siwakoti, A. Mostaan, and F. Blaabjerg, "New semiquadratic high step-up dc/dc converter for renewable energy applications," IEEE Transactions on Power Electronics, vol. 36, no. 1, pp.433–446, 2021.
[17] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Silva, "High step-up dc–dc converter for fuel cell vehicles based on merged quadratic boostCuk," IEEE Transactions on Vehicular Technology, vol. 68, no. 8, pp. 7521– 7530, 2019.
[18] J. Leyva-Ramos, R. Mota-Varona, M. G. Ortiz-Lopez, L. H. DiazSaldierna, and D. Langarica-Cordoba, "Control strategy of a quadratic boost converter with voltage multiplier cell for high-voltage gain," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1761–1770, 2017.
[19] J. Roy and R. Ayyanar, "Gan based high gain non-isolated dc-dc stage of microinverter with extended-duty-ratio boost," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), 2016, pp. 1–8.
[20] J. Roy and R. Ayyanar, "Sensor-less current sharing over wide operating range for extended-duty-ratio boost converter," IEEE Transactions on Power Electronics, vol. 32, no. 11, pp. 8763–8777, 2017.
[21] A. Gupta, N. Korada, and R. Ayyanar, "Quadratic extended-duty-ratio boost converter for ultra-high gain application with low device stress," in 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 2021, pp. 1796–1802.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY