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RTL Design of CISC CPU IP Core

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Abstract: ***Recent developments on programmable logic technology had promoted the microprocessor design task from big companies targeting the mass market to the everyday designer as intellectual property (IP) cores toward the system on-a-chip (SOC) approach. This paper shows the VHDL IP 8-bit CISC microprocessor core development which is intended as an open core for teaching applications in the digital systems laboratory. The core is fully open and therefore, the user can have access to all internal signals as well as the opportunity to make changes to the structure itself which is very useful when lecturing microprocessor design. The main advantages of the present core, compared with commercially available equivalent cores, are that it is not vendor sensitive allowing its implementation in almost any FPGA family and being an open core, it can be fully monitored and modified to fit specific design constrains. Several tests were performed to the microprocessor core, including an embedded microcontroller with RAM, ROM and I/O capabilities. The present development includes a meta-assembler and linker to embed user programs in a ROM, which is automatically generated as a VHDL description.***
Keywords: CPU; cISC; IP Core; IC

I. INTRODUCTION

CISC stands for Complex Instruction Set Computer. CISC processor is a classification of microprocessor-based of CPU design that operates on large and complex instruction sets so as to execute various tasks using the least possible codes. It is based on more than one instruction per cycle execution approach. CISC was introduced in 1970 and it handles instruction execution without making use of multiple codes. It is based on the complex nature of instruction set architecture.

The major goal behind the design of CISC is to have such an instruction set that works well with the tasks and data structures of Higher-Level Languages. This architecture supports a variety of addressing modes and therefore, the instruction length is of variable nature. This signifies that in this case, the whole emphasis is given to the hardware of the system. CISC processors are maturely designed to provide direct hardware support to the developer

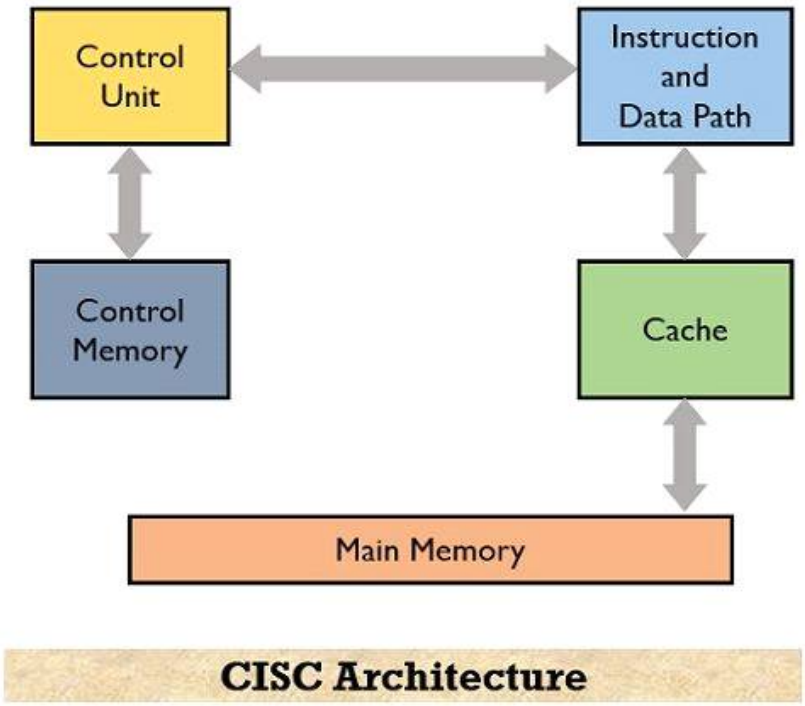


Figure 1. The main modules and interconnects in the CISC CPU IP Core.

ARCHITECTURAL OVERVIEW

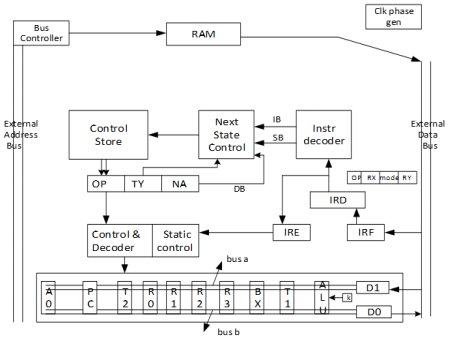


Figure 2. CPU architectural overview

Figure 2 shows the CPU architectural overview.

CISC Processor designed to execute the Following Instructions: - 1. ADD 2. AND 3. OR

These instructions should be for the addressing modes Register-to-Register, Register-to-Memory (Indirect), Register-to-Memory (Indirect with Base + Displacement format) and LBI (Load Base Register with Immediate Data (Magnitude format)).

The processor contains the following elements - Address Out Buffer (AO), 2 Temp Registers T1 and T2, Program Counter (PC), Four general purpose registers (programmer's registers) R0 to R3 and Base Register (B), ALU with constant generator, output routed to T1 and one of the inputs permanently connected to Internal Bus (a), Data out buffer (DO) with one of the inputs permanently connected to internal bus (b), Data input register DI.

AO is a Tri- state buffer that receives from and sends addresses to External Address Bus (EAB). DO is also a Tri- state buffer which sends data out to External Data Bus (EDB). DI is a register which receives data from External Data Bus (EDB) and writes the data to internal bus (b).

ALU is a combinational logic. ALU B input select is also a combinational logic Instructions are 1-byte long except when the second operand is Register Indirect with displacement. In which case the second Instruction byte contains the displacement. Memory is byte addressable. Displacement value has a signed representation but is read as a magnitude only. All memory addresses also have signed representation but are read as only positive quantities.

Data is represented in 2's complement form and manipulated using 2's complement arithmetic. In the Execution Unit, all the Reg to Bus transfers are to be done on the negedge of clock. Bus to register transfers, on the other hand, will be done posedge of the clock.

II. THE MAIN MODULES of CPU

A. Design top Architecture

Figure 3 below shows a somewhat simplified datapath architecture. This datapath is sufficient to execute most instructions so it will be used to introduce the overall CPU IP Core architecture.

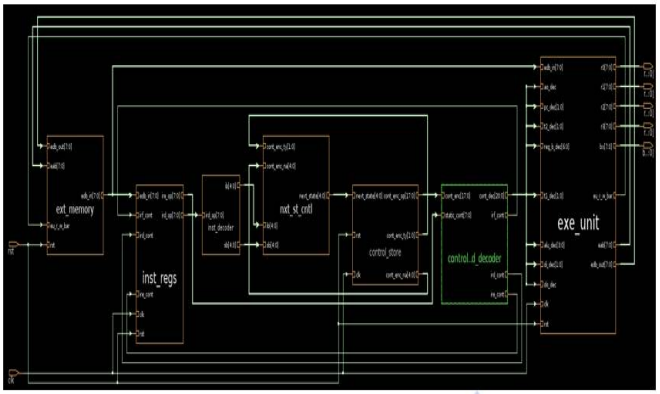


Figure 3. Design Top level Architecture

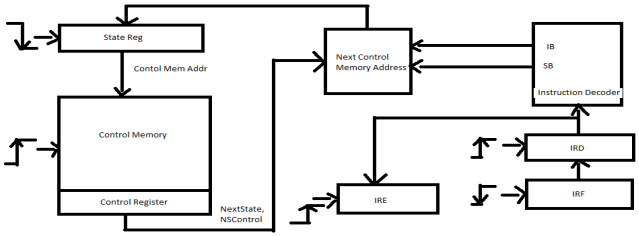


Figure 4. The Control Path timing

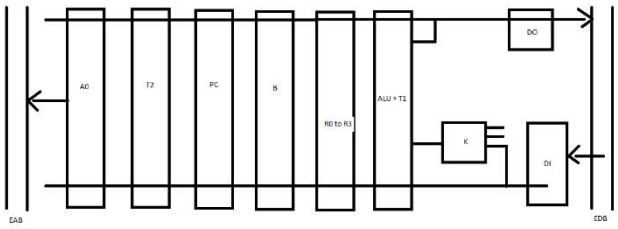


Figure 5. The Execution Unit timing

We use Verilog HDL language which describes the ALU logic function, with ModelSim Simulation software. When the instruction fetched from memory, It is decoded by control unit. This 8-bit decoded information shows the Addressing mode, register types, opcode. This same information is used by static control unit. The IRD information is used by instruction Decoder, next state control. All the information is stored in a encoded form in control store. Control n decoder use this encoded information give this to alu for doing different mode of operation. The result is than stored in memory by addressing bus.

Figure 6. Verification Simulation result

III. SPYGLASS LINT

Early Design Analysis for Logic Designers may detect design bugs but often at late Inefficiencies during RTL design usually surface as critical design bugs during the late stages of design implementation. If detected, these bugs will often lead to iterations, and if left undetected, they will lead to silicon re-spins. The Spy Glass® product family is the industry standard for early design analysis with the most in-depth analysis at the RTL design phase. Spy Glass provides an integrated solution for analysis, debug and fixing with a comprehensive set of capabilities for structural and electrical issues all tied to the RTL description of design.

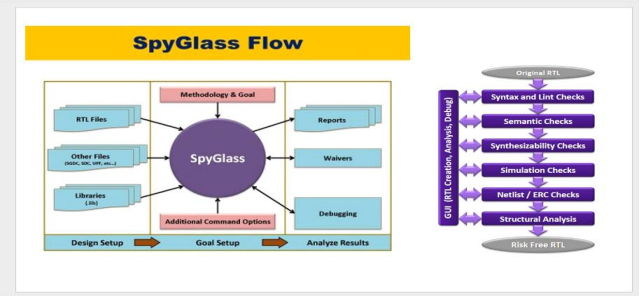


Figure 7. Spyglass Lint flow

With soaring complexity and size of chips, achieving predictable design closure has become a challenge. A multitude of coding style, structural and electrical design issues can manifest themselves as design bugs and result in design iterations, or worst still—silicon re-spins. Other tools stages of design implementation, after a significant investment in time and effort has already been made. As design teams become geographically dispersed, consistency and correctness of design intent becomes a key challenge for chip integration teams. Emphasis on design reuse and IP integration requires that design elements be integrated and meet guidelines for correctness and consistency.

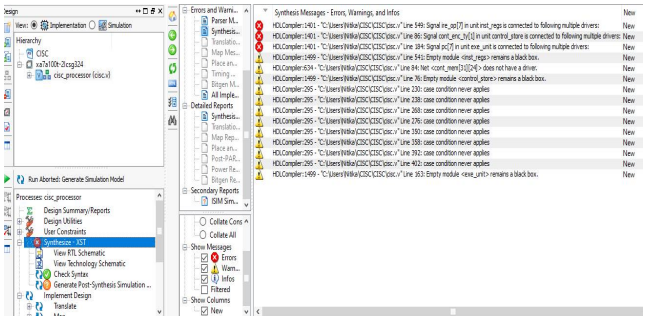


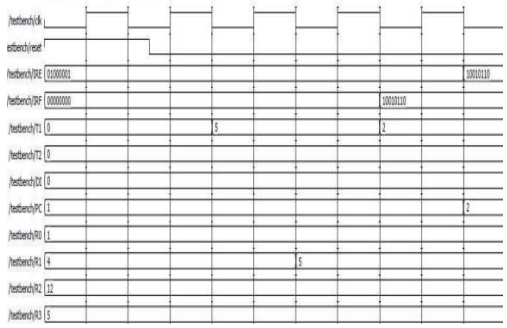
Figure 8. Lint output

IV. SIMULATION

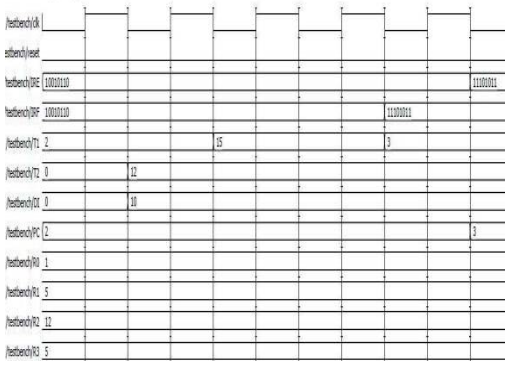
After we design the modules of CPU, we should do the simulation to test the correctness of CPU.
Simulation Results: Instructions simulated:

ADD R0,R1 (R-R)
OR R1,(R2) (R-I)
AND R2,[R3 +5] (B+DI)
ADD R1,R3,#6 (IMM)

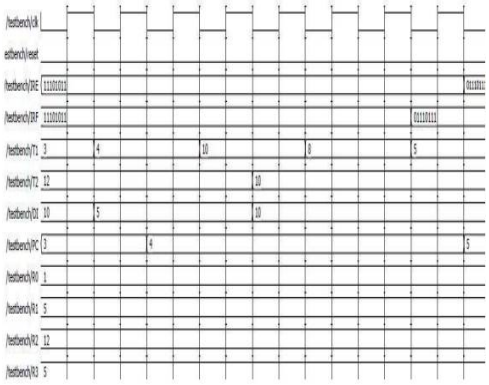
ADD R0,R1 - 01000001



OR R1,(R2) -10010110



AND R2,[R3+5] -11101011 DI-00000101



ADD R1,R3,#6 01110111 IMM-00000110

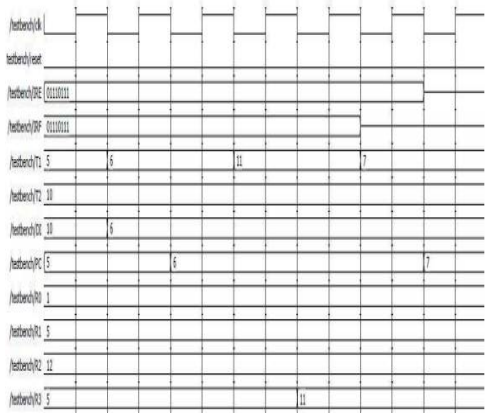


Figure 9.Instrutction Simulation output

V. COVERAGE (CODE & FUNCTIONAL)

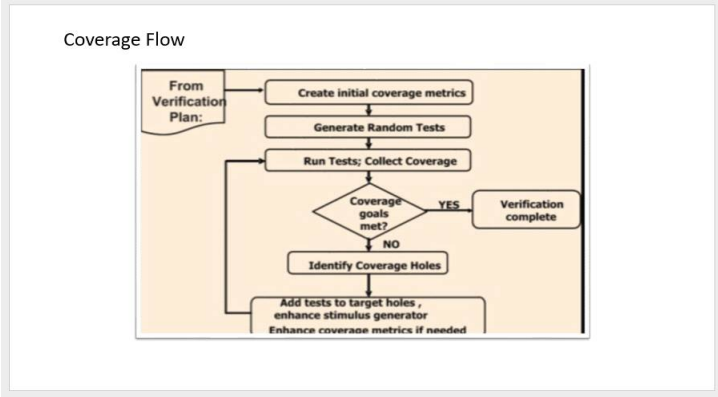


Figure 10 .Coverage output

1) *Code Coverage:* Is a software testing metric that determines the number of lines of code that is successfully validated under a test procedure, which in turn, helps in analyzing how comprehensively a software is verified.
2) *Function Coverage:* This ensures that all necessary functions are tested. It also includes testing functions with different input parameters to test the logic in the functions. Statement Coverage: In this, the code is created in a way that every executable statement in the source code is executed at least once.

VI. SYNTHESIS

We synthesize the CPU with the tool of Synplify Pro 8.0. We choose Altera Cyclone EP2C35 for synthesis.

Area:

Instance	Cells	Cell Area	Net Area	Wireload
EXEC_UNIT	1032	10407	0	enG5K (S)

Gates:

Type	Instances	Area	Area %
sequential	393	6283.000	60.4
inverter	17	51.000	0.5
tristate	104	880.000	8.5
logic	518	3193.000	30.7
total	1032	10407.000	100.0

Power:

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
EXEC_UNIT	1032	26.825	77155.265	77182.090

VII. CONCLUSION

In this paper, how to design a simple CPU is presented. Harvard bus and two level pipe-line structures are used. As a result, most of the instructions only need one machine cycle to be executed. There are only 35 reduced instructions in its instruction set, which are easy to be learned and used. The simulation results show the CPU has a good performance.

VIII. ACKNOWLEDGMENT

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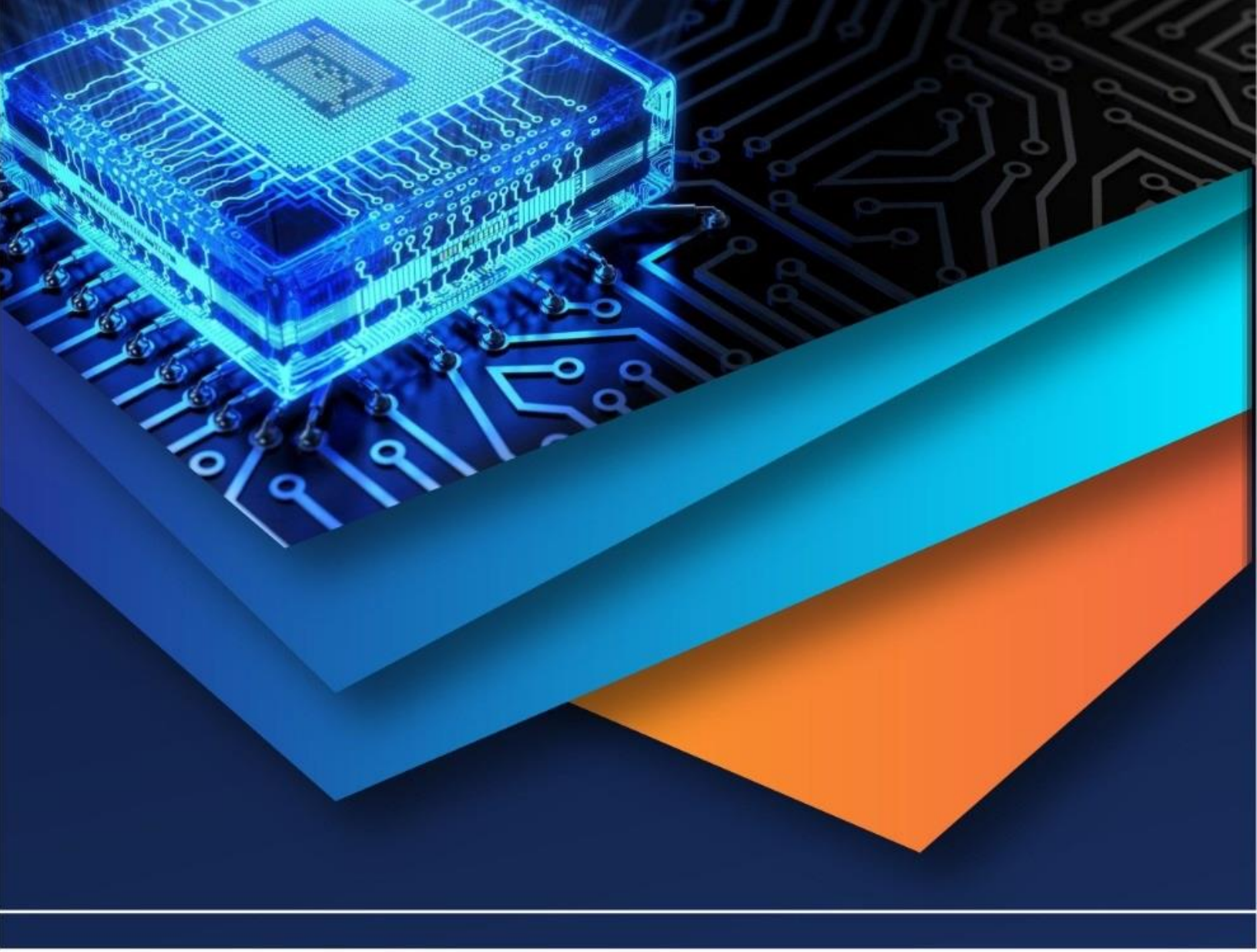
REFERENCES

[1] PIC16C63A/65B/73B/74B DataSheet, Microchip Technology Inc,2000.
[2] Piguet C. Low power design of 8-b embedded cool-RISC microcontroller cores. IEEE Journal of Solid-State Circuits, 1997, 32(7): 1067~1077
[3] OTP 8-Bit CMOS MCU with EEPROM Data Memory, USA:
Microchip Technology Inc, 1998
[4] PIC micro TM Mid-Range MCU Family Reference Manual. Microchip Technology Inc.1997. 1~688.
[5] Mano, M. M., Computer System Archetecture, Prentice Hall, Tsinghua University press,1997.
[6] Ma G K, Taylor F J. Multiplier policies for digital signal processing.
IEEE ASSP Magazine, 1990, 7(1): 6~20
[7] Wayne Wolf, Modern VLSI Design, USA: Printice Hall, 2001:298~299
[8]



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