iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 11 **Issue:** IX **Month of publication:** September 2023

DOI: https://doi.org/10.22214/ijraset.2023.55697

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 11 Issue IX Sep 2023- Available at www.ijraset.com

Studying the Performance of Underlap GAA-FET

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Abstract: ***This paper investigates the performance of underlap Gate-All-Around Field Effect Transistor (GAA FET) of 22nm gate length and evaluates the short channel performance of the device. Underlap GAA FET structure can be utilized to increase the drive current of the nanowire devices. In this work, underlap rectangular GAA FET is designed by extension of underlap regions on source/drain of GAA FET to increase the performance. This underlap device is increasing the capacitances by adding the fringing capacitances to parasitic capacitances which increases the fringing field from gate electrode to underlap regions. In this also investigating the electrical parameters on various performance metrics like threshold voltage (V_{th}), ON current (I_{ON}), OFF current or subthreshold leakage current (I_{OFF}), ON-OFF current ratio (I_{ON}/I_{OFF}) and short channel effects such as Subthreshold slope (SS) and DIBL (Drain Induced Barrier Lowering) of underlap GAA FET are systematically evaluated and analysed. In the present study, GAA FET and underlap GAA FET device performances are investigated through ATLAS device simulator from Silvaco.***

Keywords: DIBL, GAA FET, ON-current, Underlap, Subthreshold slope.

I. INTRODUCTION

To achieve high operational speed, low cost, and better performance of conventional transistors, the dimensions need to be downscaled to the sub-nanoscale region. The concept on device scaling law [1, 2] and advancements of CMOS technology, physical scaling of MOSFETs has been continuously shrinking in accordance with the standard of ITRS [3]. The issue of the nano-scale regime has led to continuous downscaling of MOSFET devices. Due to aggressive downscaling, reaches its limit facing short-channel effects (SCEs) occur in case of conventional single gate MOSFETs [4], which can observe because of the dominance of the junction of a minimal of channel in the time of escaping gate control [5]. The reduction of metal-oxide-semiconductor field effect transistor (MOSFET) dimensions will degrade the gate control over the channel due to close proximity between source and drain. This leads to increase various short channel effects (SCEs) such as hot carrier effect, threshold voltage roll-off, and substrate bias effect [1, 2]. Many new devices have been introduced beyond Moore's era [3–5] to suppress the SCEs and enable further scaling down of the device. Similarly, a number of multi-gate silicon on insulator (SOI) technologies have also been proposed to replace the conventional MOSFET [6, 7]. FINFET is the industry-standard complementary metal oxide semiconductor technology for sub-22 nm node very-large-scale integrated circuits. Due to multiple gates controlling the thin, fully depleted channel, FinFET shows improved short-channel performance compared to the single-gate planar MOSFET. To maintain acceptable short channel performance in FinFET, the channel thickness should be around a third of the gate length. Improved short channel performance results in lower threshold voltage at the same OFF-current and hence higher gate overdrive voltage resulting in higher ON-current. Since FinFET is a quasi-planar device, ON-current per device footprint can be increased by making the fins taller and reducing the device footprint. Fin height was increased from 34 nm at 22-nm node to 42 nm at 14-nm node. Device footprint can be reduced by decreasing the fin pitch. The fin pitch was 60 nm at 22-nm node and was reduced to 42 nm at 14-nm node. According to the International Technology Roadmap for Semiconductors 2.0, the fin pitch, fin width, and gate length are expected to scale. The ratio of fin width to gate length is 1/3 till the "11/10" nm node. Fin width scaling may be limited to 6 nm due to processing challenges. At the "8/7" nm node, the fin width to gate length ratio increases to 0.43, which can degrade the short-channel performance of the device. With careful source–drain underlap doping design, the short channel performance of the device can be improved due to longer effective gate length [7]. The fin thickness requirement can be relaxed to be about one-half of the gate length for acceptable short-channel performance. While the introduction of underlaps improves the short-channel performance, it can increase the total resistance of the device due to the addition of the resistance of the lightly doped underlap regions. The overall performance of an underlap device is an optimization between the underlap region resistance and the decrease in the threshold voltage due to improved short-channel performance and the corresponding increase in the gate overdrive voltage. However, the gate all around (GAA) FET is one of the novel devices which further enables scaling without hindering the device performance.

Because of the low characteristic length and higher drive current, GAA MOSFETs can achieve higher packing density as compared to double gate (DG) MOSFETs [8–10]. Also GAA FET has excellent electrostatic control of the channel, robustness against SCEs, better scaling options, no floating body effect, larger equivalent number of gates, and ideal subthreshold swing as compared to other multiple gate MOSFETs. Hence, the GAA FET is a promising solution for nanoscale technology complementary metal–oxide–semiconductor (CMOS) devices [11–15]. Recently, MOS devices with sub-50 nm channel length demonstrate more than 100 GHz of cut-off frequency [16–18]. Important device parameters such as threshold voltage (V_{th}), ON-OFF ratio (I_{ON}/I_{OFF}), SS and DIBL are very much sensitive to the device geometry such as channel length, channel thickness, and gate work function. In this paper, analysing the performance of underlap GAAFET and compare the electrical parameters of GAA FET with underlap GAA FET. In section 2 the device structure description that includes all the dimensions, materials and doping concentrations of both devices and in this section also analyses the physics of the device using device numerical simulations and models activated for simulation. Section 3 comprises all results and discussion. Finally, the concluding remarks are presented in section 4

II. DEVICE STRUCTURE

Fig. 1. shows the 3D schematic view of a) GAA FET and b) underlap GAA FET. Both the GAA FET devices are modelled and characterized by using Silvaco TCAD tools. The device has been simulated using 3D device simulator Silvaco TCAD. Device A is designed by wrapping the SiO_2 layer on the channel and the oxide layer is surrounded by the gate metal, and Device B is developed by taking the Device A, extend the equal channel length on both sides of source/drain. Device B is a underlap GAA FET designed by extension of the channel region in source and drain side known as underlap region and the source & drain bulk makes bigger. Symmetrical distances are being adopted from source to gate and gate to drain (S-G and G-D) by fixing the gate length identical is cited as underlap. Here, the observation has been done for the underlap length of 2.5 nm. SiO_2 layer is chosen as dielectric material in between the gate metal and substrate.

L_g is the channel length or gate length between source and drain and W_{th} is the channel width. L_{us} and L_{ud} is the extension length of the source and drain. It decides the significant underlap capacitance and resistance of source or drain. T_{ox} is gate oxide thickness. The underlap GAA FET structure can be characterized in terms of gate length (L_g) and underlap length (L_u). The silicon material with N-type source and drain doping concentration is 1×10^{18} cm^{-3} whereas P-type doping concentration of 1×10^{15} cm^{-3}, and oxide thickness is 1 nm. The corresponding k value for gate dielectric material are 3.9. Table I shows the parameters used for the present work of simulation. The electrical parameters of the devices are simulated by using Silvaco Atlas simulator. In the simulation of the devices, the Shockley–Read–Hall (SRH) recombination using fixed lifetimes model, the band gap narrowing model, and Auger recombination models are also included for better modelling of the 22 nm gate length GAA FETs.

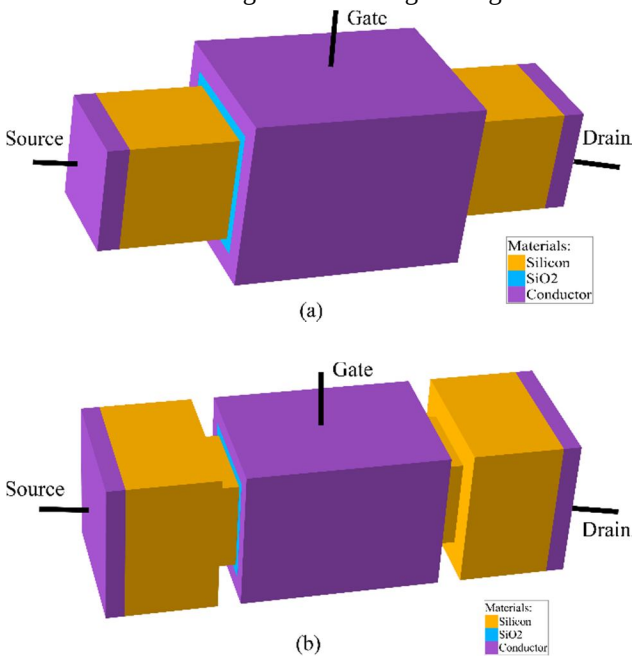


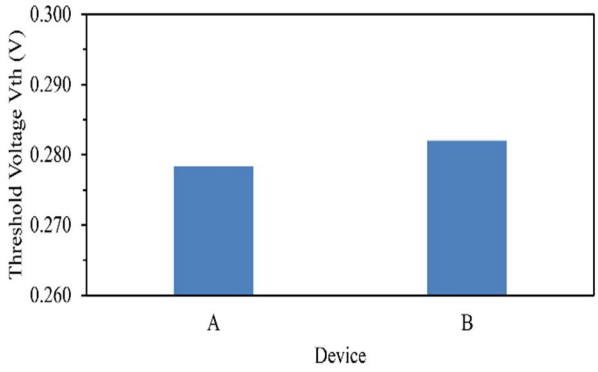
Fig. 1. a) GAA FET, b) Underlap GAA FET

Table I: Device parameters

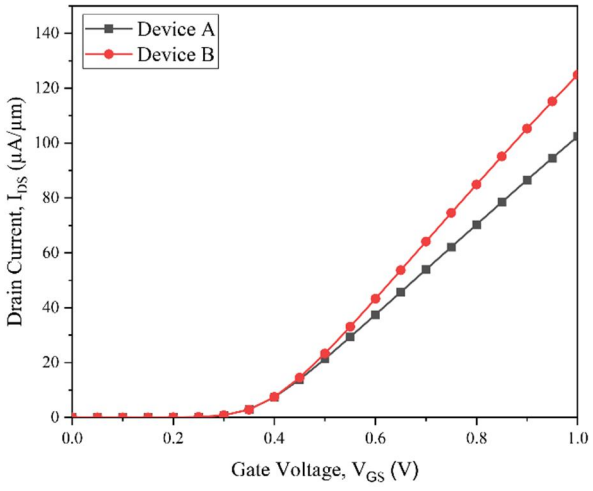
Parameter	values
Gate Length, L_g	22 nm
Length of Drain/Source, $L_{s/d}$	10 nm
Underlap Length, $L_{us/ud}$	2.5 nm
Thickness of oxide, t_{ox}	1 nm
Doping concentration of Drain/Source	1×10^{18} cm^{-3}
Doping concentration of Channel	1×10^{15} cm^{-3}
Permittivity of SiO_2	3.9

III. RESULT

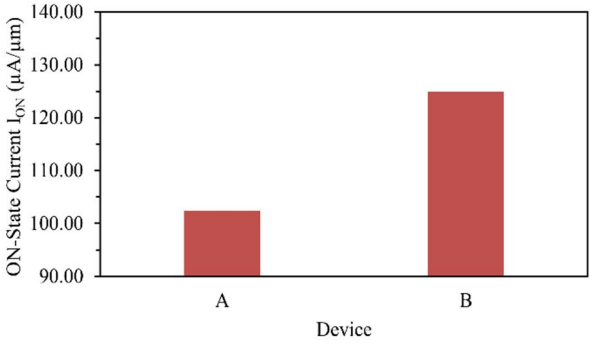
Charge sharing is the main source for V_{th} roll-off. The Threshold voltage variations (V_{th}) for Device A and Device B are shown in Fig. 2(a). For Device B acquired higher threshold voltage then Device A. From the graph, it is observed that the threshold voltage of two devices is determined to be 0.278 V and 0.282 V, respectively, at a drain voltage of 0.1 V. The threshold voltage begins to reduce as the channel length is shortening in CMOS devices because depletion region charge is supported by source and drain. An increase in drain current is observed in the underlap device with an increase in drain voltage as the gate voltage is varied from 0 V to 1 V. For a drain voltage of 0.1 V, the maximum drain current for the device A is 19 µA/µm, while it is 21 µA/µm for the device B. A similar trend is also observed for increased drain voltages where the drain current for device B is 124.88 µA/µm when compared to 102.42 µA/µm for the device A at drain voltage of 1 V that are shown in Fig. 2(b). Hence, the rectangular GAA FET with underlap device holds an upper hand in respect to performance and switching speed as shown in Fig. 2(c).



(a)



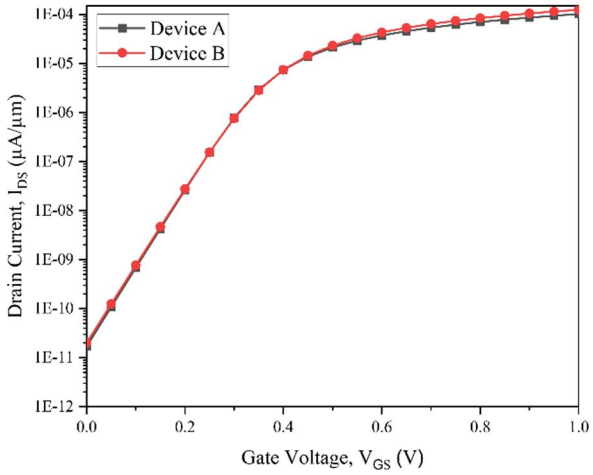
(b)



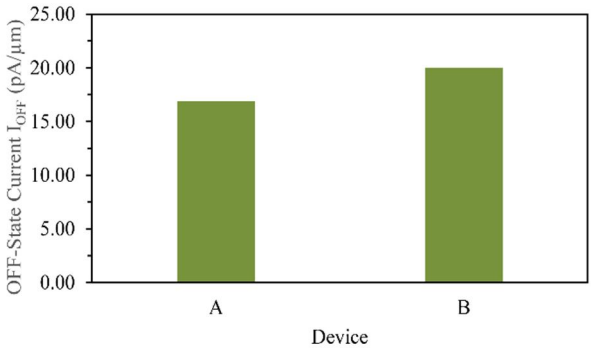
(c)

Fig. 2 (a) Threshold voltage, (b) Transfer characteristics in linear scale, (c) Comparison of ON state current

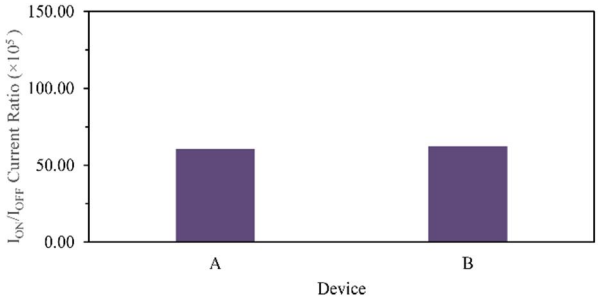
From Fig. 3, which shows the logarithmic plot of the $I_D - V_{GS}$ transfer characteristics and from this graph, leakage current, also known as OFF current (I_{OFF}), subthreshold swing (ss), and the drain induced barrier lowering (DIBL) can be determined. The leakage currents increase with increasing drain voltages while sweeping V_{GS} from 0 V to 1 V, the leakage currents are in pA/μm range also shown in Fig. 3(b), resulting in higher ON/OFF current ratio. At a drain voltage of 1 V, the GAA FET has a leakage current of 16.87 pA/μm, and the underlap GAA FET device has a leakage current of 20.02 pA/μm leading to an I_{ON}/I_{OFF} ratio of 60.70×10^5 and 62.39×10^5, respectively. It can be concluded that the I_{ON}/I_{OFF} ratio of the Device B is more than device A. Fig. 3(c) shows this comparison of I_{ON}/I_{OFF} current ratio for both devices. This trend of the ON/OFF current ratio is also observed for other drain voltages of 0.1 V and 1 V thereby proving that the underlap GAA FET structure has a higher switching speed and faster operation.



(a)



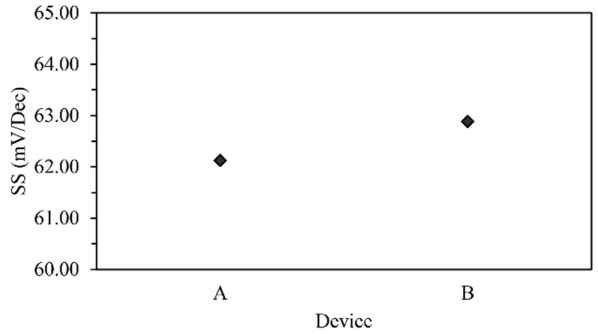
(b)



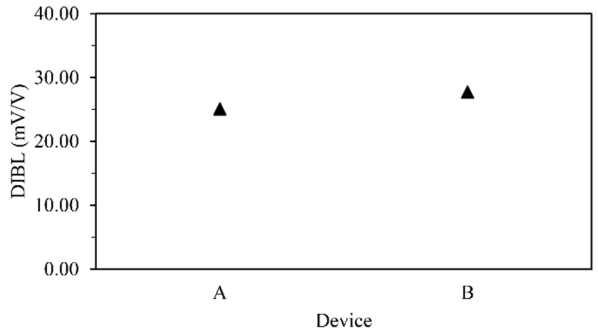
(c)

Fig. 3. (a) Transfer characteristics in log scale, (b) Comparison of OFF state current (I_{OFF}), (c) Comparison of I_{ON}/I_{OFF} ratio

The subthreshold swing is observed to be around 62.13 mV/decade for the device A and 62.89 mV/decade are found for the device B shown in Fig. 4(a). Increased SS for underlap device is observed due to increase in leakage current at underlap interfaces. Besides that, SiO_2 of low-k gate dielectric increases the leakage current between the gate metal and channel through a process of gate quantum tunnelling which result in high sub-threshold swing. A decade is ten times change in the drain current. The DIBL, measured from the logarithmic plot of the $I_D - V_{GS}$ graph, is a short channel effect that calculates the amount of change in threshold voltage as the drain voltage is subjected to a large change. The comparison of DIBL is shown in Fig. 4(b) and determined as 25.11 mV/V for device A device and 27.72 mV/V for the device B.



(a)



(b)

Fig. 4. Comparison of (a) subthreshold swing, (b) DIBL

Fig. 5. shows the output characteristics ($I_D - V_{DS}$) of the two devices, for different V_{GS} voltages of 0.5 V, and 0.8 V. The graph shows a early acquisition of saturation region and a sharp linear region of both the devices. Although the saturation current of the device A is ~ 72 µA/µm and the saturation current of the device B is ~ 84 µA/µm at V_{GS} = 0.8 V, that shows a positive slope depicting enhanced performance. Here the drain current of Device B increased by 18% as compared to Device A. The underlap regions are increasing the parasitic capacitances which increases the electric fields in source side, allows the large number of carriers from source to drain.

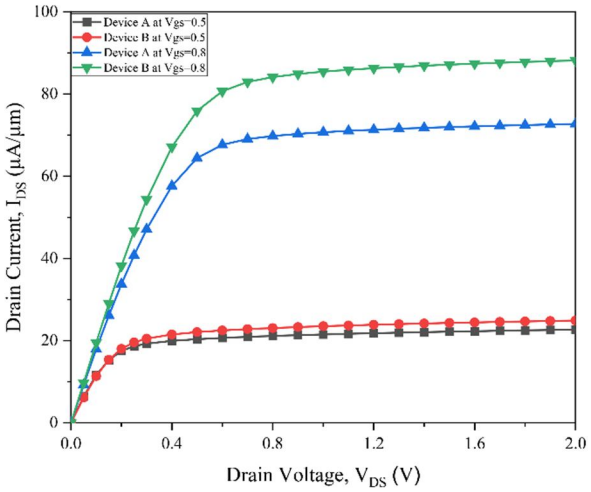


Fig. 5. Output characteristics

IV. CONCLUSION

The simulation of GAA FET and underlap GAA FET devices for a gate length of 22 nm with symmetrical underlap was performed by using SILVACO ATLAS simulation software. In this paper, the electrical characteristics of two devices have been studied and analyzed. The simulation results precisely optimized inconsideration of threshold voltage (Vth), ON current (I_{ON}), I_{ON}/I_{OFF} ratio, and slightly increased the OFF current (I_{OFF}), sub threshold swing (SS), DIBL of simulated device. Increased ON current are found in underlap GAA FET comparing with GAA FET which increases the device speed and also enhanced the device performance due to improved current ratio.

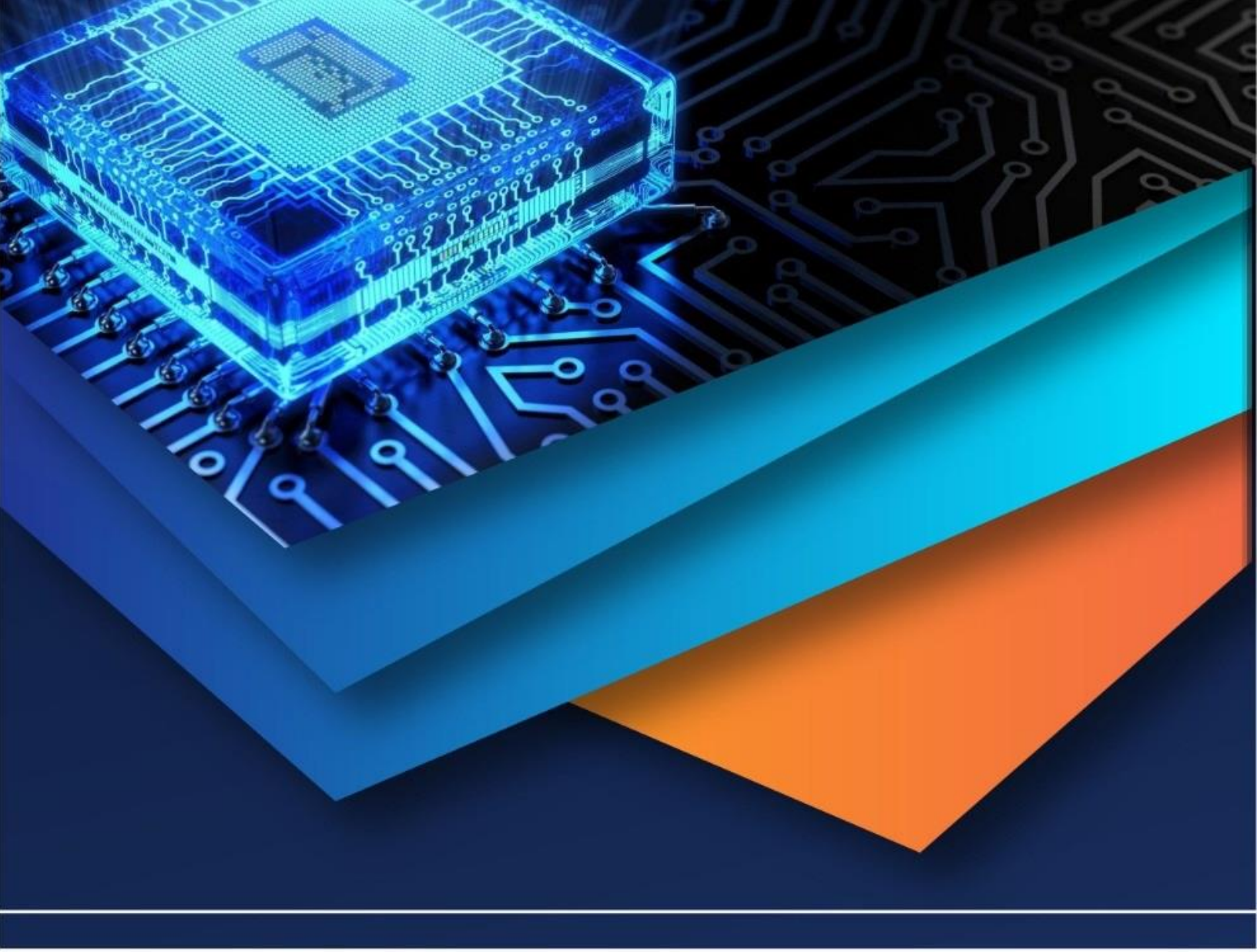
V. ACKNOWLEDGEMENT

The Authors are thankful to the HoD, Department of Electronics and Communication Engineering and also thanks to Chairman, Principal and management of Visakha Institute of Engineering and Technology, Visakhapatnam to carry out this research work

REFERENCES

[1] Huff, H. R., & Electrochemical Society. (2009). Into the nano era: Moore's law beyond planar silicon CMOS. Berlin: Springer.
[2] Moore’s Law:40thAnniversary: http://www.intel.com/cd/corporate/tec htrends/emea/eng/209729.
[3] (2013). International Technology Roadmap for Semiconductors. [Online]. Available: http://www.itrs.net/.
[4] M. R. Hasan, "Influence of device performance of Sub-10 nm GaN based DG-MOSFETs over conventional Si-based SGMOSFETs," 2017 4th International Conference on Advances in Electrical Engineering (ICAEE), Dhaka, Bangladesh, 2017, pp. 697- 702. doi: 10.1109/ICAEE.2017.8255445.
[5] D.K. Ferry, L.A. Akers, E.W. Greeneich, “Ultra Large-Scale Integrated Microelectronics,” Prentice-Hall, Englewood Cliffs, NJ, 1988.
[6] Y. Taur, et al., IEEE Electron Device Letters, Vol. 25, pp. 107-109, February 2004.
[7] J.-J. Kim and K. Roy, “Double Gate MOSFET Subthreshold Circuit forUltralow Power Applications,” IEEE Trans. Electron Devices, vol. 51, pp. 1468–1474, 2004.
[8] A. Amara and O. Rozeau, Planar Double-Gate Transistor, 2009.
[9] M. R. Hasan et al., "Metal Gate Work Function Engineering: Sub-Nano Regime Double Gate MOSFETs," 2019 International Conference on Electrical, Computer and Communication Engineering (ECCE), Cox's Bazar, Bangladesh, 2019, pp. 1-5, doi: 10.1109/ECACE.2019.8679134.
[10] M. Balaguer, B. Iñíguez, and J. B. Roldán, “An analytical compact model for Schottky-barrier double gate MOSFETs,” Solid-State Electron., vol. 64, no. 1, pp. 78–84, 2011.
[11] Kranti, T., M. Chung, and J.-P. Raskin, “Analysis of static and dynamic performance of short channel double gate SOI MOSFETs for improved cut-off frequency,” Jpn. J. Appl. Phys., vol. 44, no. 4B, 2005, pp. 2340- 2346.
[12] Md. Rabiul Islam, Md. Rokib Hasan, Md. Abdul Mannan et al., "Sub- nano Regime DG-MOSFETs", Journal of Semiconductor Devices and Circuits., vol. 5, no. 3, 2018.
[13] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, J. Fossum, IEDM Tech. Dig. (2000) 715.
[14] B. Monemar. In The Second International Conference on Nitride Semiconductors, Tokushima, Japan, pages 6–8, October 27-31, 1997.
[15] B. Ray and S. Mahapatra, IEEE Trans. Electron Devices, vol. 56 (2009) 260.
[16] Kranti, T., M. Chung, and J.-P. Raskin, “Analysis of static and dynamic performance of short channel double gate SOI MOSFETs for improved cut-off frequency,” Jpn. J. Appl. Phys., vol. 44, no. 4B, 2005, pp. 2340- 2346.
[17] Y. Awano, M. Kosugi, T. Mimura, M. Abe, “Performance of a quarter micrometer gate ballistic electron HEMT”, IEEE Electron. Dev. Lett. 8 (1987) 451–453.
[18] V. Trivedi, J.G. Fossum, and M.M. Chowdhury, IEEE Trans. Electron. Devices 56, 52 (2005).
[19] A. Dey, A. Chakravorty, N. DasGupta, and A. Das Gupta, IEEE Trans. Electron Devices, vol. 55 (2008) 3442.

[20] P. T. Vishal and G. F. Jerry, IEEE Electron. Devices, vol.26 (2005) 579.
[21] Md. Saud Al Faisal, Md. Rokib Hasan, Marwan Hossain and Mohammad Saiful Islam (2017). Projected Performance of Sub-10 nm GaN-based Double Gate MOSFETs. Circulation in Computer Science, 2, 2 (March 2017), 15-19. https://doi.org/10.22632/ccs-2017- 251-50.
[22] S. Cho; J. Hoon Lee; Shinichi O'uchi; Kazuhiko Endo; Meishoku Masahara; Byung-Gook Park "Design of SOI FinFET on 32 nm technology node for low standby power (LSTP) operation considering gate-induced drain leakage (GIDL)", International Semiconductor Device Research Symposium Year: 2009, Pages: 1 – 2.
[23] Md. Rokib Hasan, Md. Saud Al Faisal, Marwan Hossain and Mohammad Saiful Islam. "Effect of Underlap on Device Performance of GaN based DG-MOSFET".



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