



# IJRASET

International Journal For Research in  
Applied Science and Engineering Technology



---

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

---

**Volume: 11    Issue: V    Month of publication: May 2023**

**DOI: <https://doi.org/10.22214/ijraset.2023.52583>**

**[www.ijraset.com](http://www.ijraset.com)**

**Call:  08813907089**

**E-mail ID: [ijraset@gmail.com](mailto:ijraset@gmail.com)**



The Conventional 6T SRAM cell declines in various conditions such as read stability due to the conflict between Pull up or Pull down and the access transistors and Variability i.e. less reliable in Submicron technology due to the process parameters variations. To overwhelm these issues various cells have been designed which started with the 8T SRAM cell design as given in Fig 2.

The cell comprises a decoupled read path With two extra nmos transistors to eradicate the read disturb issue. But, it suffers from the leakage problem due to the added transistors relying on the information stored in the cell.

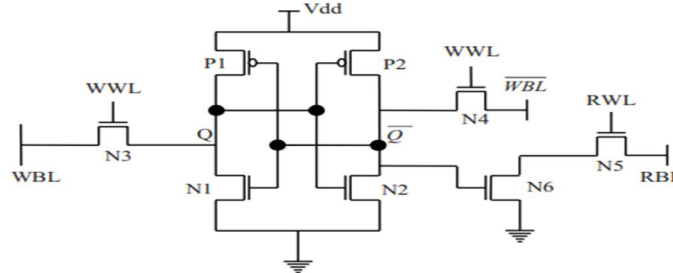


Figure 2: 8T SRAM cell

In order to solve the leakage problem many other cells have been designed. A recent work was proposed in as shown in Fig 3. (referred to as 10T-E1) which includes a pmos transistor at the read path reducing the leaking current passing through the M6 transistor. But the design at the same time also causes to the flow of leaking current from the node into the RBL which thereby leads to the reduction of sensing margin and is also data dependent.

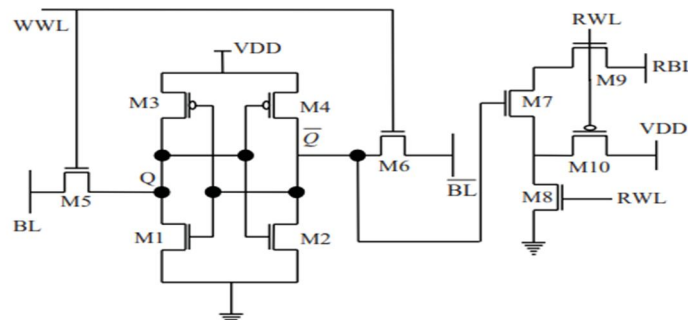


Figure 3: 10T-E1 SRAM cell

10T-E1 is modified in by designing the SRAM cells with NMOS-only based read ports as depicted in Fig 4 and Fig 5 (referred to as 10T-E2 and 10T-E3). These designs use a separate read port consisting of four NMOS transistors (R1, R2, R3, and R4) to perform the read functionality.

The isolated read ports in both the designs cause a destruction-free read operation with better read stability. Bit Line Leakage is also improved in such cases as the separated read port uses a stack of transistors. But Fig 4 is still data dependent whereas Fig 5 maintains a complete data-independent leakage path.

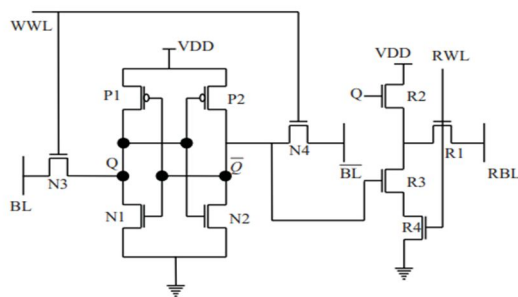


Figure 4: 10T-E2 SRAM cell

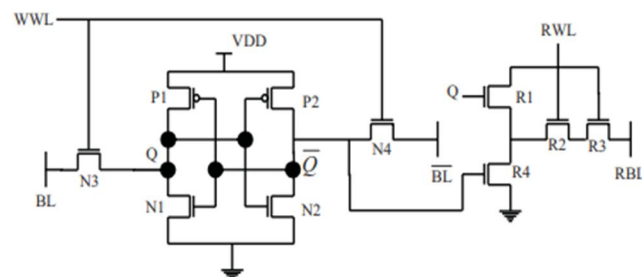


Figure 5: 10T-E3 SRAM cell



### III. PROPOSED WORK

#### A. Proposed Transmission Gate Based 8t Sram Cell

The existing cells succeed in improving the read stability but at the cost of an increase in area as they require more number of transistors to do so. However, for many applications such as Biomedical and Wireless, area occupancy also plays a vital role. If considered in Biomedical Implants, less area occupancy of the device inside the body provides less invasive to the human body.

In view of such an issue related to the SRAM design, this brief presents a Transmission gate based 8T SRAM cell as shown in Fig 1. This design reduces the area occupancy by eliminating the peripheral circuitry.

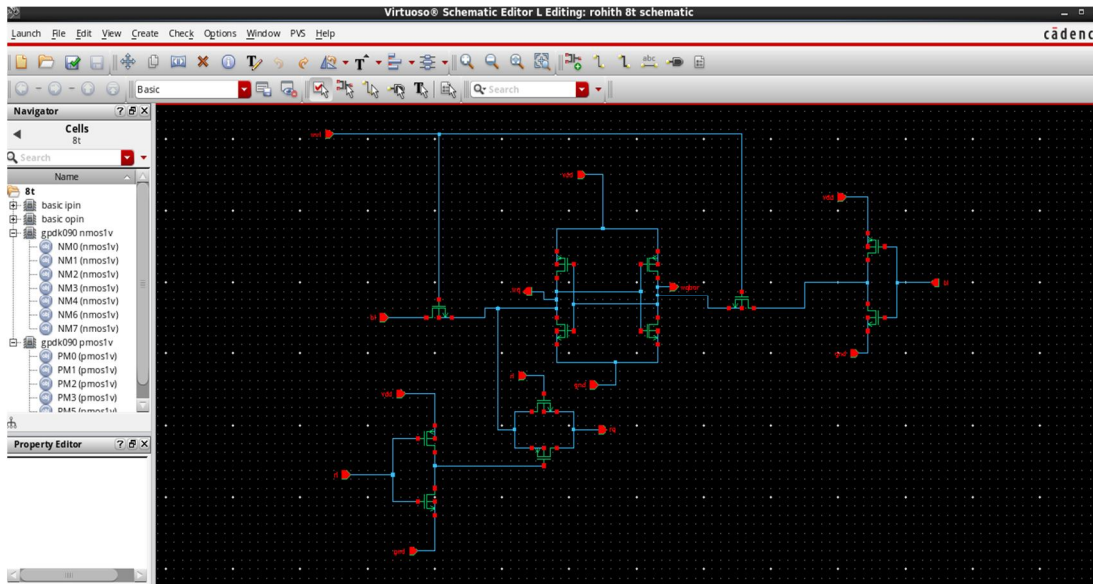


Figure 1: Proposed Transmission Gate Based 8T SRAM Cell

The proposed design chiefly concentrates on the read operation, which in the existing designs exclusively instills on the peripheral circuits. The Write operation is homogeneous to the Conventional and the other SRAM cells.

The Write functionality is controlled by the Word Line (WWL). The content which we are inclined to write is given to the Bit Lines BL and BL Bar. Now, the enabled Word Line, making the access transistors active, allows the data of the Bit Lines to intrude into the memory cell. The intruded data will thus be cached into the two storage nodes WQ and WQ Bar.

### IV. EXPERIMENTAL RESULTS

The tools used are Cadence Virtuoso and the technology used is 45nm.

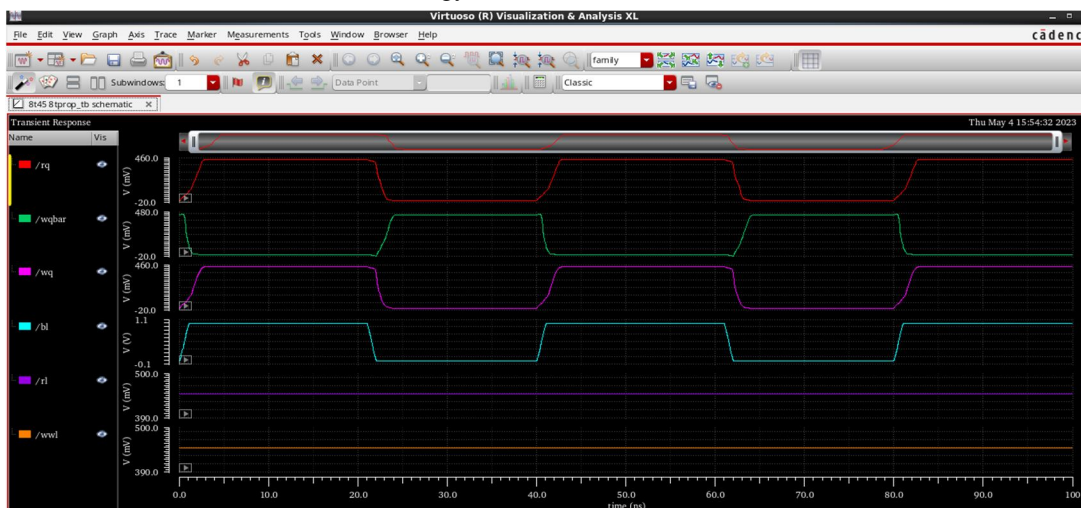


Figure 2: TG-8T SRAM simulation result using 45nm technology

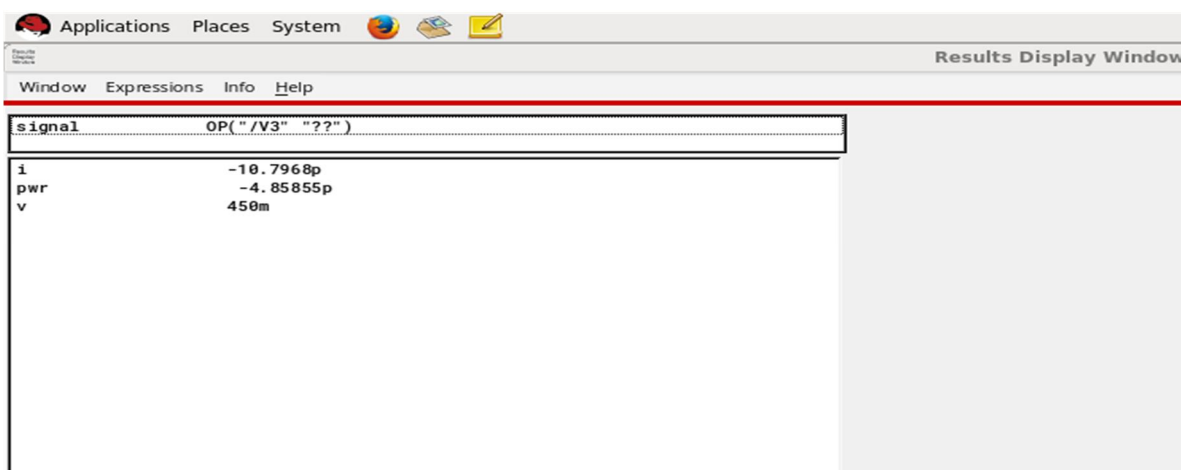


Figure 3: Proposed SRAM read power result using 45nm technology.

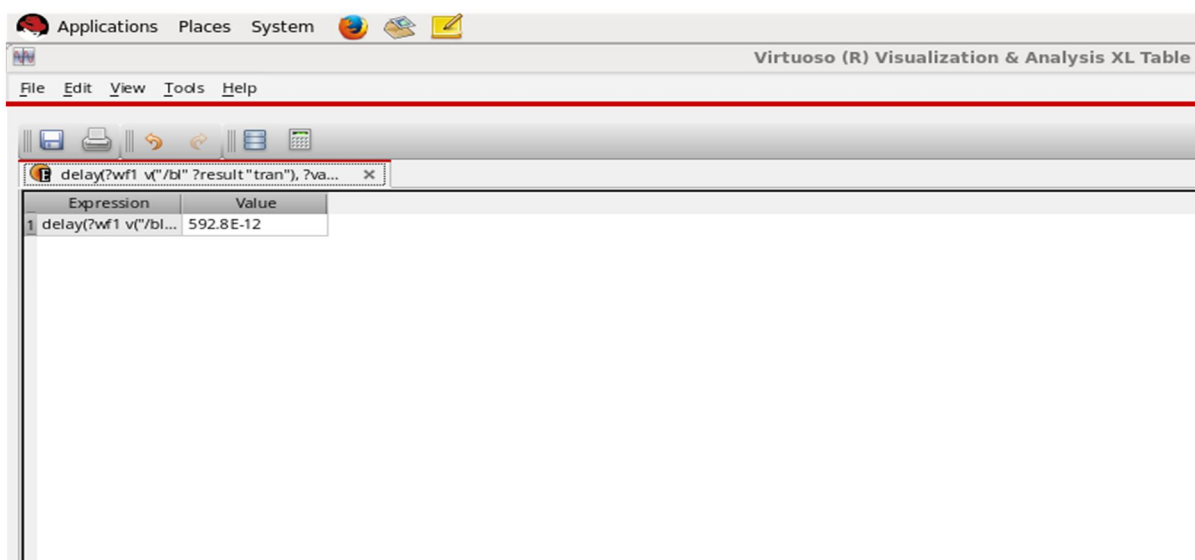


Figure 3: Proposed SRAM delay result using 45nm technology.

### V. ANALYSIS OF RESULT

Results mainly contains information regarding performance analysis of different parameters of SRAM's.

Using 45nm Technology.

	C6T	8T	10T-E1	10T-E2	10T-E3	8T-P
Technology	45	45	45	45	45	45
Supply (mv)	450	450	450	450	450	450
Read Power (w)	112.2n	19.84n	12.74n	12.73n	12.74n	4.8585p
Read Delay (s)	0.3106 $\mu$	0.077 $\mu$	0.0756 $\mu$	0.0629 $\mu$	0.0775 $\mu$	592.8E12

## VI. CONCLUSION

In this paper, Cadence virtuoso tool along with 45nm technology is used to observe the behaviors of different types of SRAM. This design provides a virtuous improvement in Delay and Area. This proposed work enlarges the overall performance of the system by reducing complexity and cost. By analyzing overall performance, the proposed SRAM has more advantages. The Speed is also improved to some extent from the existing SRAMs.

## REFERENCES

- [1] G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M.-T. Chen, Z. Foo, D. Sylvester, and D. Blaauw, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in Proc. of IEEE Int. Solid State Circuits Conf. Dig. Tech. Papers, Feb. 2010, pp. 288-289.
- [2] A. P. Chandrakasan, D. C. Daly, J. Kwong, and Y. K. Ramadass, "Next generation micro-power systems," in Proc. of IEEE Symp. VLSI; Circuits, Jun. 2008, pp. 2-5.
- [3] Liang Wen, Xu Cheng, Keji Zhou, Shudong Tian, and Xiaoyang Zeng, "Bit-Interleaving-Enabled 8T SRAM With Shared Data-Aware and Reference-Based Sense Amplifier", IEEE Transactions on Circuits and Systems, vol. 63, No. 7, July 2016.
- [4] N. Maroof and B.-S. Kong, "10T SRAM using Half-VDD precharge and row-wise dynamically powered read port for low switching power and ultralow RBL leakage," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 4, pp. 1193-1203, Apr. 2017.
- [5] J. P. Kulkarni and K. Roy, "Ultralow-voltage process-variation tolerant Schmitt-trigger-based SRAM design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 319-332, Feb. 2012.
- [6] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "Low-power embedded SRAM modules with expanded margins for writing," in proc. of IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2005, pp. 480-481.
- [7] T.-H. Kim, J. Liu, and C. H. Kim, "A voltage scalable 0.26 V, 64 kb 8T SRAM with Vmin lowering techniques and deep sleep mode," IEEE J. Solid-State Circuits, vol. 44, no. 6, pp. 1785-1795, Jun. 2009.





10.22214/IJRASET



45.98



IMPACT FACTOR:  
7.129



IMPACT FACTOR:  
7.429



# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089  (24\*7 Support on Whatsapp)