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Mechanism to Regulate DC Fault Currents in DC Solid State Transformers under Continuous Working Performance of Multi-Terminal HVDC Systems

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***Abstract:** Once the pole-to-pole dc fault occurs in a multi-terminal HVDC system, it is desirable that the stations and dc solid-state transformers on healthy cables continue to operate, rather than blocking. To reduce the fault current of a modular multilevel converter based dc solid-state transformer, active fault current control is proposed, where the dc and ac components of fault arm currents are controlled independently. By dynamically regulating the dc offset of the arm voltage rather than being set at half the rated dc voltage, the dc component in the fault current is reduced significantly. Additionally, reduced ac voltage operation of the dc solid-state transformer during the fault is proposed, where the ac voltage of transformer is actively restricted in the controllable range of both converters in the transformer to effectively suppress the ac component of the fault current. The fault arm current peak and the energy absorbed by the surge arrester in the dc circuit breakers are reduced by 31.8% and 4.9% respectively, thereby lowering the capacities of switching devices and circuit breakers. The novel active fault current control mechanism and the essential control strategy are presented and simulation results confirm its feasibility.*

I. INTRODUCTION

The deregulation of international energy markets and the trend to decentralized power generation are increasing the demand for advanced power electronic systems. For this application field multilevel converters with a high number of voltage levels seem to be the most suitable types, MMC was first proposed for HVDC applications at 2003from a Marquardt and it is first employed commercially in Trans Bay Cable project in a San Francisco. In the present scenario the Modular Multi-Level Converter (MMC) is becoming the most common type of a voltage source converter for HVDC applications. DC fault protection is an issue to be resolved for the development of modular multilevel converter (MMC) based HVDC transmission systems.[1-4]. The dc circuit breakers (DCCBs) have the potential to isolate a dc fault and protect stations from damage and limiting reactors are series connected with the fast acting DCCBs (e.g. solid-state DCCBs, hybrid DCCBs) to limit the fault current *di/dt* and decrease the fault current peak. Recently, the concept of the dc solid-state transformer (DCT) has been proposed which uses active controlled power electronic components to optimize converter performance.[6-9]. Similar to the ac transformer, the dc solid-state transformer can adapt the dc voltage to any higher or lower voltage level. By blocking all the converters of the dc solid-state transformer, dc faults can be isolated without significantly affecting the healthy system parts. Thus, the dc solid-state transformer appears the only approach to connect and interconnect existing HVDC links with different dc voltages. These transformers are available in different configurations which include the thyristor based solid-state transformer[10],the dual-active bridge (DAB) transformer[11], and the MMC based transformer[12]. Due to extremely low switching losses and improved harmonic characteristics, the MMC based dc solid-state transformer is an attractive approach, hence it is considered in this paper. The aim of this study is to use active control of the dc fault currents to reduce current stresses on solid-state transformer and DCCBs during ride-through operation of the healthy parts of a multi-terminal HVDC system under a dc fault. The paper is organized as follows. In Section II, the radial three-terminal HVDC system incorporating a solid-state front-to-front dc transformer is presented. In Section III, novel active control of the fault current is proposed, where the dc and ac components of fault currents are regulated independently. Testing the proposed scheme during ride-through operation assessed in Section IV, considering a pole-to-pole dc fault at the dc-link node of a three-terminal HVDC system. Finally Section V draws the conclusions.

II. DESCRIPTION OF THE TOPOLOGY

A. Network Outline

A terminal station with a different dc voltage rating is connected to the main HVDC link through a dc solid-state transformer. When a dc fault is applied at a dc cable, the solid-state transformer on the faulty cable can be blocked quickly to isolate the fault from the healthy main HVDC link. Thus the stations on main HVDC link can be operated continuously. However, a fault on the main HVDC link is not considered.

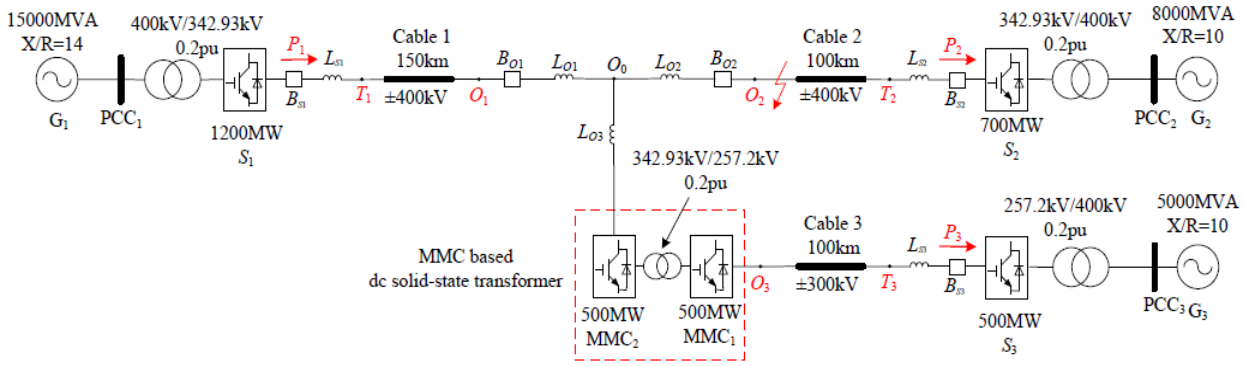

Fig.1 Radial three terminal HVDC system incorporating DC solid-state transformers

Radial three terminal HVDC system is shown in the above fig.1 it is constructed using 3 cables of different length and voltage rating which are indicated in the fig.1, dc inductances and DCCBs are at the both ends of Cables 1 and 2 and one end of Cable 3 (*T*3) to limit the fault current increase rate and isolate the fault, The other end of Cable 3 (*O*3) is connected to the dc-link node through a dc solid-state transformer to match the dc voltage of station *S*3 (±300kV) to that of the main HVDC link (±400kV). As shown in Fig.1, the dc solid-state transformer is composed of two MMCs (MMC1 and MMC2) which are front-to-front connected through a three-phase ac transformer. Both MMCs in the dc transformer, Both MMCs in the dc transformer, as well as the stations *S*1, *S*2, and *S*3, employ the generic MMC topology with half-bridge (HB) submodules (SMs). The parameter details of the test system are listed in Table 1.As the active fault current control to be proposed does not depend on the fundamental operating frequency of the dc transformer, the DCT MMCs are operated at 50Hz for simulation simplicity. With a higher operating frequency, for example, 500Hz, the SM capacitance, arm inductance, and three-phase ac transformer sizes can be reduced significantly, but at the expense of higher switching losses.[14, 15].

Table: 1Nominal Parameters of Modeled Test System

PARAMETER	*Nominal value*
Rated dc voltages of DCT MMC1 and station *S*3: *Vdc*1	±360kV
Rated dc voltages of DCT MMC2 and stations *S*1 &*S*2: *Vdc*2	±400kV
Power rating of stations S1: P1	1200MW
Power rating of stations S2: P2	700MW
Power rating of station *S*3 and MMC1 & MMC2 in transformer: *P*3	500MW
SM number per arm of DCT MMC1 and station *S*3	30
SM number per arm of DCT MMC2 and stations *S*1 &*S*2	30
SM capacitor voltage: VSM	2.105kV
SM capacitance of DCT MMC1 and station *S*3	4.59mF
SM capacitance of DCT MMC2	3.46mF
SM capacitance of stations *S*1	8.3mF
SM capacitance of stations *S*2	4.84mF
Fundamental operating frequency of DCT	50Hz
Arm inductance	5%pu
Station terminal inductance	100mH
DC-link node inductance	300mH
Pi section number in the dc cable	10
R, *L*, and *C* of dc cable	9mΩ/km, 1.4mH/km, 0.23μF/km

B. Significance of DC Fault Ride-Through Process

Whenever a dc fault occurs at O_2 as shown in Fig. 1, it is desirable that stations S_1 and S_3 continue operating without disrupting power transfer between S_1 and S_3 through the solid-state transformer. This requires that there are no overcurrents in S_1, S_3 and the solid-state transformer during the fault period, while the DCCBs isolate the fault from the rest of the dc network. If slow DCCBs with 10ms opening time are employed [5, 16] and [17], it is necessary to limit the fault current increase, especially in MMC_2 of the transformer. As the fault is near MMC_2, its SM capacitors are rapidly discharged through node inductors L_{O2} and L_{O3} (MMC_2 cannot be blocked if dc fault ride-through is to be achieved) and high ac currents are likely due to the transformer ac voltages, via freewheel diodes. Thus the pole-to-pole dc fault at O_2 is the most serious fault case for ride-through operation of S_1, S_3 and the solid-state transformer, thus is considered in this paper.

C. Revised Generic MMC Average Model

The configuration of MMC keeps on changing from the day it has been invented. As MMCs typically use hundreds of SMs per arm in HVDC application, it is a burden to simulate the whole system using detailed switching models. To reduce computation time and accelerate the simulation, average models are used to evaluate MMC performance in normal operation and during a dc fault. In the prior MMC model[13] only one equivalent capacitor is employed. Thus the state equation that describes MMC behaviour is significantly reduced, resulting in model inaccuracy.[13]. But the modified average model adopted in this paper, uses 6 capacitors and can represent the MMC behavior accurately under various operating conditions, including a pole-to-pole dc fault The modified average model in Fig.2 provides reliable representation of MMC behavior during dc fault ride-through operation. This is achieved with the typical SM capacitance requirement of 30-40kJ/MVA as suggested by ABB,[21] which yields a capacitor voltage ripple in the range of ±10%. Compared to the average model with only one equivalent capacitance, the modified average model in Fig. 3 reproduces MMC behavior during dc fault ride-through operation.model derivation and switching logic is represented in [18],[19] and [20].

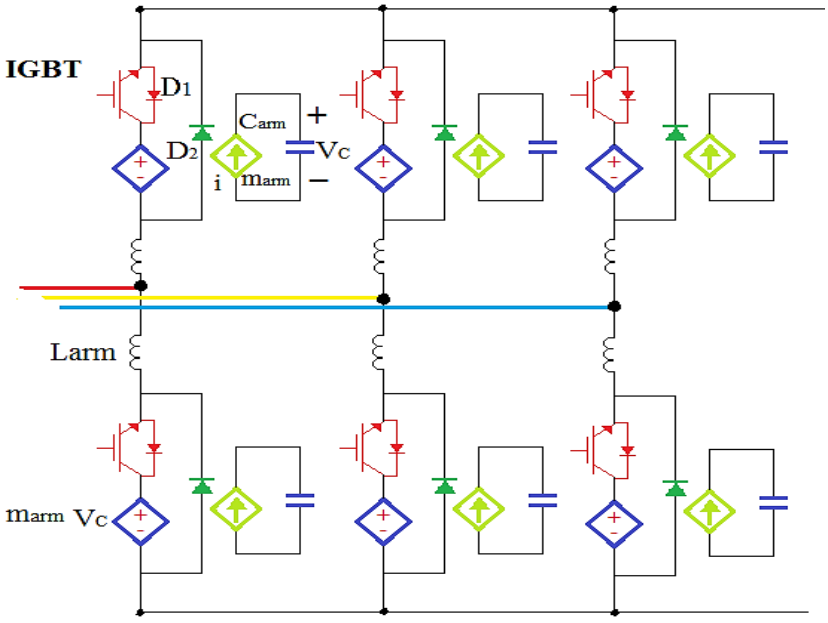

Fig.2 Modified average model of generic MMC with half-bridge sub-modules.

III. METHODOLOGY

The fault arm current during a pole-to-pole dc fault is composed of dc and ac components. In this section, active fault current control is proposed where the dc and ac fault current components are independently controlled to suppress the fault arm currents.

A. Lowering the AC Voltage of the DC Solid-State Transformer

To reduce the fault current ac component, solid-state transformer operation with reduced ac voltages is proposed, where the amplitude of the ac phase voltage is actively limited in the controllable range of both transformer converters. Thus, the ac voltage contribution to the fault current is reduced. Fig.3 illustrates the ac phase voltage in the ac component fault current control. During normal operation (t=0 to 0.03s), the peak of ac phase voltage is lower than half the rated dc voltage (600kV) and the ac currents can be regulated. Assume the actual dc voltage of the DCT MMC drops below the original peak of phase voltage *vac*, after the dc fault is applied at a dc cable at t=0.03s. By using active fault current ac component control, the ac voltage peak is limited to half the reduced dc voltage to avoid inrush currents forced by the ac voltage. Due to the reduced ac voltage, the power transfer capability of the solid-state transformer is correspondingly lowered. But this reduces the fault current significantly and thus the solid-state transformer can be operated continuously rather than having to be blocked. Additionally, the dc circuit breaker capacity is reduced by the active control.

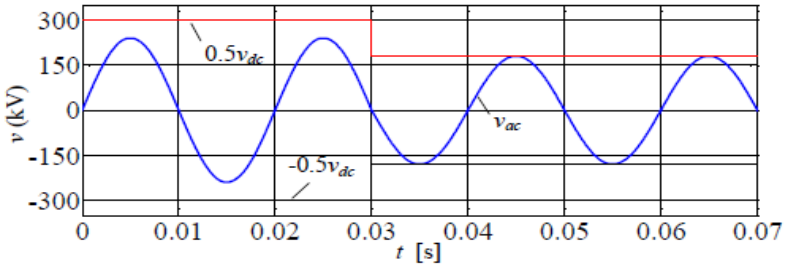

Fig.3 AC phase voltage in the proposed reduced ac voltage operation of dc solid-state transformer.

B. Fault Current regulating Methodology

The proposed active fault current control is shown in Fig. 4. MMC1 in the solid-state transformer operates in an ac voltage control mode and its control strategy is shown in Fig. 4 (a). MMC2 is assigned to control the active power with a control strategy illustrated in Fig. 4 (b), where only active dc component control for the fault current is required and the reference voltage v'_{ref2} is set by the current control loop.[22, 32]After the fault occurs, the arm inductors suffer a high fault short-circuit voltage, which causes a rapid increase of fault currents. Thus, the active dc component control of fault current is required to have a fast response and the ability to predict the future error of the system response

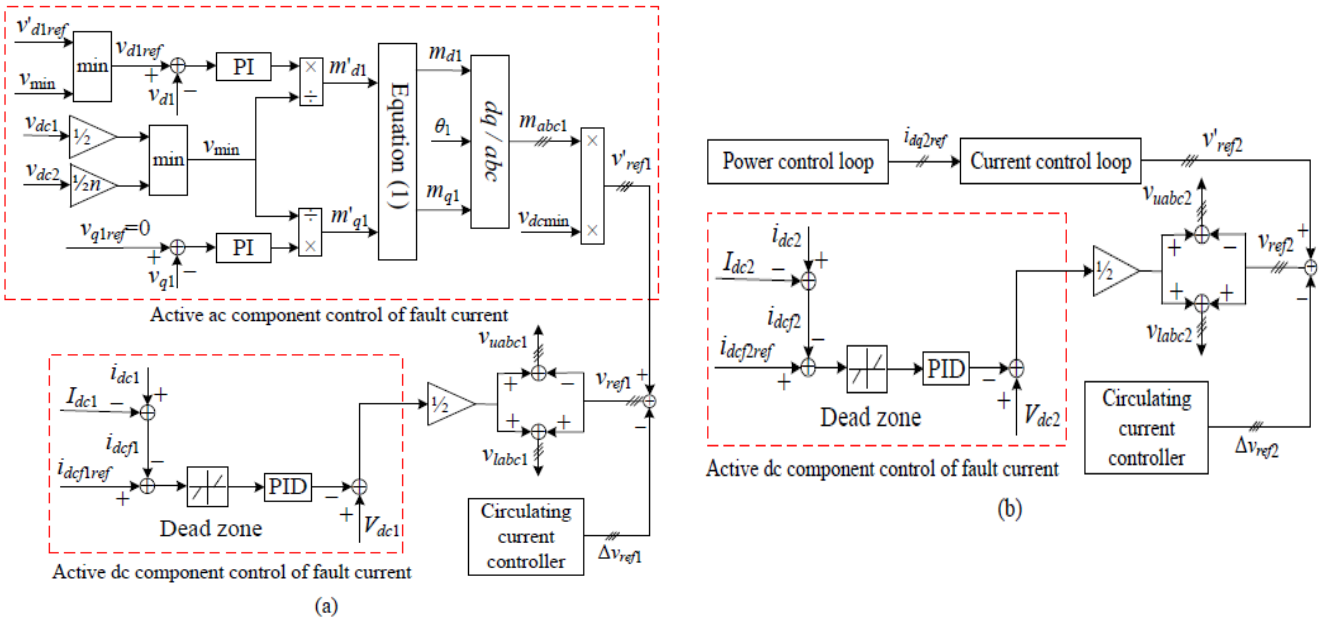

Fig.4 Active control strategy of the dc solid-state transformer: (a) ac voltage control mode and (b) power control mode.

PID control is thus used to effectively limit the dc component of the fault current, as shown in Fig. 4. The fault current dc component is obtained by subtracting the rated dc current I_{dc}(I_{dc1} and I_{dc2}, Fig. 4) from the actual dc current i_{dc}(i_{dc1} and i_{dc2}, Fig. 4) and is used as the feedback for the PID controller. During normal operation, the PID controller input is limited to zero by the dead zone block such that the arm voltage dc offsets are at their rated value. If the fault current is outside the predefined dead band, the PID controller output starts to increase from zero and regulates the arm voltage dc offsets continuously. The fault current band needs to be set such that active dc component control can quickly be enabled after the fault but avoids false activation under normal operation. The ac voltage of the dc transformer needs to be controlled and coordinated between MMC_1 and MMC_2 to ensure controllability of both MMC ac currents. As demonstrated in Fig. 4(a), PI control sets the ac side voltage of the transformer. Compared with open loop control, PI control suppresses the dc voltage variation disturbance and thus the ac voltage can be accurately set to the reference value.

The reference voltages v_{d1ref} and v_{q1ref}, Fig. 4 (a), need to be set to limit the ac phase voltage to less than half the actual dc voltage. To achieve this, the *d*-axis reference voltage v_{d1ref} is obtainedas $V_{d1ref} = \min(V^{1}_{dref}, v_{min})$ as while the *q*-axis reference voltage v_{q1ref} is set at 0. $v'_{d1ref}$is the original *d*-axis reference voltage and $v_{min}$is obtained from the minimum value of the two dc voltages of the dc transformer $v_{min}=\min(1/2\ v_{dc1}, 1/2n\ v_{dc})$where *n* is the ac transformer ratio. Thus, the ac voltages of the dc transformer are always within the control range of both MMC_1 and MMC_2 when the actual dc voltage is lower than the rated value. The inrush currents forced by the ac voltage are thus avoided by the proposed active ac component control of the fault current. The minimum voltage $v_{min}$is the base voltage for the pu values of the PI outputs m'_{d1} and m'_{q1}, which are then limited by (1) to avoid over-modulation and further limit the ac voltages within the converter control range

$$m'_{d1}=\frac{m_{d1}}{\sqrt{m_{d1}^{2}+m_{q1}^{2}}}\quad m'_{q1}=\frac{m_{q1}}{\sqrt{m_{d1}^{2}+m_{q1}^{2}}} \qquad (1)$$

The dc transformer operates with reduced ac voltage during the fault to lower the fault current and restores the rated value after the fault is isolated, in order to transfer rated power. By independently regulating the dc and ac components in the fault currents, the proposed active control significantly reduces the fault currents. This implies the submodule capacitors are discharged by a smaller fault current and their voltages can be maintained higher during a dc fault. This characteristic improves converter controllability of the dc transformer and reduces oscillation during restoration after the fault is isolated.

As the SM capacitors and the ac voltage provide less energy to the dc side fault, the converter actual dc voltage *vdc*under active control is lower than that with conventional control. Nevertheless, even with a lower converter dc voltage, the proposed active control still reduces the fault currents. The proposed fault current control is achieved by actively regulating the reference waveforms for the upper and lower arms, rather than carrier waveforms. This makes it independent on the carrier waveform arrangement and is thus valid for both of the *N*+1 and 2*N*+1 [24, 25] modulations. Once a fault is detected (generally any dc fault is detected by monitoring the voltage across link inductors *LS*1,2,3 and *LO*1,2,3), the circuit breaker *BO*2 is commanded to open with a 10ms opening time to isolate the fault from the healthy parts of the multi-terminal HVDC system. Due to the reduced fault current resulting from the proposed active control, the energy absorbed by surge arrestor in *BO*2 is reduced from 26.5MJ to 25.2MJ, a 4.9% reduction.

IV. TESTING THE PROPOSED SCHEME DURING RIDE-THROUGH OPERATION

The active fault current control during ride-through operation is assessed using the model in Fig. 1 with the parameters listed in Table I. The simulated scenario assumes the system in Fig. 1 is subjected to a permanent pole-to-pole dc fault at *O*2 at *t*=0.7s. As mentioned, the DCCBs isolate the fault after 10ms from the fault initiation. Station *S*2 is blocked after the detection of dc fault while *S*1, *S*3, and the dc solid-state transformer remain operational. [5].

From the below comparisons it can be observed that the three phase arm currents with active controlled is far better in retaining the genuine value during the pole-to-pole dc fault as compared to conventional methods which is represented in the fig5.c and 5.d also the three phase ac currents remains to be persistent even under severe pole-to-pole dc fault which is represented in the below fig5.a and fig5.b. Hence this active control strategy has a upper hand compare to the conventional control strategy.

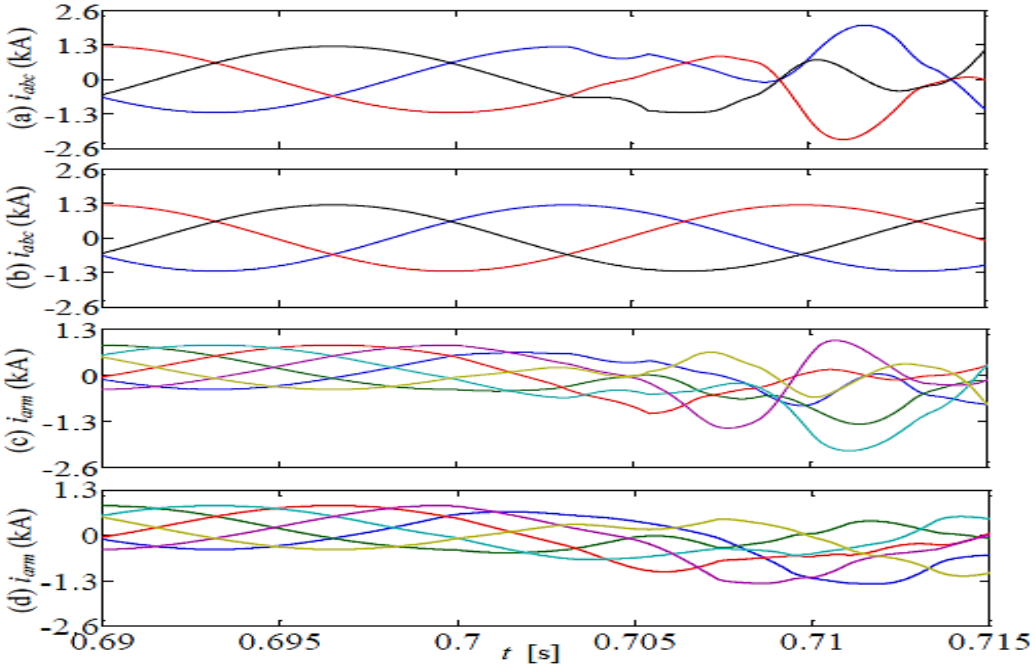

Fig.5 Comparison between conventional control and the proposed active control: (a) three-phase ac currents with conventional control, (b) three-phase ac currents with active control, (c) arm currents with conventional control, and (d) arm currents with active control.

A. Stresses on DC Circuit Breaker

Fig.6 shows the waveforms of breaker *BO*2 which is connected on the faulty branch at the dc-link node. The fault current flows through the mechanical switch until the switch opens at around t=0.71s. Then the current through the switch is commutated into the surge arrestor to limit the voltage across the circuit breaker, without exposing it to significant overvoltage. In Fig.6 (b), the voltage across the circuit breaker is lower than 600kV (1.5pu). Only circuit breaker *BO*2 opens after detecting the fault at the dc-link node while *BO*1 and the dc transformer continue to transfer power between stations *S*1 and *S*3. As a result, the voltage across the surge arrestor in *BO*1 is always around zero, so does not absorb energy during the fault. All the opening energy is absorbed by the surge arrestor in *BO*2 and this energy is almost 25MJ, as shown in Fig.6(c).

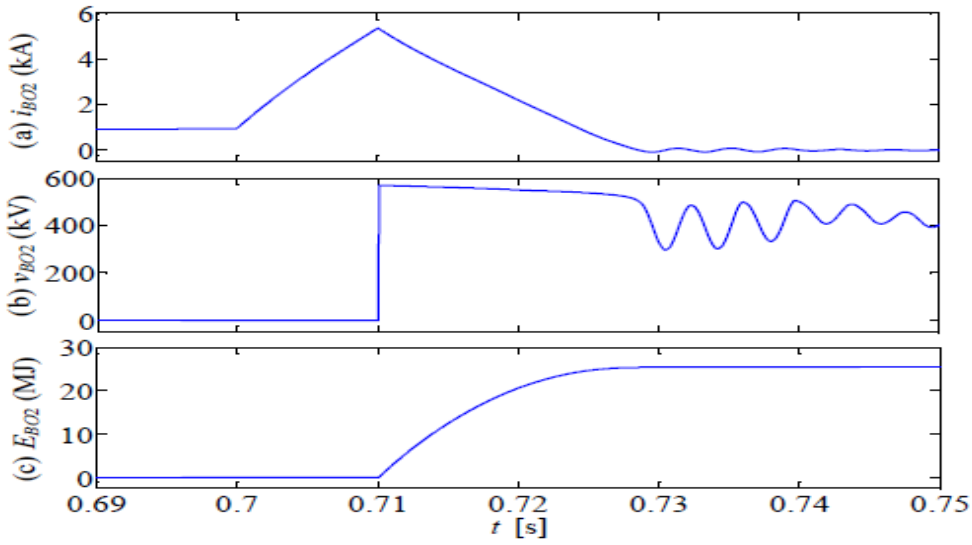

Fig.6 Waveforms of dc circuit breaker *O*2 at dc-link node: (a) current, (b) voltage, and (c) DCCB absorbed energy.

Besides *BO*2 (connected on the faulty branch at the dc-link node) opening, breaker *BS*2 at the terminals of station *S*2 also needs to open to protect station *S*2 converter. As shown in Fig.7, circuit breaker overvoltage is avoided and the energy absorbed by the surge arrestor in DCCB *BS*2 is less than 7MJ.

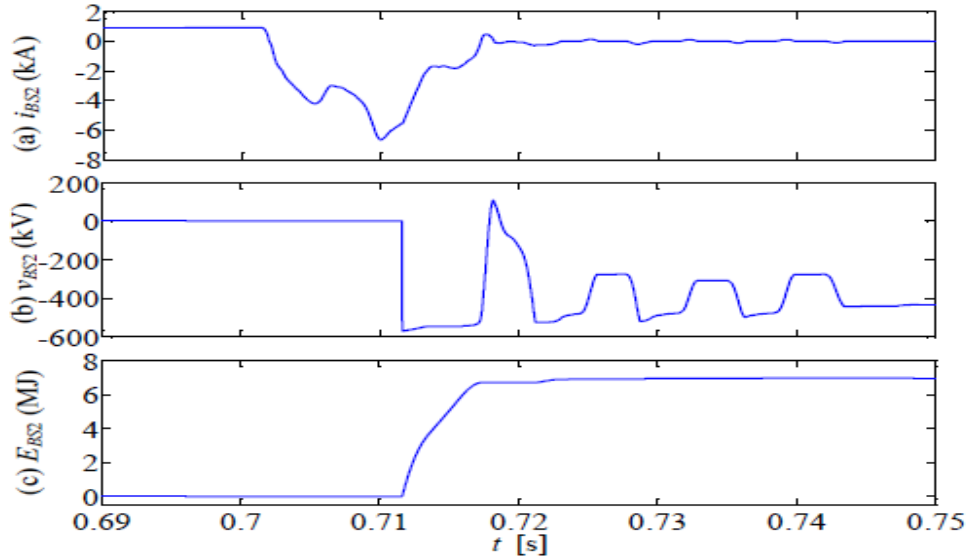

Fig.7 Waveforms of dc circuit breaker *BS*2 at terminal of station *S*2: (a) current, (b) voltage, and (c) DCCB absorbed energy.

The simulated pole-to-pole dc fault, which is the most serious fault case for ride-through operation of the dc transformer, causes disturbance for the converters on the healthy branches, especially for DCT MMC2, as it is close to the fault location. However, benefitting from the proposed active fault current control, the fault currents are significantly reduced and the submodule capacitor voltages are maintained higher during a dc fault, which improves dc transformer converter controllability and reduces oscillation during restoration, after the fault is isolated. All the fault currents are lower than the threshold (2pu) and the healthy parts are gradually restored to normal operation. DC fault ride-through operation of multi-terminal HVDC systems is thus achieved.

B. Functioning of DC Solid-State Transformer under fault

With the use of introduced active fault current control, the fault arm current crest of MMC2 in the transformer is condensed to 1.8pu, inferior than the current threshold (2pu). After the occurrence of fault the current of MMC_2 changes the magnitude from 2kA to 3kA during restoration period as shown in the fig.9

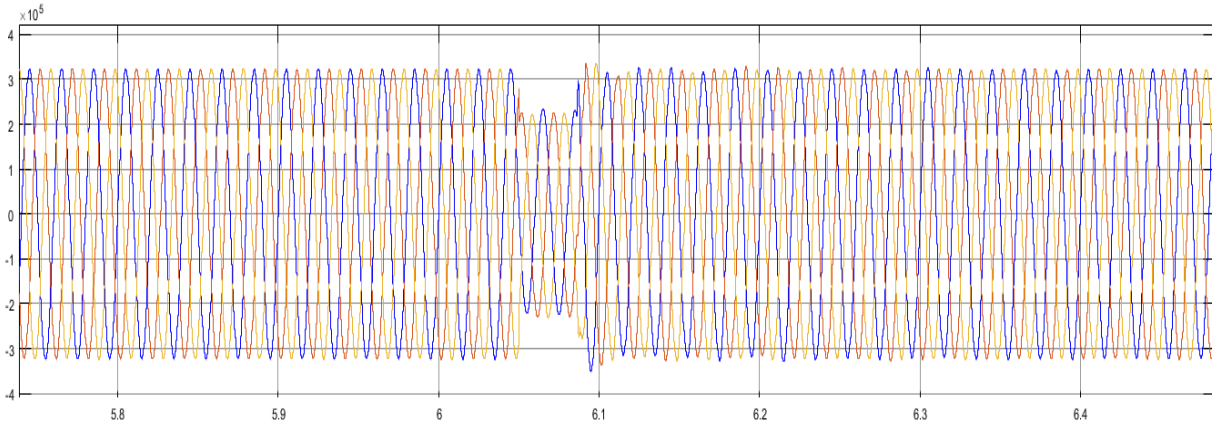

Fig.8 Voltage waveforms of MMC_1 in the dc solid-state transformer

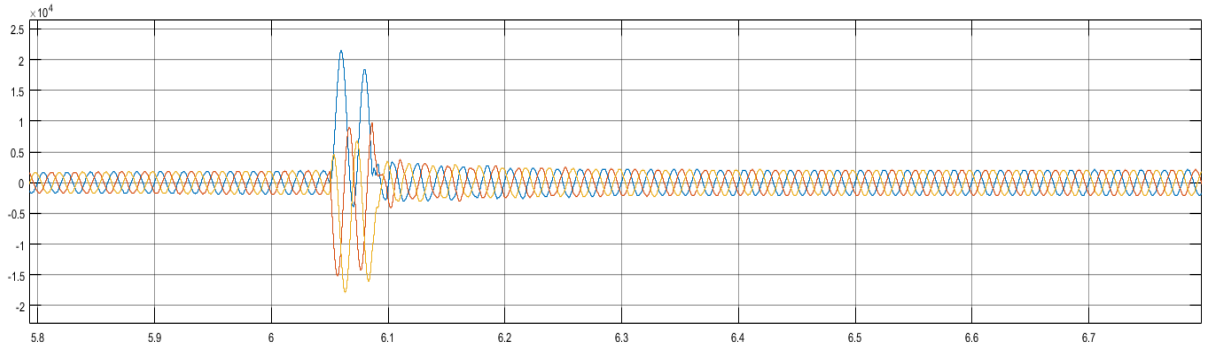

Fig.9 Current waveforms of MMC_1 in the dc solid-state transformer

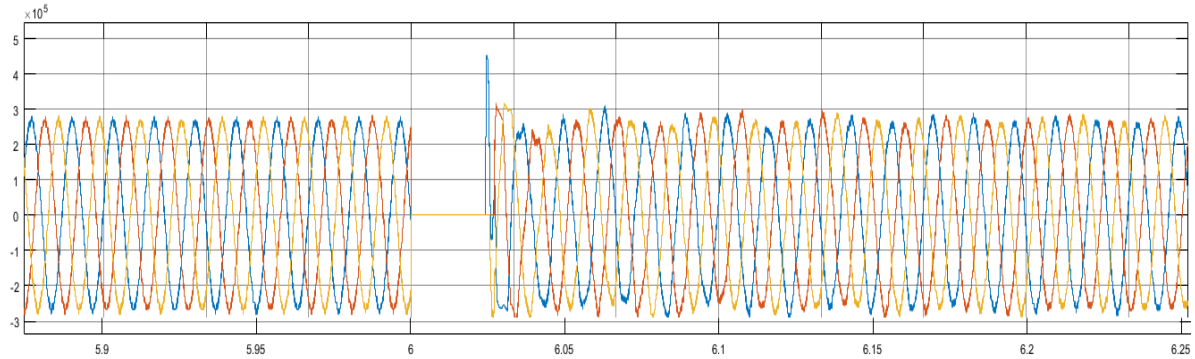

Fig.10 Voltage waveforms of MMC_2 in the dc solid-state transformer

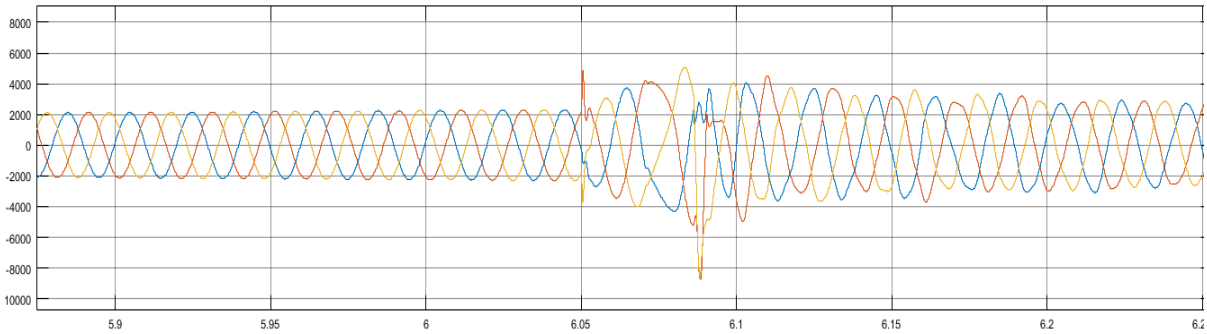

Fig.11 Current waveforms of MMC_2 in the dc solid-state transformer

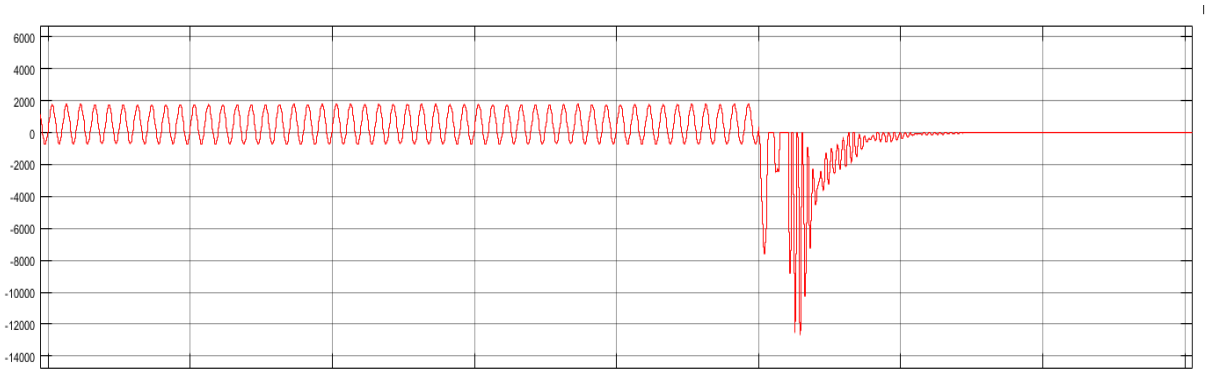

Fig.12 Upper arm current of MMC_1 converter in dc solid-state transformer

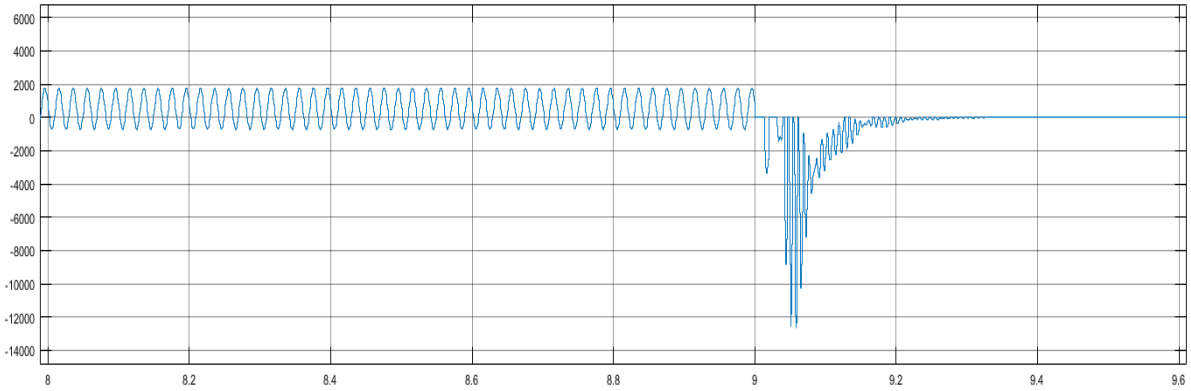

Fig.13 Lower arm current of MMC2 converter in dc solid-state transformer

V. CONCLUSION

This paper proposes active fault current control of the dc solid-state transformer during a pole-to-pole dc fault, where the dc and ac components of the fault currents are independently suppressed. The mechanism of the novel active control was analyzed and a control strategy was presented. By dynamically regulating the dc offsets in the arm voltages rather than being set at half the rated dc voltage, the dc component in fault current is reduced by the proposed active control. The ac component in the fault current is also effectively lowered with the proposed reduced ac voltage operation of the dc transformer where the ac side voltage of transformer is actively limited in the controllable range of both transformer converters. The maximum arm current peak and the energy absorbed by surge arrestor in the dc circuit breaker are reduced by 31.8% and 4.9% respectively, and thus devices with low power capacity can be potentially used, yielding reduced losses and capital cost. The dc-link inductance can be halved that recommended by using active control thus the cost and volume of the dc-link inductors are decreased. System ride-through operation with a dc fault on the main HVDC link is achieved without exposing the dc transformer or station converters to significant fault currents and over-voltages.

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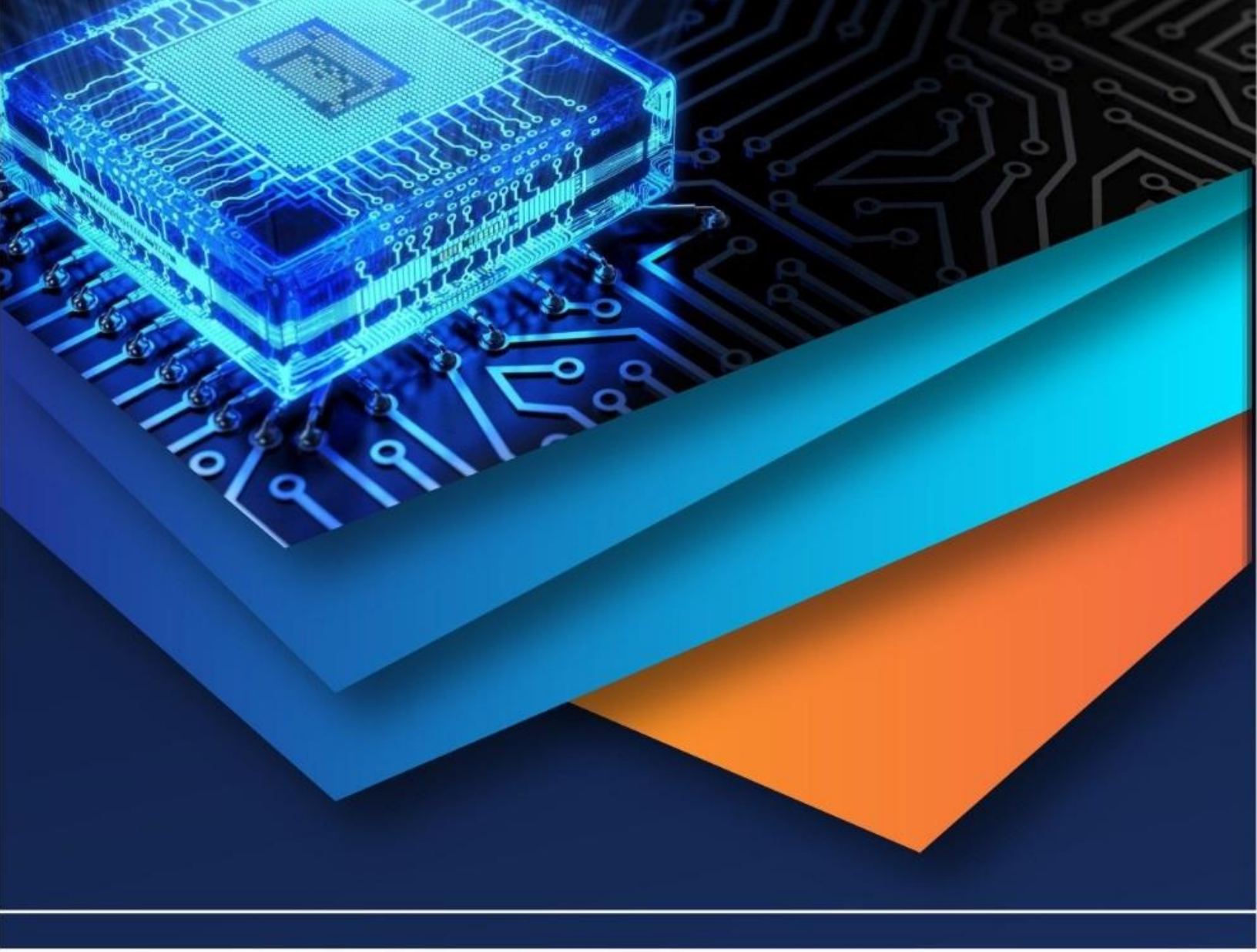

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