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Implementation of Reversible Control and Full Adder Unit Using HNG Reversible Logic Gate

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Abstract: ***Reversible logic is one of the most vital subject at present time,used to reduce the power dissipation that occurs in conventinal circuits by preventing the loss of information, in this paper we are presenting the implementation of efficient arithmetic logic i.e. reversible control unit and reversible full adder unit, using reversible HNG logic gates which can performseven logical operations and eight arithmetic operations. Alsoour focus on improving the performance parameters of design: number of constant inputs, number of garbage outputs, quantum cost, number of gates and propagation delay compared to existed designs.***

Keywords: ***Reversible logic gates, HNG gate, Control unit, Full adder, Fault,***

I. INTRODUCTION

As the complexity of VLSI circuits increases, and number of transistors on integrated circuits increases rapidly hence power dissipation by these also increases. In Conventional logic circuits, every time one bit information is lost during computation hence heat is generated due to the loss of bit. In order to avoid this loss of information the Conventional circuits are designed using Reversible logic.

is a digital circuit and it executes arithmetic and logical operations on binary numbers. It is data processing componnt in CPU. Arithmetic operations includes add, minus, increment, decrement, operations while in logical operations AND, OR, NOR and NAND, Ex-OR etc. are present. We can reduce the power dissipation if above functions can be realized by using reversible HNG gates. As we know, ALU contain control unit and adder so we need to design reversible control unit and reversible full adder. By cascading the control unit and full adder we can implement the reversible ALU. Fig 1 is the block diagram of proposed 1-bit reversible ALU design for three control signal which performs 8 arithmetic operations and 7 logical operation as mentioned in the Table 1

Table - 1 Arithmetic and logical operations

Function select				ALU Output	Adder input		Function
S_2	S_1	S_0	C_{in}		X_i	Y_i	
0	0	0	0	A_i	A_i	0	Transfer A
0	0	0	1	A_i+1	A_i	0	Increment A
0	0	1	0	$A_i + B_i$	A_i	B_i	Addition
0	0	1	1	$A_i + B_i + 1$	A_i	B_i	Addition with carry
0	1	0	0	$A_i + B_i - 1$	A_i	$\bar{B}i$	Subtraction with borrow
0	1	0	1	$A_i - B_i$	A_i	$\bar{B}i$	Subtraction
0	1	1	0	$A_i - 1$	A_i	1	Decrement A
0	1	1	1	A_i	A_i	1	Transfer A
1	0	0	0	$A_i \vee B_i$	$A_i \vee B_i$	0	OR
1	0	0	1	$\overline{Ai \vee Bi}$	$A_i \vee B_i$	0	NOR
1	0	1	0	$\bar{A}i$	A_i	1	Complement A
1	0	1	1	$A_i \wedge B_i$	$A_i \wedge \bar{B}i$	$\bar{B}i$	AND
1	1	0	0	$\overline{Ai \wedge Bi}$	$A_i \wedge \bar{B}i$	$\bar{B}i$	NAND
1	1	0	1	$A_i \oplus B_i$	A_i	B_i	EXOR
1	1	1	0	$\overline{A_i \oplus B_i}$	A_i	B_i	EXNOR

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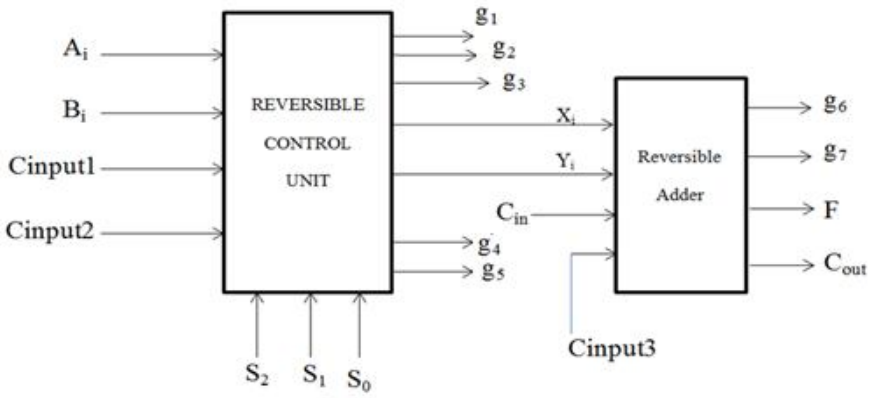

Fig 1 block diagram of proposed 1-bit reversible ALU design.

II. LITERATURE REVIEW

The amount of energy (heat) dissipated for every irreversible bit operation is given by $KTln2$, which is small but not negligible[1]. If we could compute entirely with reversible operations, there would be no lower limit on energy consumption.$kTln2$ energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Low-power multiplexer-based 1-bit full adder that uses only 12 transistors and the new adder has more than 26% in power savings over conventional 28-transistor CMOS adder. Also, it consumes 23% less power than another 10-transistor adder and is 64% faster [3]. Low power operations [4], which can use the lowest possible supply voltage coupled with architectural, logic style, circuit and technology optimizations. A synthesis model and a synthesis procedure which allow us to minimize the number of garbage outputs [5], in reversible circuit and also showed that the new gates differ only marginally from the generalized TOFFOLI gates.Oracle Synthesized circuits [6] for Grover'ssearch algorithm and shown a significant improvement over previously proposed synthesis algorithms and also showed constructively that every even permutation can be implemented without temporary storage using NOT, CNOT and TOFFOLI gates. Four designs for Reversible full-adder circuits [7] and the implementation of these logic circuits into electronic circuitry based on CMOS technology and pass-transistor design. A 3x3 Reversible TKS gate [8] with two of its outputs working as 2:1 multiplexer. A implementation of Binary Coded Decimal adder in Reversible logic, [9] which is basis of ALU for reversible CPU.A general approach to construct the Reversible full adder and can be extended to a variety of Reversible full adders with only two Reversible gates [10]. Various adder/subtractor circuit designs and showed that design III is good and optimized [11], Design full adder circuit using IG gates and MIG gates with constant inputs of 2 and Garbage output of 3, and designed Fault Tolerant Reversible Carry Look-Ahead and Carry-Skip Adders [12].Two types of reversible Arithmetic Logic [13] Unit (ALU) designs and implemented using Altera Quartus II tool. And it can perform 8 arithmetic and 4 logic operations. A new design of Arithmetic and Logic unit made with effective Reversible control unit and reversible full adder [14], ALU has been verified and implemented using Verilog and Quartus II 5.0 software.

III. PROPOSED WORK

The design is shown in Fig.2 is reversible ALU design based on reversible logic gates. In this design, Full adder is realized with HNG gate, Control unit and full adder are cascaded to construct ALU. Total number of gates 6, garbage outputs 6, Constant inputs 3 and quantum cost 22. The proposed 1-bit ALU synthesized using VHDL on Xilinx ISE Design is shown in Fig.3. Synthesis report shows that maximum propagation delay is 6.92ns.

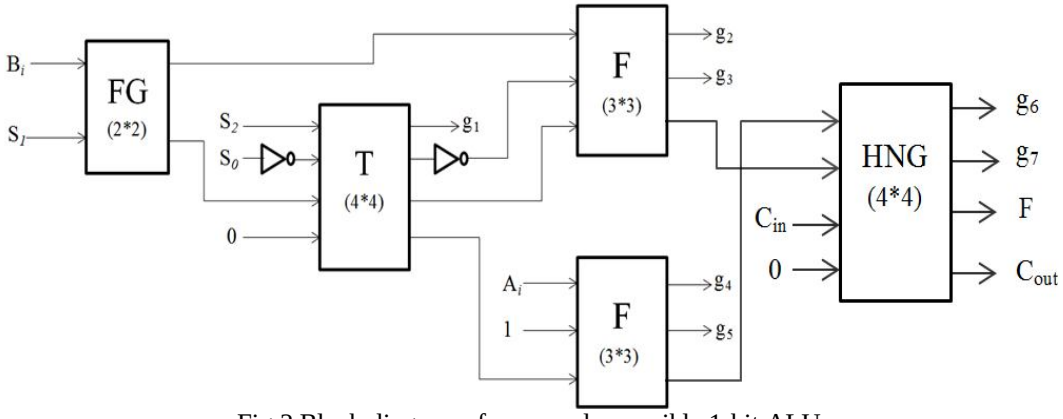

Fig 2 Block diagram of proposed reversible 1-bit ALU

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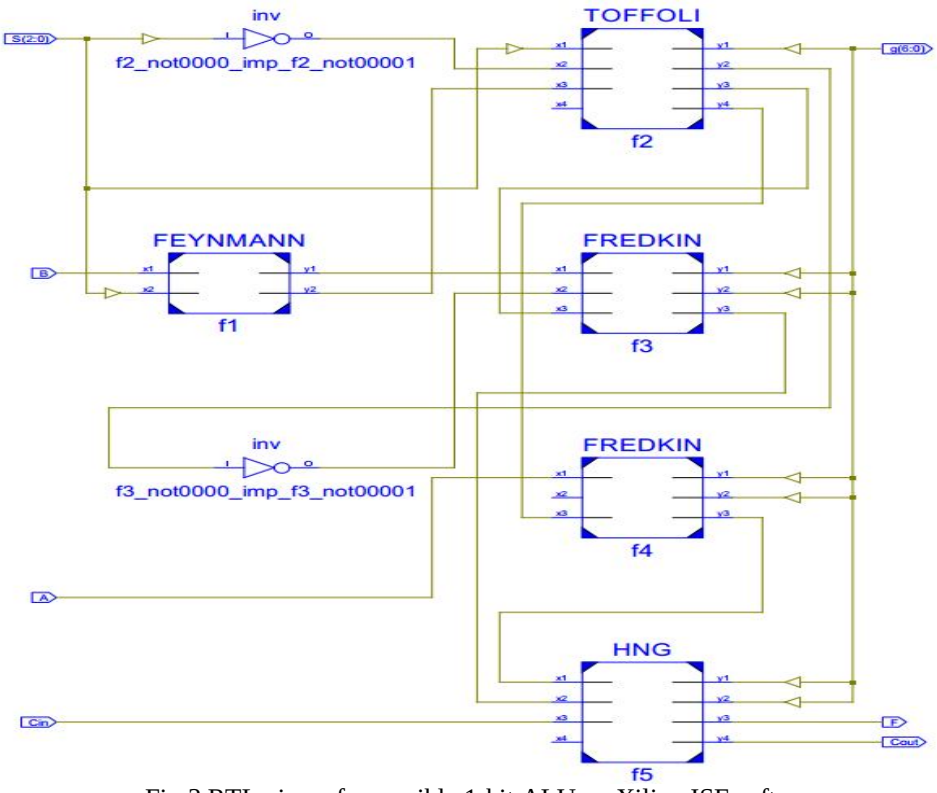

Fig 3 RTL view of reversible 1-bit ALU on Xilinx ISE software

The control unit in fig 4, processing the input operands A_i and B_i under the control of control veriables S_2, S_1 and S_0 then combined parameters X_i and Y_i will be generated at output of Control unit. Three control signals S_2,S_1 and S_0along with C_{in} select fifteen operations, and S distinguishes between arithmetic and Logical operations.

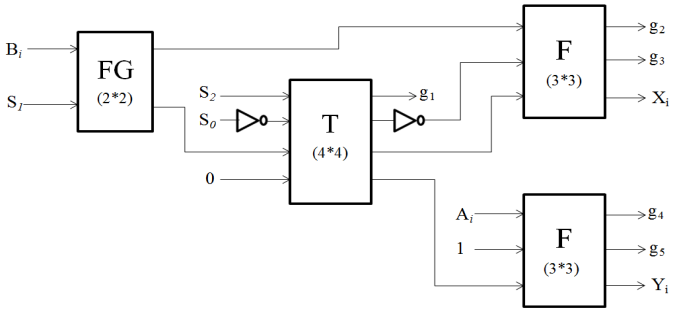

Fig 4 Block diagram of reversible Control Unit

The reversible full adder build by using HNG gate [15,16] is shown in the Fig.5. This gate having inputs are $A, B$and C_{in}, outputs S and C_{out} are Sum and Carry respectively. One constant input and two garbage outputs present. Quantum cost of this reversible full adder is 6.

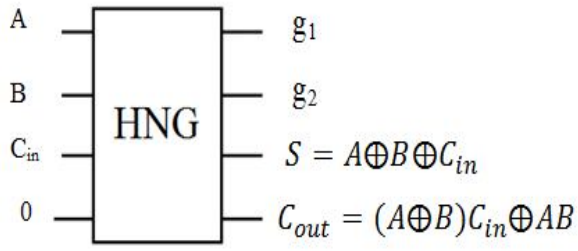

Fig.5 Full adder using HNG gate

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Fig. 6 showing the block diagram of conventional ALU, which can perform fifteen operations as mentioned in Table1. The control unit processing the input operands A_i and B_i under the control of control veriablesS_2,S_1 and S_0, then combined parameters X_i and $Y_i$will be generated at output of Control unit. Three control signals S_2,S_1 and S_0along with C_{in} select fifteen operations, and S distinguishes between arithmetic and Logical operations. Implementation of Conventional 1-bit ALU using Verilog HDL is shown in the Fig.6. Synthesis report shows that Propagation delay of conventional ALU is 8.133ns.

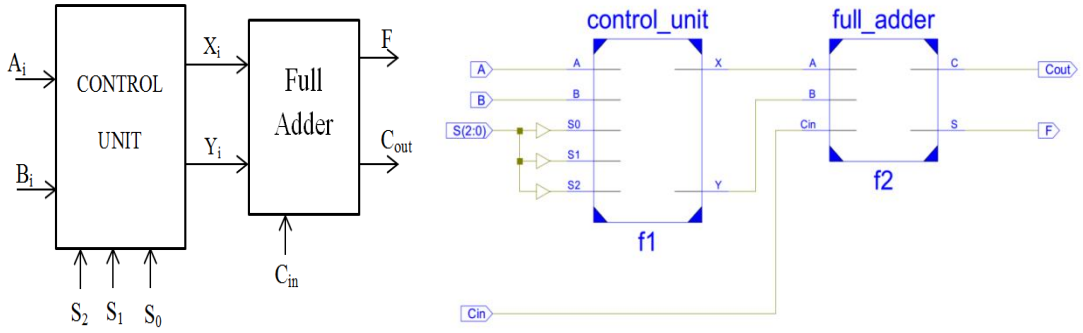

Fig 6Block diagram and RTL view of conventional 1-bit ALU on Xilinx ISE

IV. SIMULATION RESULT

The Fig.7 showing the output waveforms satisfy the function Table1 For A_i = 1and B_i = 0.

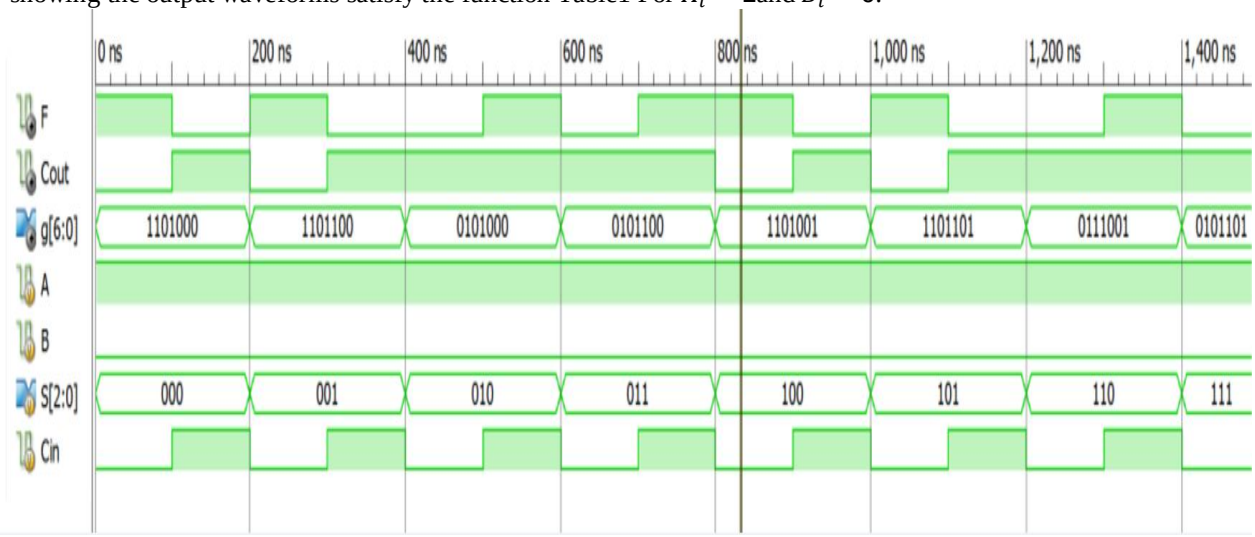

Fig.7 Output waveforms for functions in Table1 For A_i = 1and B_i = 0.

There are basically two input operands $A$and B, depending on the values of S_2,S_1, $S_0$and C_{in} we can get different Arithmetic and logic operations on F and C_{out} as per the above Table 1.

Table 2Performance Parameters

Performance parameters	Proposed 1-bit ALU	Existed 1-bit ALU
Constant inputs	3	5
Garbage outputs	6	11
Gate count	6	9
Quantum cost	22	27

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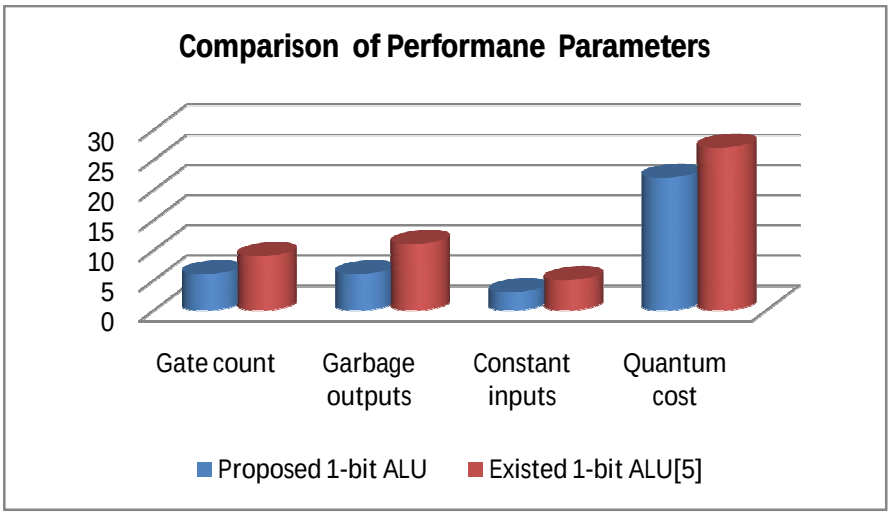
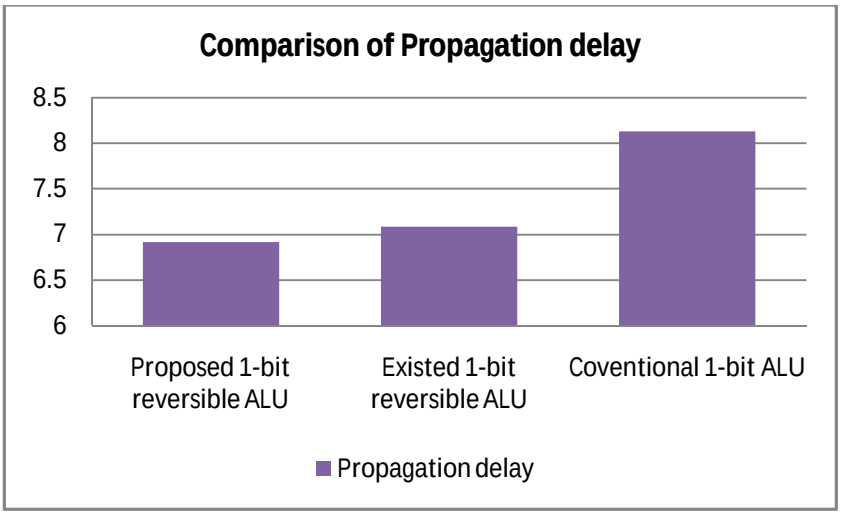


The Verilog code is synthesized using Xilinx RTL compiler for the delay analysis of proposed reversible ALU.Table 3 shows the propagation delay analysis of proposed 1-bit ALU and existed 1-bit ALU[5] and Conventional 1-bit ALU. It can be concluded that proposed reversibleALU design shows higher reduction in delay in compared with existed design and conventional design

Table 3Comparison of Dealy

ALU Designs	Propagation delay
Proposed 1-bit reversible ALU	6.92 ns
Existed 1-bit reversible ALU	7.17 ns
Coventional 1-bit ALU	8.133 ns



IV. CONCLUSION

In this paper, 1-bit reversible ALU i.e. reversible control unit and reversible full adder unit, using reversible HNG logic gates has been implemented on Xilinx ISE design suite 14.7 tool. We have compared this proposed design with the existing designs in terms of reversible gates used, Garbage outputs, Quantum Cost, constant inputs and number of logical & arithmetic functions. Arithmetic & logical unit using reversible control unit has also great improvement over existing designs.It has 6 gate count, 6 garbage output, 22 Quantum cost, 3 constant input which are less in compare to existing design. Reversible computing has its great significance in reducing the complexity of the digital circuits. Reversible logic has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing, quantum dot cellular automata, communication and computer graphics.In future we candesign complete reversible computer architecture with the help of proposed designs.

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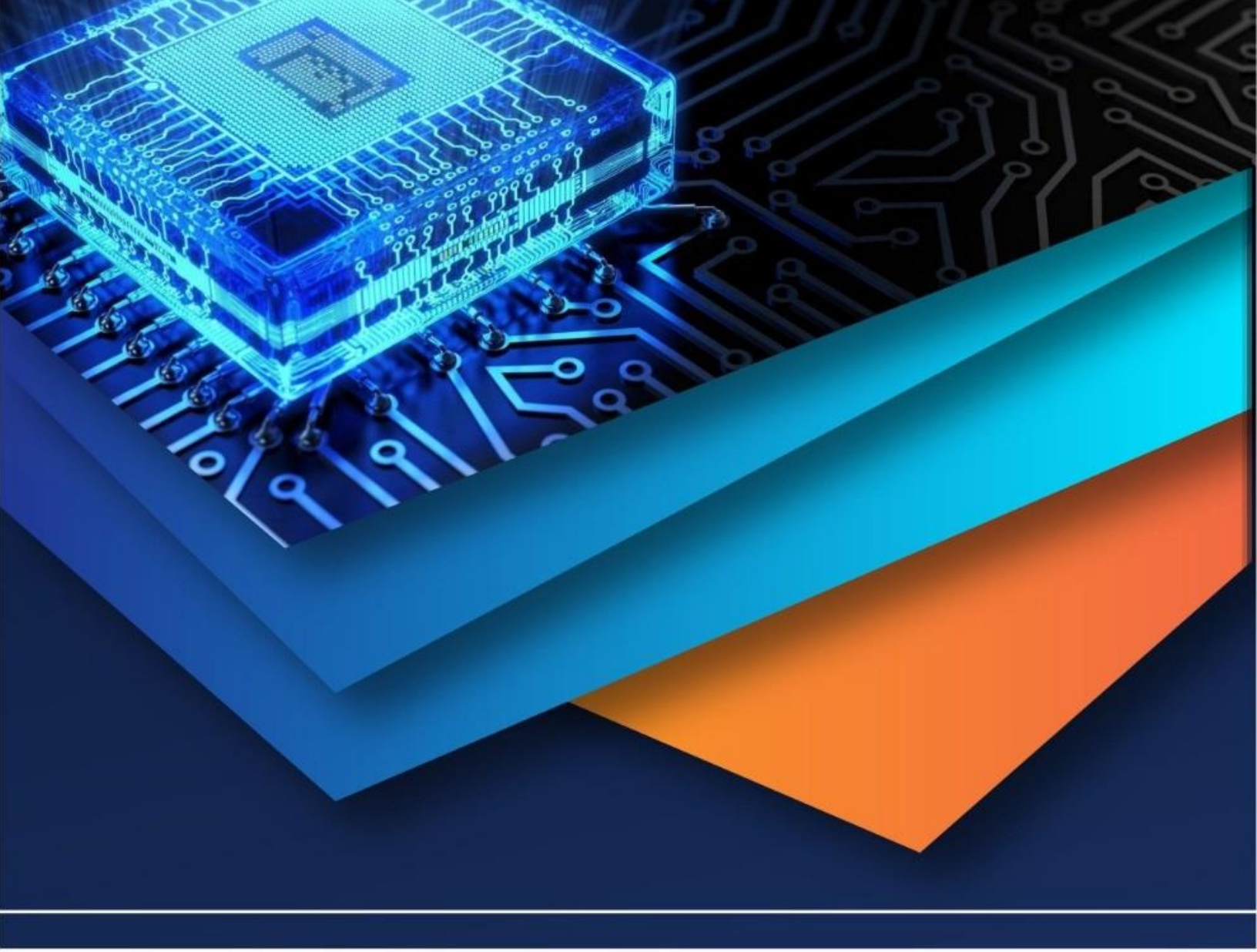

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