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Design Analysis of Charge-Pump Phase Locked Loop with Analogy Lock Signal Generator

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Abstract*: In this paper a design of 450 MHz CP-PLL (Charge Pump Phase-locked Loop) with lock signal generator (LSG) is presented as Phase-locked Loop (PLL) is a circuit in modern integrated circuit design implementations. Here, the implemented PFD (Phase Frequency Detector), CP (Charge Pump) and LP (Loop Filter) circuit to produce a stable control voltage for the voltage controlled oscillator (VCO). Finally, the desired frequency was generated under locked condition using the VCO. A frequency divider circuit was also implemented to divide the output frequency of VCO by 16. Finally, the behaviour of PLL was determined through Analog Lock Signal Generator Circuit.

Keywords: ***IPLL, PFD, CP, VCO, LSG, LP***

I. INTRODUCTION

PLL (Phase-locked loop) today, is a promising concept to design modern integrated circuit. In this project, a CP-PLL (Charge Pump PLL) has been designed for the frequency of 450 MHz with Analog Lock Signal Generator (LSG). At the very first of the project, I implemented Phase Frequency Detector (PFD) that has two input signals of same frequency with different phase. Then, I designed a Charge Pump (CP) circuit that combined the two outputs of the PFD into one output and hence I determined a Loop filter to produce a controlled voltage that drives the Voltage Controlled Oscillator (VCO). In addition, the corresponding output of the VCO is divided by a divider circuit (N=16) which was used as feedback to the input of PFD. At the end a LSG circuit has been designed to determine whether our PLL is locked or not on the basis of implemented design.

Phase-locked loop (PLL) is used very widely for clock generator, frequency synthesis, and clock / data revival. A browsing through the phase-locked loop literature of the past is very resourceful. Although I often consider phase-locked loops as relatively new structures, historical literature dates the concept as early as 1919. Vincent and Appleton experimented and analysed, respectively, the practical synchronization of oscillators. [1] In addition, CHARGE-PUMP based phase-locked loops (CPLL) are widely used as clock generators in a variety of applications including microprocessors, wireless receivers, serial link transceivers, and disk drive electronics. One of the main reasons for the widely adopted use of the CPLL in most PLL systems is because it provides the theoretical zero static phase offset, and arguably one of the simplest and most effective design platforms. The CPLL also provides flexible design trade-offs by decoupling various design parameters such as the loop bandwidth, damping factor, and lock range. While there are numerous CPLL design examples in the literature, precise analysis and a mathematical clarity of the loop dynamics of the CPLL is lacking. The two most popular references in this arena by Hein and Scott and Gardner, provide useful insight and analysis for second-order PLLs. However, they do not provide a complete and extensive analysis for practical integrated circuit (IC) PLLs, i.e., third-order CPLLs [2].

II. PURPOSE

The main purpose of this design is to design a CPLL and observe the behaviour of PLL on the basis of LSG that determine whether the PLL is locked or not and hence analyse the simulations and results of corresponding circuits.

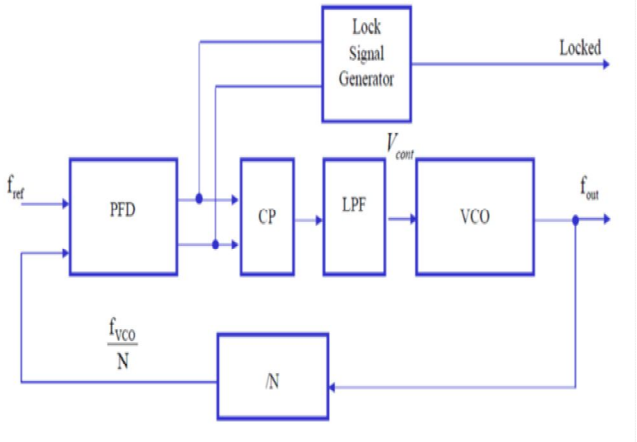

Fig. 1 Phase-Locked Loop with Lock Signal Generator

III. CIRCUIT DESIGN METHOD

In this paper, I have determined the design of CPLL through schemes of PFD, CP, LP, VCO, Divider (N=16) and finally, LSG to get the result of the whole project goal. Again, I utilized the principle of Schmidt trigger to way out LSG behaviour on the basis of combine circuits output and consequently, whether the PLL is locked or not I can determined from the results.

A. Phase Frequency Detector (PFD) Circuit Design

I have designed our PFD using NAND and NOT gate. Our simulated values are listed below-
For NAND Gate: Wp=15.98 µm, Wn= 5.33 µm and L=0.4 µm
For Inverter: Wp= 5.10 µm, Wn= 1.70 µm and L= 0.4 µm

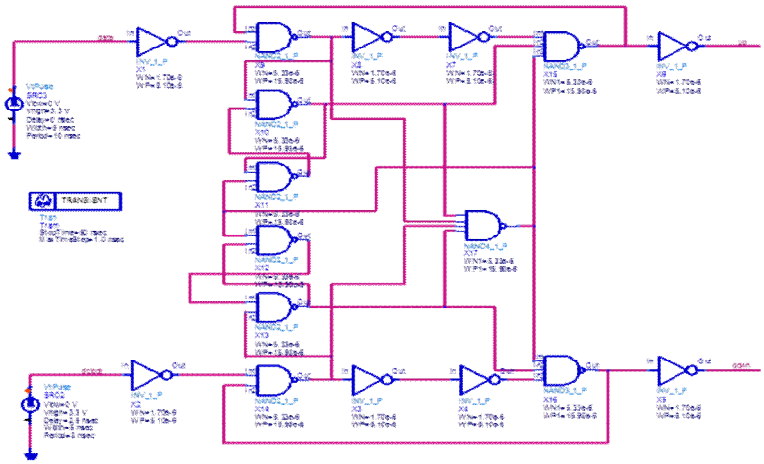

Fig.2 Proposed Schematic of PFD

B. Charge-Pump Circuit Design

I have designed our Charge-Pump with Current mirror circuit. Current mirror is a circuit that sources (or sinks) a constant current [2]:

1) Calculation: The useful equations used for calculating the transistors parameter are described below:

$$\text{For PMOS, } I_{REF} = \frac{KP_P}{2}\frac{WP}{L}(V_{GS} - |V_{THP}|)^2 \qquad (3.1)$$

For NMOS, $I_{REF} = \frac{KP_N}{2}\frac{WN}{L}(V_{GS} - |V_{THN}|)^2$ (3.2)

Here, $I_{REF} = 15\mu A$ and $V_{GS} - |V_{THP}| = 0.3\ V$

2) *Assumption:* I assumed that the channel-length modulation of transistors is zero (0). Our calculated value for Transistors are shown below
on Table I-

TABLE I
TRANSISTORS PARAMETERS OF CHARGE PUMP

Mirror Transistor Length, L_{ana}	1 µm
Mirror Transistor Width of PMOS, WPA	4.74 µm
Mirror Transistor Width of NMOS, WNA	1.74 µm
Switching Transistor Length, L_{dig}	0.4 µm
Switching Transistor Width of PMOS, WP	0.6 µm
Switching Transistor Width of NMOS, WN	0.5 µm

The proposed charge pump circuit is also shown below on Fig. 3

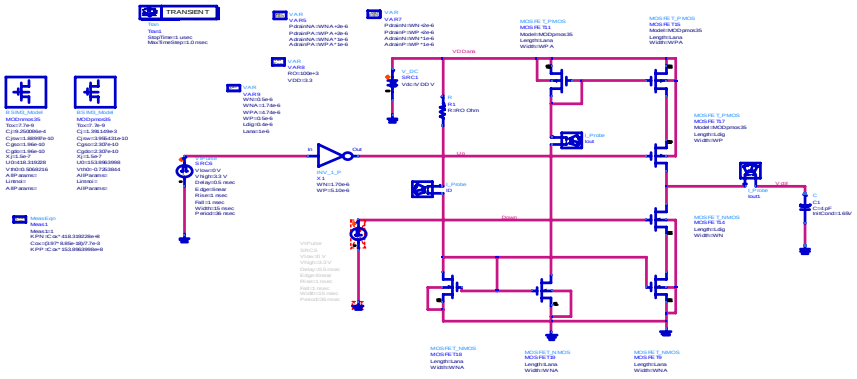

Fig. 3 Schematic of Charge Pump Circuit

C. Loop Filter Circuit Design

Loop filter is called brain of PLL [2]. It keeps the PLL from oscillating. So, Loop filter should be designed correctly.

1) Calculation

Input frequency or Reference frequency of PLL:

$$f_{in} = f_{REF} = f_{out}/N$$

$f_{out} = 450\,MHz$ and N = 16

$$f_{in} = f_{REF} = 28.125\,MHz$$

Natural frequency, $\omega_n = \left(\frac{f_{REF}}{10}\right) \times 2\pi = 2.8125 \times 2\pi$ Mrad

Capacitance, $Cs = \left(\frac{I_{cp}}{2\pi}\right) \times \left(\frac{K_{VCO}}{N}\right) \times \left(\frac{1}{\omega_n^2}\right)$

Here, $I_{cp} = 15\,\mu A$

$$K_{VCO} = (9.1934 \times 2\pi)\frac{Mrad}{VS}$$

$\therefore \boldsymbol{Cs} = 441.64\ \boldsymbol{fF}$

Again, Capacitance, $Cp = \frac{Cs}{10}$ $\quad \therefore \boldsymbol{Cp} = 44.164\ \boldsymbol{fF}$

Resistance, $R = \frac{2 \times \zeta}{\omega_n \times Cs}$

Here, Damping Factor, ζ =0.707

$\therefore \boldsymbol{R} = 181.117\ \boldsymbol{k}\ \Omega$

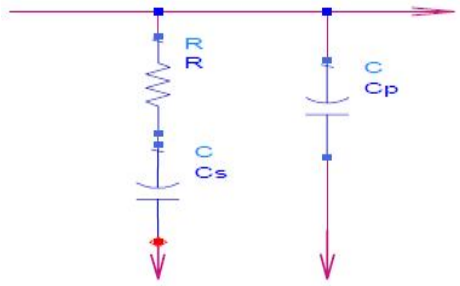

Fig. 4 Schematic of Charge Pump Circuit

D. VCO Circuit Design

Useful Equations for VCO Design:

Drain current when the transistor is in saturation

$$\text{For PMOS, } I_{DP} = \frac{KP_P}{2}\frac{WP}{L}(V_{GS} - |V_{THP}|)^2 \quad (3.3)$$

$$\text{For NMOS, } I_{DN} = (KP_N)/2WN/L(V_GS - |V_THN|)^2 \quad (3.4)$$

$$\text{Gain of the VCO, } K_{VCO} = 2\pi\frac{(f_{max} - f_{min})}{(V_{max} - V_{min})} = \frac{(\omega_{max} - \omega_{min})}{(V_{max} - V_{min})} radinas/Vs \quad (3.5)$$

$$\text{Oscillation Frequency, } f_{OSC} = \frac{I_D}{N}\frac{1}{V_{DD}}\frac{1}{10C_{ox}LW_N} \quad (3.6)$$

The following assumptions have been taken into consideration for VCO Design

I am also considering the following assumptions for the VCO design-

1) All currents through all branches are equal

2) Center frequency occurs when the control voltage, $V_{ctr} = \frac{V_{DD}}{2}$

3) Taking only oxide capacitance, Cox and neglecting other capacitance of the MOSFETs

Process Parameter for VCO:

Oscillation Frequency, f_{osc}= 450 MHz

Length, L= 0.35 µm
Number of stage, N= 9
Threshold Voltage for NMOS, V_{THN} = 0.5 V
Threshold Voltage for PMOS, V_{THP}=0.7 V
KPN = 190 µA/V^2
KPP = 70 µA/V^2
Cox = 4.563 fF/μm^2
VDD = 3.3 V
ID= 360 µA
Calculation for Inverter & Current Source MOSFET:
Design of Inverter:Using equation 3.6, I have calculated the value of WN and then calculated WP considering the equal driving capacity for Both PMOS and NMOS, i.e. WP = 3WN.

Finally I get, WN $\frac{360\times10^{-6}}{(450\times10^{6})\times9\times3.3\times(4.563\times10^{-3})\times(0.35\times10^{-6})}\approx1.70$ µm

So, WP = 3×1.70 = 5.10 µm

Design of Current Source

For designing the curret source, I have used the equation 3.4, $I_{DN} = \frac{KP_N}{2}\frac{WN}{L}(V_{GS}-|V_{THN}|)^2$

Finally I get, WN= $\frac{2\times360\times10^{-6}\times0.35\times10^{-6}}{(1.90789\times10^{-4})\times(0.5)^2}\approx5.33$ µm

So, WP = 3×5.33 = 15.98 µm
Schematic Diagram for VCO with hand calculated value:

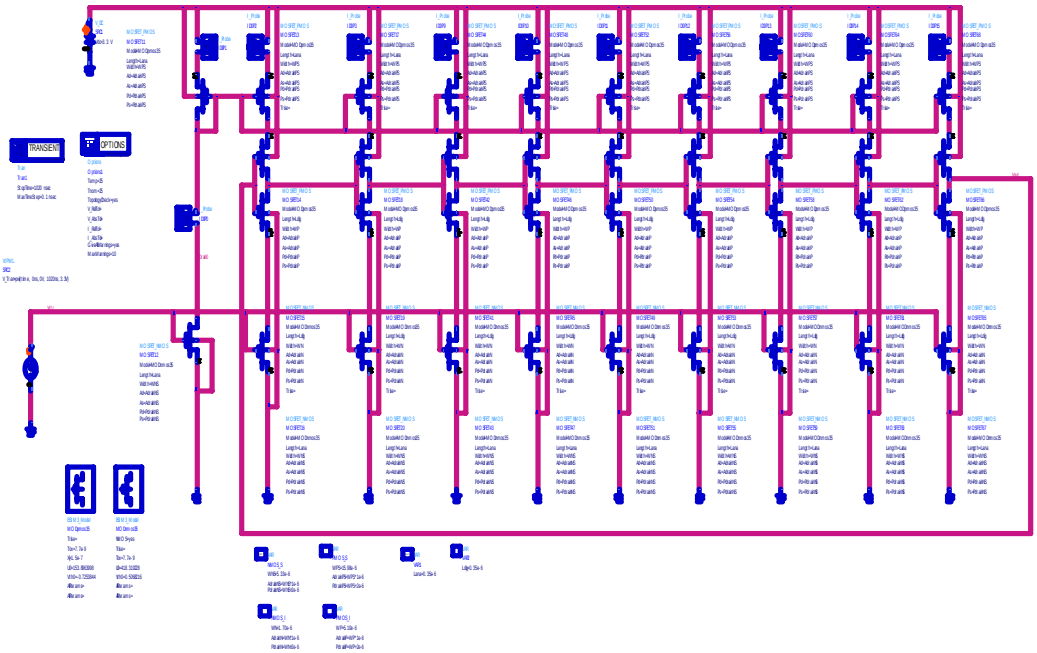

Fig. 5 Schematic Diagram for VCO with N=9

E. Divider Circuit Design

I have designed the Divider circuit as shown in Fig. 6 with Edge triggered D-FF. The designed divider circuit will divide the output frequency of VCO by 16. In our divider circuit four Edge triggered D-FF are used. One output from each D-FF is feed to another D-FF Clock. Another output of D-FF is feed back to the input of each D-FF. Each block of D-FF divides the frequency by 2.

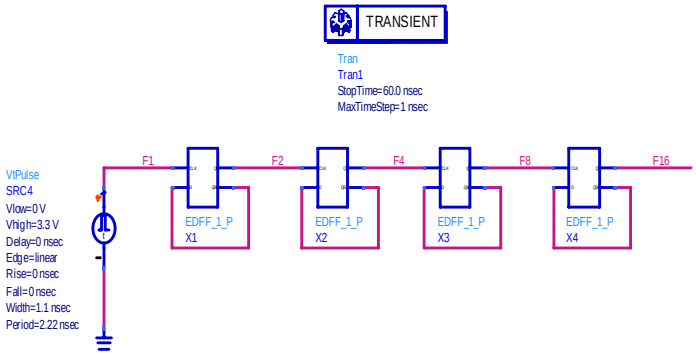

Fig. 6 Schematic of Frequency Divider (N=16)

F. Edge Triggered D-FF Design

Parameter used in Edge Triggered D-FF:

For NAND gate Width of PMOS, Wp= 15.98 um, Width of NMOS, Wn= 5.33 um

For Inverter Width of PMOS, Wp=1.70 um, Width of NMOS, Wn=5.10 um

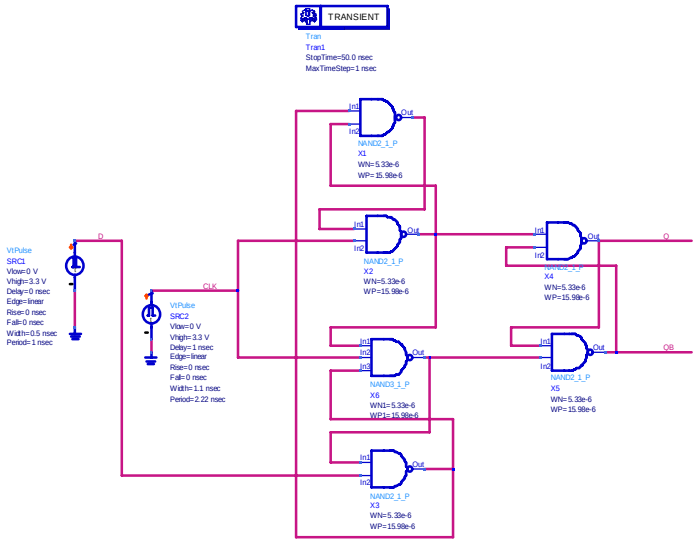

Fig. 7 Schematic of Edge Triggered D-FF

G. Phase Locked Loop (PLL) Circuit Design

The Input Frequency or Reference Frequency of our PLL is 28.125 MHz. Figure below shows the block diagram of our PLL. Fig. 8 shows the block diagram of PLL. First component of the PLL is Phase Frequency Detector (PFD). PFD is feed through two input signals. One is treated as Reference frequency and other one is feedback from VCO output. The frequencies of the two signals are same but phase of the two signals are different. The UP output of PFD goes high when the reference signal leads the signal which is feedback from VCO output. Again the DOWN output goes high when the signal that is feedback from VCO leads the reference signal. The out of the PFD is feed to the second component of PLL which is known as Charge Pump. The charge pump circuit combined the two outputs from the PFD into single output to drive the Loop Filter. The Loop filter is known as brain of the PLL. Loop Filter controls the voltage to drive the VCO. It supplies a constant voltage known as “control voltage” to the VCO. Then the VCO oscillate at a certain frequency.

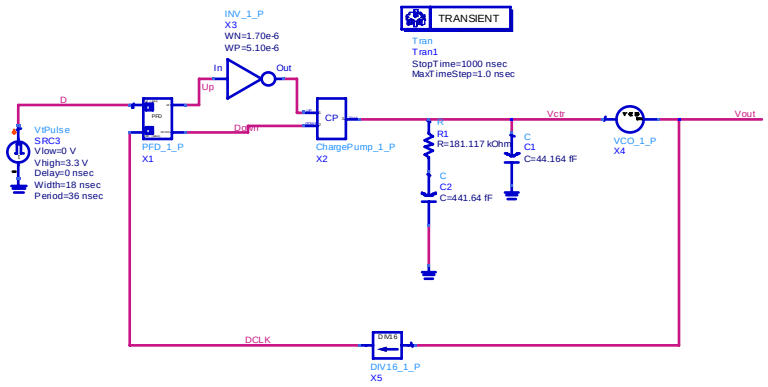

Fig. 8 Block Diagram of PLL

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H. Circuit Design of Lock Signal Generator

Lock Signal Generator circuit determines whether the PLL is locked or not. I have designed a Lock Signal Generator circuit with Schmitt trigger. Schmitt trigger is circuit that is useful to generate clean pulse from a noisy input signal [2].

Parameter used to design Schmitt Trigger:

Width of PMOS WP= 5.10 um and Width of NMOS, WN= 1.70 um

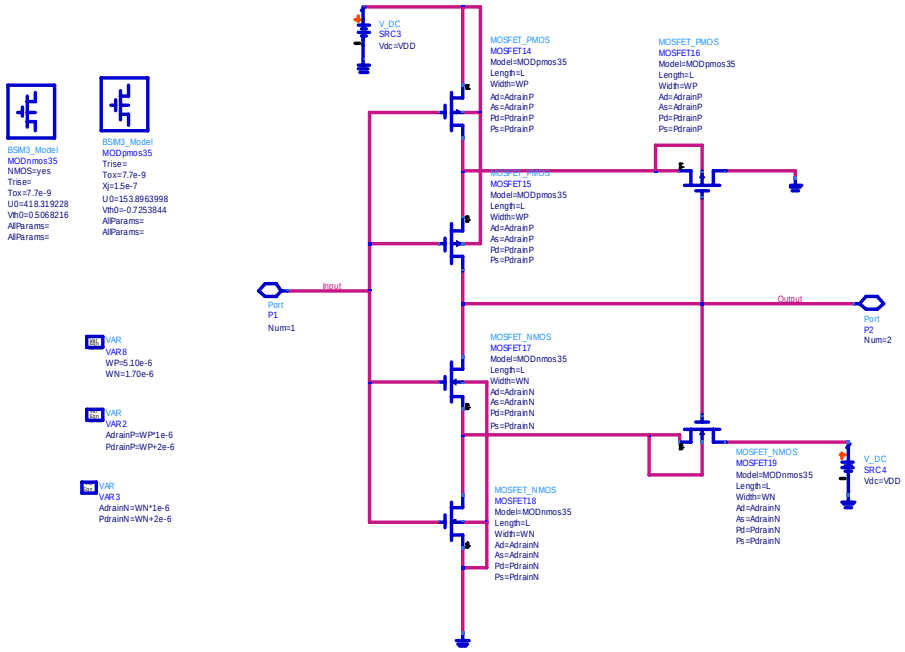

Fig. 9 Schematic of Schmitt Trigger

Fig. 9 shows the Schematic of Schmitt trigger circuit. We can divide the circuit into two parts, depending on whether the output is high or low. If the output is low, then the MOSFET 16 (upper most MOSFET of the circuit on right side) is on and MOSFET19 is off (lower most MOSFET of the circuit on right side) and we are concerned with the P-channel portion when calculating the switching point voltages, while if the output is high, MOSFET19 is on (lower most MOSFET of the circuit on right side) and the MOSFET 16 (upper most MOSFET of the circuit on right side) is off and we are concerned with the n-channel portion. Also, if the output is high, MOSFET14 and MOSFET15 (Upper most MOSFETs of the circuit on left side) are on, providing a DC path to VDD [2].

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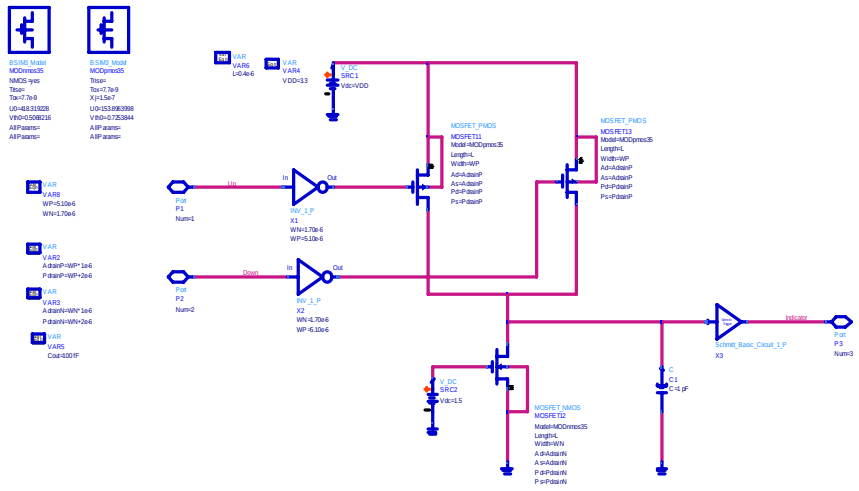


Fig. 10 Schematic of Lock signal Generator

I. PLL with Lock Signal Generator

Finally, the block diagram of PLL with the Lock Signal Generator is shown below in Fig. 11:

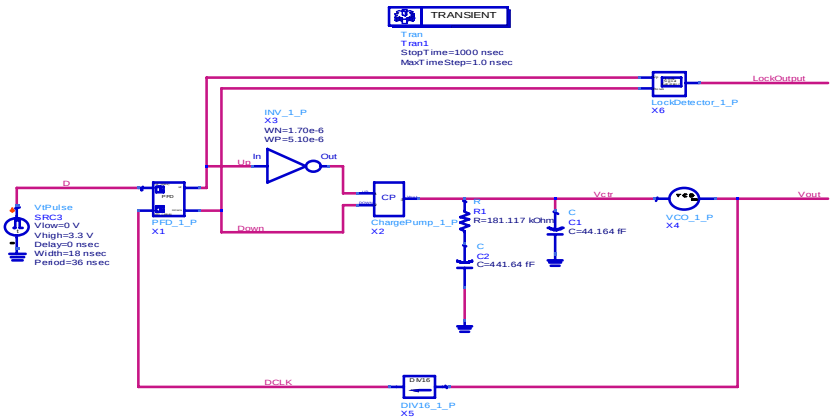


Fig. 11 Circuit Diagram of PLL with Lock signal Generator

IV. SIMULATION RESULT

Finally, the Fig. 12 shows the overall output of PLL circuit and the lock signal generator. First two graph of the figure below shows the Reference Signal (D, V) and Feedback signal (DCLK) from VCO. These two signals have same frequency with different phase. These two signals are feed to the PFD. The two graphs UP and Down (bellow the graphs of input signals) show the output of PFD. These two graphs show the UP output of PFD goes high when the reference signal leads the signal which is feedback from VCO output. Again, the DOWN output goes high when the signal that is feedback from VCO leads the reference signal. These two outputs from PFD are combined to one output by charge-pump circuit to drive the Loop Filter. Then the loop filter controls the voltage to drive the VCO. The graph 'Vctr' of the above figure shows the output of loop filters which is treated as control voltage. This control voltage is used to drive the VCO and the VCO oscillate at a certain frequency. The graph 'Vout' shows the output of VCO. The last graph 'LockOutput' shows the output of lock signal generator which determines whether the PLL is locked or not. From this graph we can see that the output of Lock Signal Generator is at constant voltage level which implies our PLL is locked.

The following parameter has been used in the simulation

Reference Frequency=28.125 MHz, Pulse Width=18 nsec, Period=36 nsec, Delay=0 nsec

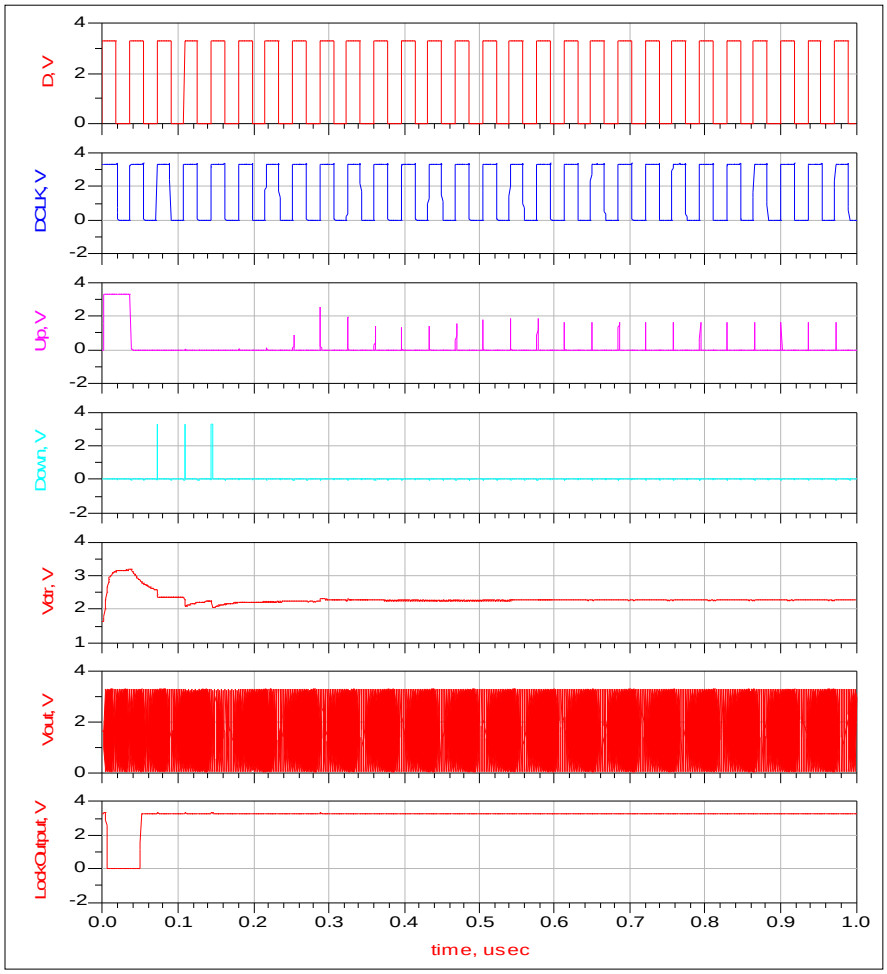


Fig. 12 Overall output of PLL with lock signal generator

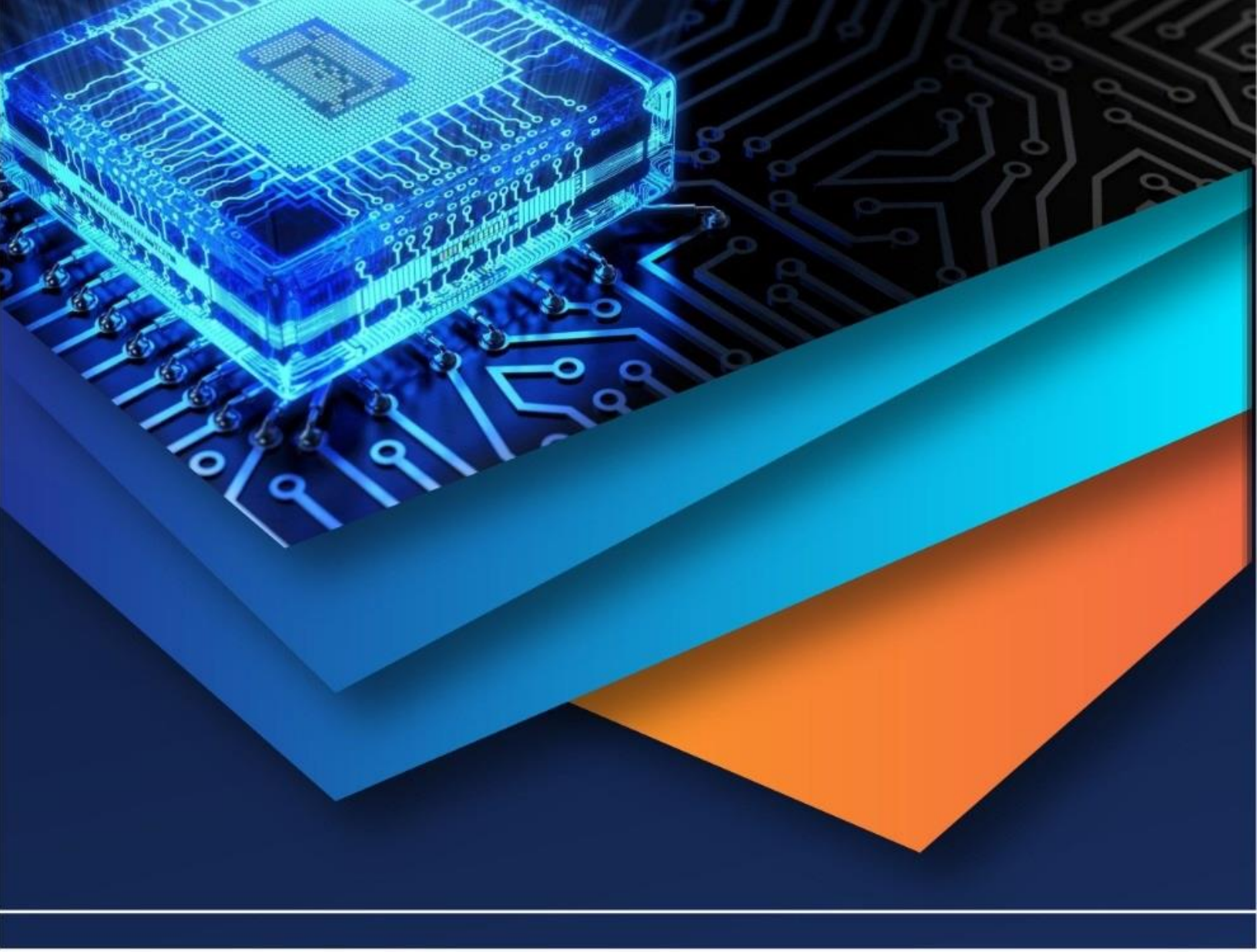
Here, we found that our each block was functioning well individually. After the combination of all block we found that it was working in a well manner, although there were some challenging issues while working with the PLL.

V. CONCLUSIONS

The designing of a PLL is a challenging work. As PLL is a combination of several blocks. So, without optimizing the individual block, it is really tough to expect a quite good result. VCO plays the main role in PLL so by ensuring a stable or constant input voltage to the VCO- we can expect a phase locked condition. Several parameters like Reference current, Width of the transistor and number of stages were optimized for better result. As usual by using trial and error method was performed to ensure expected result. Another critical aspect in the design was the Phase Frequency Detector (PFD). At first our PFD was not working well with the condition when up is active, but it was optimized by putting different values for the inverter.The proper functioning of PLL is solely depends upon the calculation & optimization of each block. We tried to make all the basic functions working in a well manner. Each block of the PLL such as VCO, PFD, Divider, CP and Loop filter have been verified individually and output results were slightly deviated from the ideal condition because while doing the hand calculation, parasitic capacitances of the MOSFETs were totally ignored. But in the simulation, all the parasitic effects were included in the MOSFET model. That is why calculated value of Charge Pump and VCO current are little bit different from ADS simulation result. But overall the project was done in a well manner.

REFERENCES

[1] Donald R. Stephens , "The Early History of Phase-Locked Loops", August 22, 2017[online]. Available: http://www.globalspec.com/reference/38384/ 203279/ chapter-1-the-early-history-of-phase-locked-loops.
[2] R. Jacob Baker, "CMOS- Circuit Design, Layout and Simulation", 3rd Edition, Published in IEEE Press, ISBN 978-0-470-88132-3.
[3] Voltage Controlled oscillator, October 16, 2017 [online]. Available: http://www.electronics-
[4] manufacturers.com/info/electronic-components/voltage-controlled-oscillator-vco.html
[5] R. Bertrand, "The Basics of PLL Frequency Synthesis", September 23, 2017[online]. Available:
[6] http://www.nsarc.ca/hf/pll.pdf.



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