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# A Shared Multiplier for Effectual Area of 1024 Point Fast Fourier Transform Processor

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**Abstract:** *This paper proposes A Shared Multiplier for Effectual Area of 1024 Point Fast Fourier Transform Processor. This processor utilizes 28% of complex multipliers with reduced area. These processors have flexibility of different Fast Fourier Transform sizes (2, 4,8,16,3,64,128,256 and 512) of length, So that the hardware complexity reduced. The proposed mixed radix butterfly units can be designed in MATLAB SIMULINK. This processors verified by XILINX HDL tool modified with VERILOG language and implemented in 45-nm CMOS technology. The synthesis results shows that area reduce by 19% and achieve a high throughput rate up to 27.5GS/s at 530 MHz In addition, the processor can support for any FFT sizes by addition of stages and works for inverse Fast Fourier Transform by simply taking conjugation of Fast Fourier Transform.*

**Keywords:** *Fast Fourier Transform (FFT), Mixed Radix Multipath Delay Commutator (MRMDC), Butterfly Unit (BU).*

## I. INTRODUCTION

FFT is an important part in OFDM systems. OFDM has been used as a leading modulation technique for wireless and wire line communication standards, such as IEEE 802.11n/ac/ad [1], IEEE 802.15.3.C [2], DAB [3], ultrawide-band UWB [4], and optical OFDM [5][6]. High speed OFDM systems such as wireless personal area networks (WPANS [2], UWB [4] and O-OFDM [5],[6] require high speed FFT computations to meet higher data rates. The FFT Computation of real input samples be in 1-4, gives the symmetry property

of FFT to reduce the computational complexities in different area of applications like medical in electrocardiography [5].

The FFT processors proposed with real time processing requirements and less hardware complexity [9]-[11]. To achieve less area, memory based architectures [11]-[14] like application-specific instruction set processors meet the computation of FFT but they cannot reach high-speed requirements. For high throughput rate, There are many pipelined architectures proposed [14]-[16]. Pipelined architectures are divided into single path delay commutator [14], single path feedback [15],[16], multipath delay feedback or commutator [12]-[14].

The MDC architectures [13]-[15] are a high throughput and used multiple data paths to maintain easy synchronization control. The radix -4 MDC architectures improve the area by reducing of complex multipliers from three to one in each stage. To perform twiddle factor multiplications in one stage leads one clock cycle, another multiplication needs one more clock cycle faster than the system [13]. Therefore, the architecture in [13] may not use as high speed applications. To get high throughput rate, FFT architectures using folding transformations [14], [15] have proposed.

For high speed applications, processors requires a through put rate of over 2 GS/s, radix-8 or radix-16 algorithms are used [18]. Normally, the FFT size is a power of two, for typical like 128, 256, 512 and 1024 FFT sizes are not powers of eight. That is radix-8 algorithms cannot handle these FFT sizes. To provide these requirements, the proposed 1024 FFT processor meets the OFDM requirements by using mixed

Radix algorithm. Therefore the proposed processors can perform FFT computations for sizes of not powers of eight.

A brief interpretation on the 128/256, 256/512-point MRMDC pipelined FFT processors [17], [18] with eight parallel data paths can operate on high clock frequency. To maintain the demands of OFDM systems, three types MRMDC architectures are proposed [17]. shared multiplier of 1024 -point eight parallel MRMDC FFT processor have Type 1 reduces the number of butterfly units (BU's in the first stage. Type 2 proposes the shared multiplier of 1024 processor can reduce the complex multipliers for radix-8 BU's in the second stage. Type 3 combines both the Type 1 and Type 2 can reduce the number of BU's and complex multipliers.

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**II. MIXED - RADIX FFT ALGORITHM**

The N-point discrete fourier transform (DFT) is defined as  $X(k) = \sum x(n) W_N^{nk}$ ,  $k=0,1,2,\dots,N-1; n=0,1,2,\dots,N-1$ ; (1)

Where  $x(n)$  is the input sequence  $X(k)$  is the output sequence, and  $N$  is the transform length.  $W_N^{nk}$  denotes the  $N$ th primitive root of unity, with its exponent evaluated modulo  $N$  and is expressed as

$$W_N^{nk} = e^{-j(2\pi nk/N)} = \cos(2\pi nk/N) - j \sin(2\pi nk/N). \quad (2)$$

When the FFT size is not a power of radix  $r$ , then mixed radix algorithm should be used.

For example if

$$N=256$$

$$n = 64n_1 + n_2, \quad 0 \leq n_1 \leq 4, 0 \leq n_2 \leq 63$$

$$k = k_1 + 4k_2, \quad 0 \leq k_1 \leq 4, 0 \leq k_2 \leq 63 \quad (3)$$

Substituting (3) in (1)

$$X(k) = X(k_1 + 4k_2) \quad (4)$$

$$= \sum x(64n_1 + n_2) W_{256}^{(64n_1 + n_2)(k_1 + 4k_2)}, \quad 0 \leq n_1 < 4; 0 \leq n_2 < 64$$

$$= \sum \{BF_4(n_2, k_1)\} W_{64}^{n_2 k_2}; \quad n_2 = 0, 1, \dots, 63. \quad (5)$$

The 256 point mixed radix FFT algorithm can be derived from (4) by decomposing the remaining 64-point DFT into 8-point DFT twice.

The MRMDC architecture is explained using 128/256-point MRMDC FFT/IFFT processor [19]. The architecture consists of BU's, delay commutators, and twiddle factor multipliers. In the first stage, the radix-2/4 BU can perform one radix-4 or two radix-2 operations to compute the 128 and 256-point FFTs. There are three stages based on radix-2, radix-4, and radix-8 algorithms. The input sequence of single path is divided into eight data paths.

**III. EXISTING 128-POINT MRMDC FFT/IFFT PROCESSOR**

The proposed FFT processor can support the 128-point FFT/IFFT in a similar manner to compute the 256-point FFT described in Section. As shown in Fig. 1, the proposed structure reduces the number of BUs from two to one in the first stage compared with the existing structure in Fig. 2. In Fig. 2, the input sequence of each data path is split into four data streams, and it takes 12 cycles using D4, D8, and D12 to start the first butterfly computation and four cycles to perform the radix-2/4 operations. To finish the radix-2 computation using one radix-2/4 BU, the proposed structure requires four cycles. Therefore, the first stage of the proposed processor also requires 16 cycles, even with one radix-2/4 BU. Thus, the structure consisting of one radix-2/4 BU in the first stage can reduce the hardware complexity without increasing the number of clock cycles compared with the existing architecture.

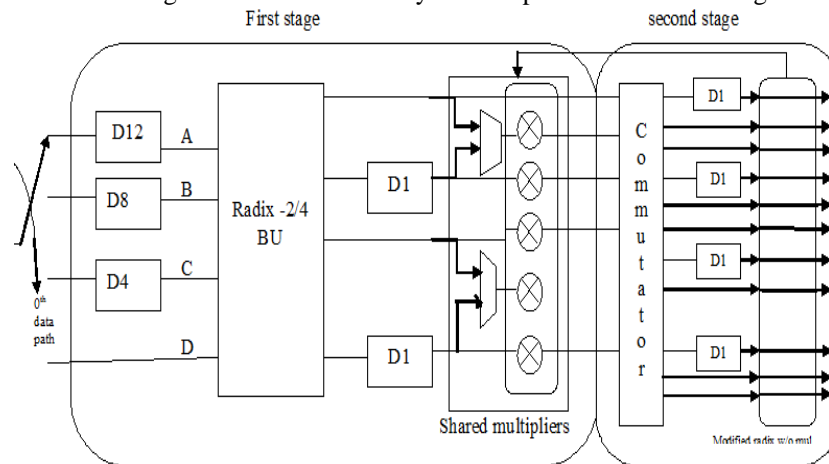
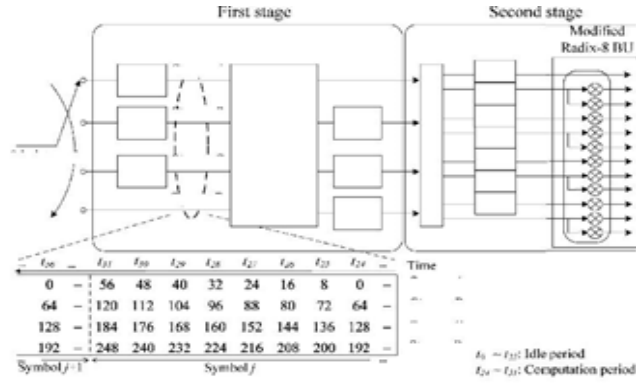
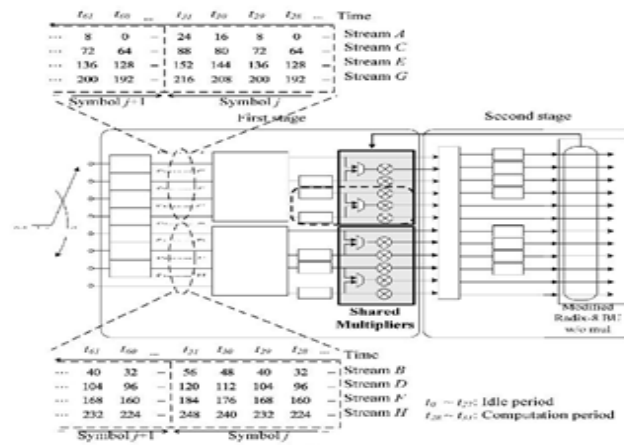


Fig 1: SMSS based 128/256 point FFT Processor

In the first stage in Fig. 2(a), the radix-2/4 BU can perform two radix-2 butterfly computations. The proposed structure performs complex multiplications for the second stage before the delay commutator using the shared multipliers. The Commutator is configured by the operation mode. In the 128-point FFT, the operation mode number is calculated by  $t$  modulo four. The commutator operates in four different operation modes for performing the 128-point FFT.

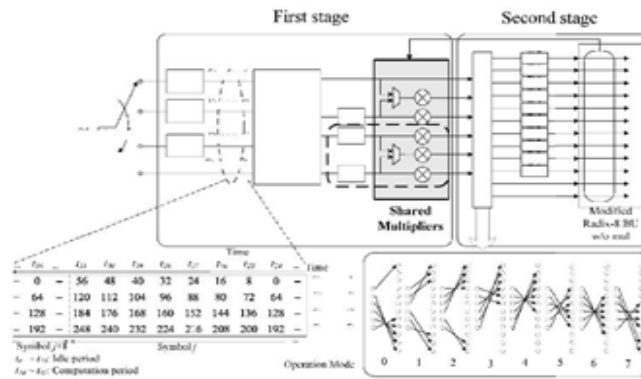


(a)



(b)

Fig. 3 shows the proposed first stage in the dotted box shown in Fig. 1, which consists of the input buffer, butterfly Processing element, and commutator. In the first stage, the input sequence of each data path is divided into four data streams (A, B, C, and D), which are delayed by the delay elements to synchronize proper cycles. The butterfly operations in the first stage are performed by four data streams. The output data of the first stage are delivered to the second stage through the delay elements and the delay commutator by the operation modes.



(c)

Fig 2: Existing first stage of the zeroth data-path for the 256-point FFT

- A. Reducing the number of butterflies (Type I)
- B. Reducing the number of complex multipliers (Type II)
- C. Architecture employing the scheduling scheme (Type III)

The FFT size determines the delay cycle of each delay element and the butterfly operation of the first stage. Moreover, the switching of the multiplexers, MUX1, MUX2, and MUX3, depends on the FFT size regardless of whether the data on the same path are to be delayed or not. The control signals of the delay elements vary with the FFT size, and each delay element has different operation modes depending on the FFT size.

**D. Second and Third Stage Structure**

The input data multiplied by the appropriate twiddle factors are fed into the second stage for the radix-8 butterfly operation through the delay commutator, as shown in Fig. 2. In the second stage, the remaining radix-8 calculation without multiplications is performed because all the multipliers of the second stage in the existing one are moved to the shared multipliers in the proposed first stage. A suitable structure is required to ensure the correction of the FFT output data because the third stage in Fig. 1 is different from the second stage. All the output data generated by the radix-8 butterfly in the second stage are fed to the third stage by a specific order

$$in_3(p,l) = out_2(l, p) \tag{6}$$

Where  $in_3$  and  $out_2$  represent the input data of the third stage and the output data of the second stage, respectively.

In (13),  $p$  and  $l$  represent  $p = 0, 1 \dots P-1$  and  $l = 0, 1 \dots L-1$ , respectively.

$P$  is the number of parallel data paths and  $L$  is the number of outputs from a parallel data path.

The proposed processor has the eight-parallel paths, and each path has eight- parallel data streams (A,...,H). The radix-8 BU operates in the third stage using the input sequence from the second stage based on (4). In the existing architecture, the second stage consists of the radix-8 BU in [16] that requires 11 complex multipliers. The third stage using the radix-8 BU also requires 11 complex multipliers. Therefore, the existing architecture requires a total of 22 complex multipliers. In contrast, the proposed architecture requires five multipliers

And 11 multipliers in the first stage and the third stage, respectively. Therefore, the proposed architecture in Fig. 2(c) has 16 multipliers, while the existing architecture requires 22 multipliers for each data path. The proposed MRMDC in Fig. 1 has a total of 128 ( $16 \times 8$ ) multipliers because the processors have eight- parallel data paths, whereas the existing architecture requires 176 ( $22 \times 8$ ) multipliers.

**IV. PROPOSED 1024 POINT FFT PROCESSOR**

This subsection presents the proposed MRMDC 1024-point FFT processor. Fig. 3 shows the proposed processor that consists of four stages. The radix-2 BUs in the first stage are added to support the 512-point FFT compared with that shown in Fig. 1. The second, third, and fourth stages are the same, as shown in Fig. 1. The processor shown in Fig. 4 performs the 1024-point FFT, which is similar to the 256-point FFT in Fig. 2(c). As shown in Fig. 4.

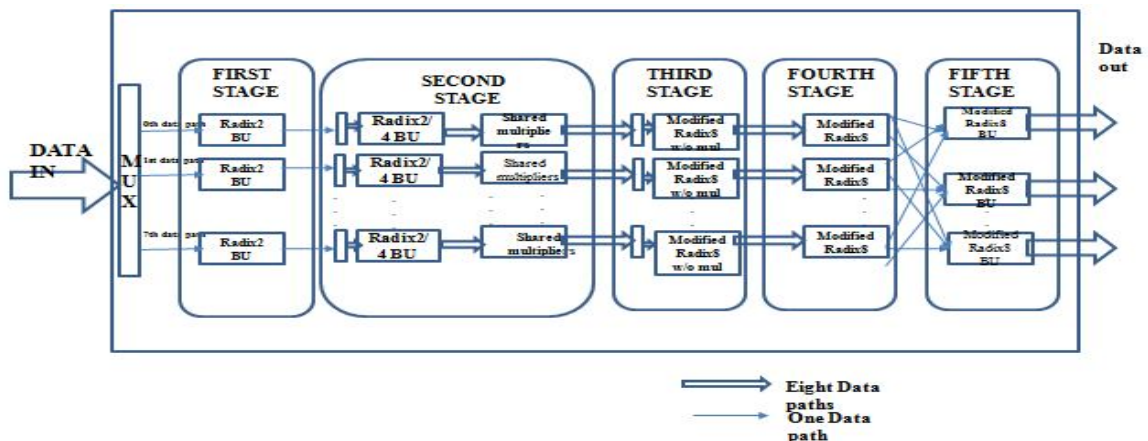


Fig 3: Block Diagram of 1024 –point FFT processor.

The input sequence is split into eight-parallel data paths that are delayed to arrange the input data order in the first stage. Fig. 10 redrawn from the dotted box in Fig. 3 shows one data path of the existing and proposed structures for the 1024-point FFT, respectively. As shown in Fig. 4, all the multipliers present in third stage are moved to the shared multipliers in the second stage as we proposed in Type III.

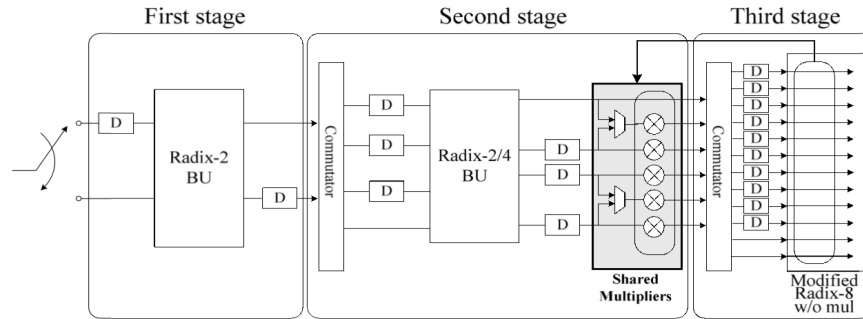


Fig 4: Structure of the proposed first and second stages of 1024 point FFT processor

The SMSS shown in Fig. 5 can also be applied to the 1024-point FFT. To perform the 1024-point FFT, the proposed structure computes twiddle factor multiplications for the second stage using the shared multipliers on each parallel data path. By employing SMSS, the proposed processor can support both the 256- and 512-point FFTs. In addition, the proposed MRMDC can be applied to larger-size FFTs, such 2048, and 4096, using additional stages. For example, the 2048-point FFT processor consists of one radix-4 BU, the shared multipliers, one radix-8 BU without multipliers, and two radix-8 BUs.

### V. RESULTS

The multiplexer, radix 2, and radix 2/4 and modified radix-8BU can be designed in MATLAB Simulink as shown in figures 4,5 and 6.

The first and second stage of the 1024 Point FFT processor is modeled in Verilog with RTL diagram as shown in Fig 9. then that processor operated in the cadence 45 nm technology to perform with high speed compared previous methods in [16],[17]. The processor have the form of physical design as shown in fig 11.

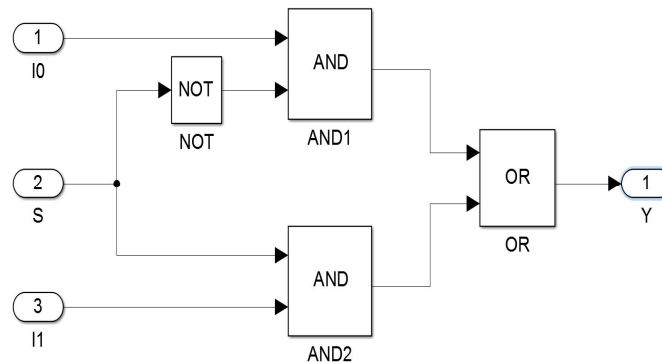


Fig 5: Multiplexer 2:1

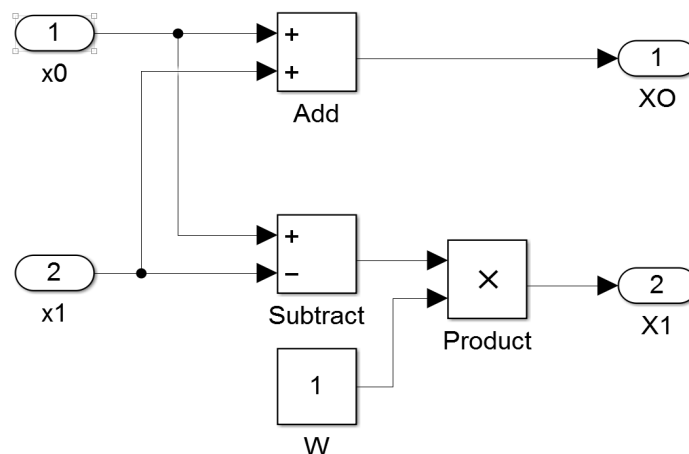


Fig 6: Radix-2 BU

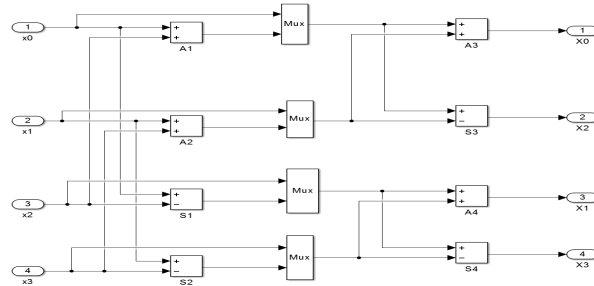


Fig 7: Radix-2/4 BU.

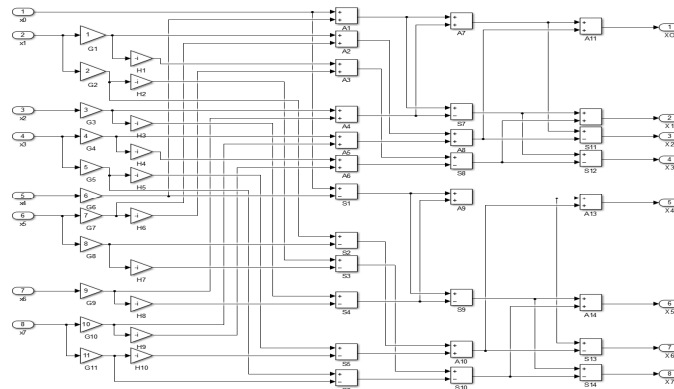


Fig 8: Modified Radix-8 BU.

The proposed SMSS based FFT/IFFT processor using Shared multiplier is designed using Xilinx ISE14.2 tool and modeled in Verilog HDL. The proposed FFT processors use shared multiplier to improve computation speed. The synthesis result shows the area efficiency of propose processor and computation speed improvement. The proposed processor is simulated using Xilinx ISim simulator. The Radix Butterflies of processor is done using MATLAB Simulink Tool. SMSS based FFT/IFFT processor implemented using CADENCE 45nm technology by implementing in this technology we reduce area, delay or power.

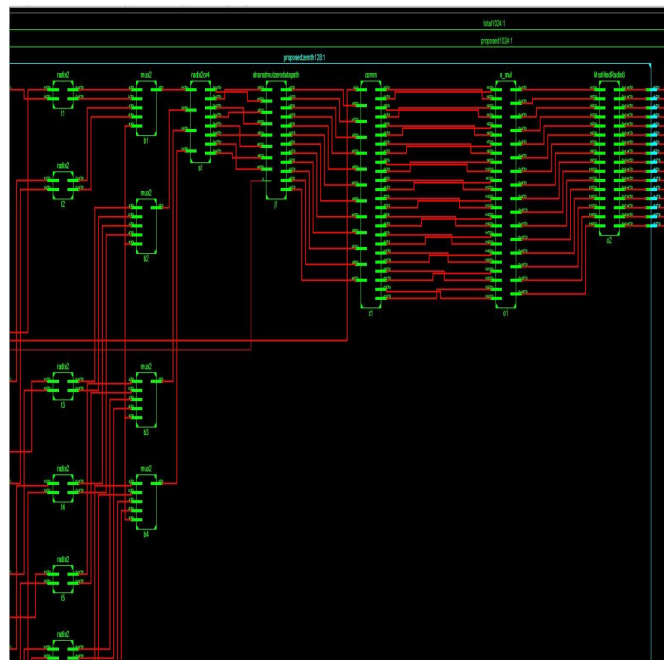


Fig 9:Proposed 1024 FFT Processor in XILINX.

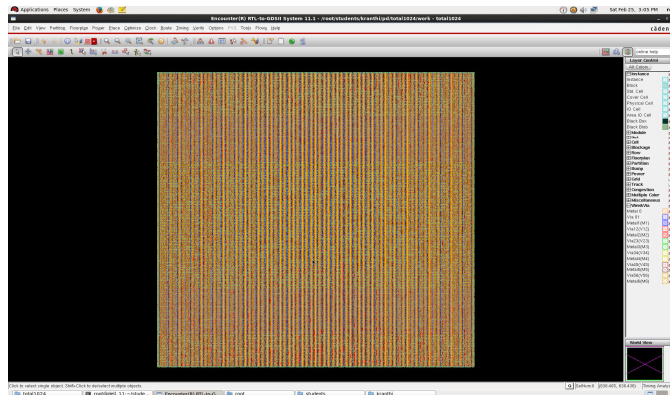


Fig 10: Physical Design of 1024 point FFT processor.

## VI. COMPARISONS

Comparison for Hardware Complexities table 1:

	EXISTING 128	EXISTING 1024	PROPOSE D 128	PROPOSE D 1024
Radix	4,8	2,4,8	4,8	2,4,8
No.of Datapaths	8	8	8	8
No.of Multipliers	224	1,792	160	1,280
No.of Adders	1,104	8,832	776	10,920

Performance Comparison Table 2:

processor	Existing128	Proposed128	Proposed 1024
Area(mm <sup>2</sup> )	11,82,099	3,56,810	20,21,796
Power(uw)	1,41,630.8	8,97,534.5	37,34,251
Timing(ns)	5.30	2.615	1.735
Clock rate (MHz)	188	382	570
Gate count	4,52,634	1,71,804	2,40,43,548
Throughput(GS/s)	1.5	3.056	4.560
TGR	0.0001856	0.0009961	0.000152

Technology Wise Comparison Table 3:

	Cadence(180nm)	Cadence(45nm)
Area(mm <sup>2</sup> )	20,21,796	5,38,660
Power(uw)	37,34,251	20,99,075
Timing(ns)	1.735	0.001

Expecting that the processor have same throughput rate i.e.  $(64 \times \text{clock rate}) = 36.48 \text{GS/s}$  at 570 MHz clock rate. The equipment multifaceted nature and calculation speed are looked at in the execution table. The equipment intricacy is contrasted and the current SMSS based 256-point FFT processor as far as ASIC outline metric door check. The proportional door mean the proposed processor is gotten from the union report of Xilinx XST apparatus. The union report of proposed processor is appeared in figure 7.3. The combination report gives gadget use rundown as far as FPGA plan metric. With a specific end goal to think about regarding door



check, the proportional entryway tally is figured in light of NAND entryways required to configuration cut registers, cut Look Up Tables (LUT's). The timing report gives the data about most extreme clock recurrence, way delay for the proposed processor.

The performance comparison is shown in above table 1. From the above data conclusion is that the proposed processor can be performance effective by applying for re-configurability feature and multiplier using optimizes the area and delay for the FFT/IFFT processor.

## VII. CONCLUSION

In this thesis report we proposed A Shared Multiplier for Effectual Area of 1024 Point Fast Fourier Transform Processor. This processor utilizes 28% of complex multipliers with reduced area. This processors have flexibility of different Fast Fourier Transform sizes (2,4,8,16,3,64,128,256 and 512) of length, So that the hardware complexity reduced. The proposed mixed radix butterfly units can be designed in MATLAB SIMULINK. This processors verified by XILINX HDL tool modified with VERILOG language and implemented in 45-nm CMOS technology. The synthesis results shows that area reduce by 19% and achieve a high throughput rate up to 27.5GS/s at 530 MHz. In addition, the processor can support for any FFT sizes by addition of stages and works for inverse fast Fourier transform by simply taking conjugation of Fast Fourier Transform.

In addition the proposed architecture can apply any FFT size greater than 256 point using additional stages.

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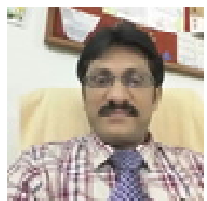
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