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Optimization of VLSI Architecture for High Performance PLL

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Abstract: ***Phase Locked Loop (PLL) plays a vital role in many modern electronics as well as communication system. Phased lock loop is a control system that generates an output signal whose phase of an input as reference signal. This compares the phase of the input signal with the phase of output oscillator which fine-tunes the frequency of its oscillator to maintain the phase matches. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Modern wireless communication systems utilize Phase Locked Loop (PLL) primarily for synchronization, clock synthesis, skew and jitter reduction. Phase locked loop finds wide application in several modern applications mostly in advance communication and instrumentation systems. PLL itself is a mixed signal circuit which has design challenge at high frequencies. The phase locked loop is designed using VLSI technology, which in turn offers high speed performance at low power. In this paper, the faster locking of the PLL is mainly concentrated by properly choosing the circuit architecture and parameters. The optimization of the VCO circuit is carried out to get a better frequency precision. The work characterizes the layout design of Phased Lock Loop PLL with multiple outputs. Effort has been made to design and implement using low power sub threshold D flip flop. The design implemented in analog design tool from Microwind 3.1 where each sub block is designed at its low power design.***

Keywords: Phase Noise, Phase Locked Loop, Frequency Synthesizer, phase frequency detector, Voltage Controller Oscillator, Charge pump

I. INTRODUCTION

A PLL is a feedback system in a closed loop that forms a fixed phase relationship between its output clock phase and the reference clock phase. A PLL is capable of tracking the phase changes that falls in the bandwidth of the phase sequence. A PLL also multiplies a low-frequency reference clock CLKref to produce a high-frequency clock CLKout which is known as clock synthesis. High component counts and multiple chips in various technologies increase the cost and form factor. A higher integration level is required to lower the cost and form factor. A closed-loop feedback system is a PLL that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL.

A circuit of PLL is a negative feedback control system. The main purpose of a PLL is to produce a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals.

The basic block diagram of the PLL is shown in the Figure-1. In general a PLL consists of four main blocks:

1) Phase Detector or Phase Frequency Detector (PD or PFD)
2) Low Pass Filter (LPF)
3) Voltage Controlled Oscillator (VCO) and
4) Divide by N Counter

PFD compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency variation, it generates two output signals “UP” and “DOWN”. The “Charge Pump” (CP) circuit is used to merge both the outputs of the PFD and give a single output. The output of the CP circuit is fed to a “Low Pass Filter” (LPF) to produce a DC control voltage.

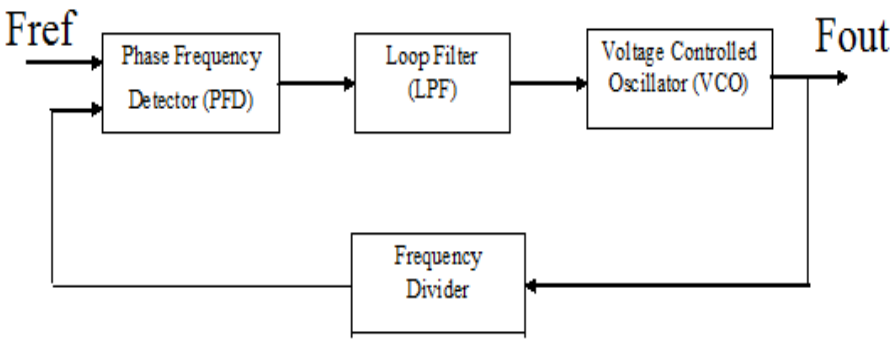

Figure-1 Basic Block diagram of PLL

The Voltage Controlled Oscillator (VCO) output of the phase and frequency depends on the generated DC control voltage. If the PFD generates an "UP" signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency[2]. On the contrary, if a "DOWN" signal is produced, the frequency of VCO output signal decreases. The output of the VCO is then supply back to the PFD in order to recalculate the phase difference, and then it form closed loop frequency control system.

II. PLL ARCHITECTURE

A PLL involves of several components. They are (1) phase or phase frequency detector, (2) charge pump, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider. The Figure-2 shows the architecture of PLL. The functioning of each block is briefly explained below.

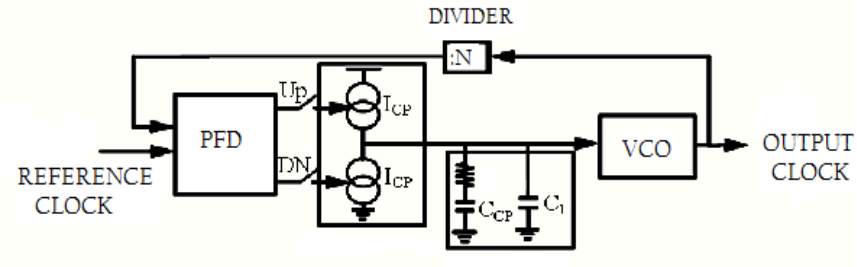

Figure-2 Architecture of PLL

A. Phase Frequency Detector

The "Phase Frequency Detector" (PFD) is a device to compare the phase of two input signals. Among the two input signals, one from a voltage controlled oscillator and another signal from external source. The phase locked loop error output is fed to a loop filter to combine the signal to smooth it. The smoothed signal is fed to a voltage controlled oscillator which produces an output signal with a frequency that is proportional to the input signal voltage. The VCO output is fed back to the PFD to form the PLL circuit.

B. Charge Pump

Charge pump circuit is an main block of the entire PLL system. It converts the phase or frequency difference data into a voltage, used to tune the VCO. Charge pump circuit is used to join both the outputs of the PFD and give a single output which is fed to the input of the filter.

C. Loop Filter

The passive low pass loop filter is used to convert back the charge pump current into the voltage. The filter must be as compressed as possible [2].The output voltage of the loop filter controls the oscillation frequency of the VCO.

D. Voltage Controlled Oscillator

The performance of the voltage controlled oscillator is of paramount importance in the PLL circuit. A Voltage controlled oscillator is an electronic oscillator whose oscillation frequency is directly related to the voltage at its input. The applied input voltage

determines the instantaneous oscillation frequency [3]. The VCO produces a signal which is send through the phase detector where the phase is been compared with the reference signal hence a difference or error voltage is produced, resulting to the phase difference between the two signals

E. Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The closed loop of the PLL circuit is formed by the frequency divider. It scales down the frequency of the VCO output signal.

III. MODEL VALIDATION

A basic phase detector is the XOR gate. It generates error pulses on both falling and rising edges. Analysis of the XOR PD is considered when the reference (ref) and feedback signals (VCO) are out of phase by zero, $\pi/2$ and respectively. The XOR Phase detector is shown in Figure-3.

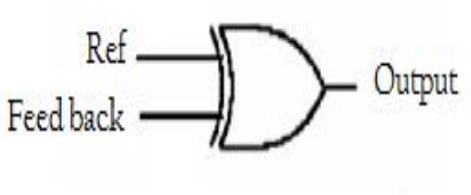

Figure-3 XOR Phase Detector

The phase difference between the two signals is zero—locked phase. The average output, Vavg, from the XOR gate is zero for this case. This phase enables us to observe the PD output for a range of phase differences [4]. However, major drawback is that harmonics of the reference signal can be locked and most importantly a difference in frequency cannot be detected.

IV. PHASE FREQUENCY DETECTOR

By considering the disadvantages, it was implemented the Phase Frequency Detector, which can detect a difference in phase and frequency between the reference and feedback signals. Also, unlike the XOR gate PD, it is free from false locking to harmonics and it responds to only rising edges of the two inputs. Furthermore, the PFD outputs either an “up” or a “down” to the CP.

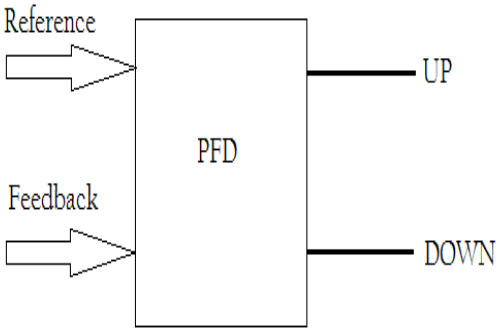

Figure-4 Basic PFD Block

The PFD design uses two flip flops with reset features as shown below in Figure-4. The reference and feedback signals are the input to the two clocks of the circuit. The D inputs are connected to VDD which always remain high. The outputs are either “UP” or “DOWN” pulses. These outputs are both connected to an AND gate to the reset of the D-FF’s. When both UP and DOWN pulses of the AND gate is high, the output will be high and which resets the flip flops. Thus, both signals cannot be high at the same time. This means that the output of the PFD is either an up or down pulse—but not both. The difference in phase is measured by the first occurrence of rising edge.

The PFD circuit shown in Figure-5 can be analyzed in two different ways—one way in which Fref leads Fin(fb) and the other in which Fin(fb) leads Fref. The term “lead” in this case represents that the signal is faster or in the lead of the other.

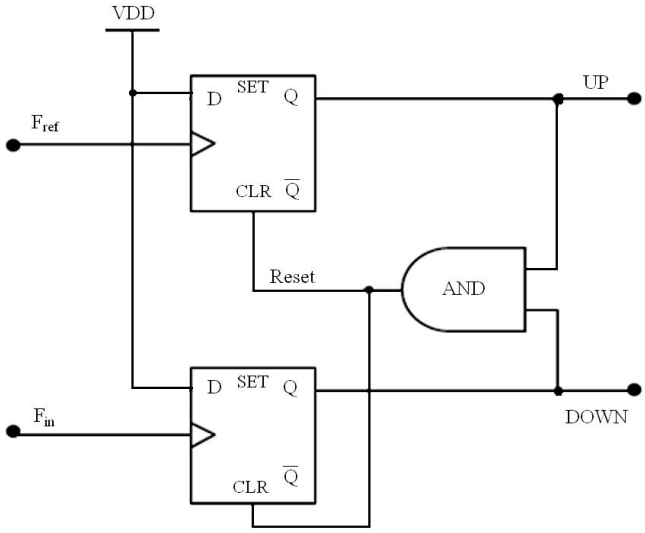

Figure-5 PFD Using Two D-Flip Flops

When fref leads fin, an UP pulse is generated. The UP pulse represents difference between the phases of the two clock signals. This UP pulse in the circuit indicates that the feedback signal needs to speed up or "catch up" with the reference signal. Ideally, the two signals must be at the similar speed or phase.
The feedback signal leads the reference signal, which generates a DN signal. This DN signal indicates in the circuit that the feedback signal is quicker than the reference signal and needs to slow down.

A. Voltage Controlled Ring Oscillator

The Voltage Controlled Ring Oscillator consists of several delay cells forming a closed loop as shown in Figure-6. The output clock frequency is determined by the delay of each delay cell which in turn is controlled by control voltage. The delay cell is usually a differential pair with a tail current and some active loading. The delay of each cell is controlled by the tail current and the tuning range is limited by the control voltage range. If the small tail current is chosen, the tail current is still not large enough even that the control voltages reach the up limit so that the high end frequency range of VCO is small. On the other hand, if the large tail current is chosen, the tail current is still large even that the control voltage reached the lower limit so that the lower end frequency range of VCO is large.

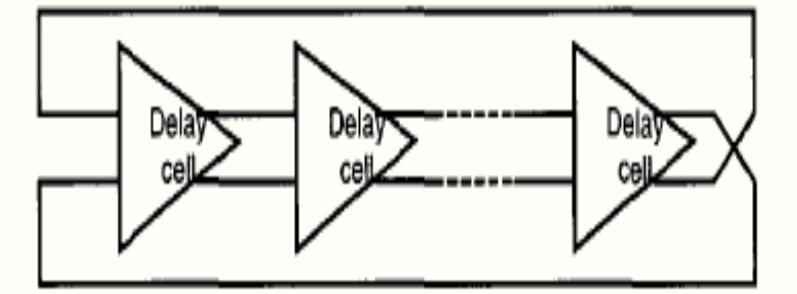

Figure-6 Ring Oscillator

In order to overcome the drawback of ring oscillator the Current-starved VCO is used because of their wide frequency range of operation, allowing for tunable designs that can easily accommodate the high-speed specifications in an RF application.
The current-starved VCO, schematically represented in Figure-7, includes two components: the input-bias stage and a ring oscillator (RO) structure designed using an odd number of current-starved inverters, where N is the number of RO stages. The input voltage, Vin VCO sets the current through the input-bias stage and current mirrors, which subsequently control the current through the current-starved inverters and control the delay of each stage. The RO oscillates at a period of (TD*2N), where TD is the delay time of an inverter stage.

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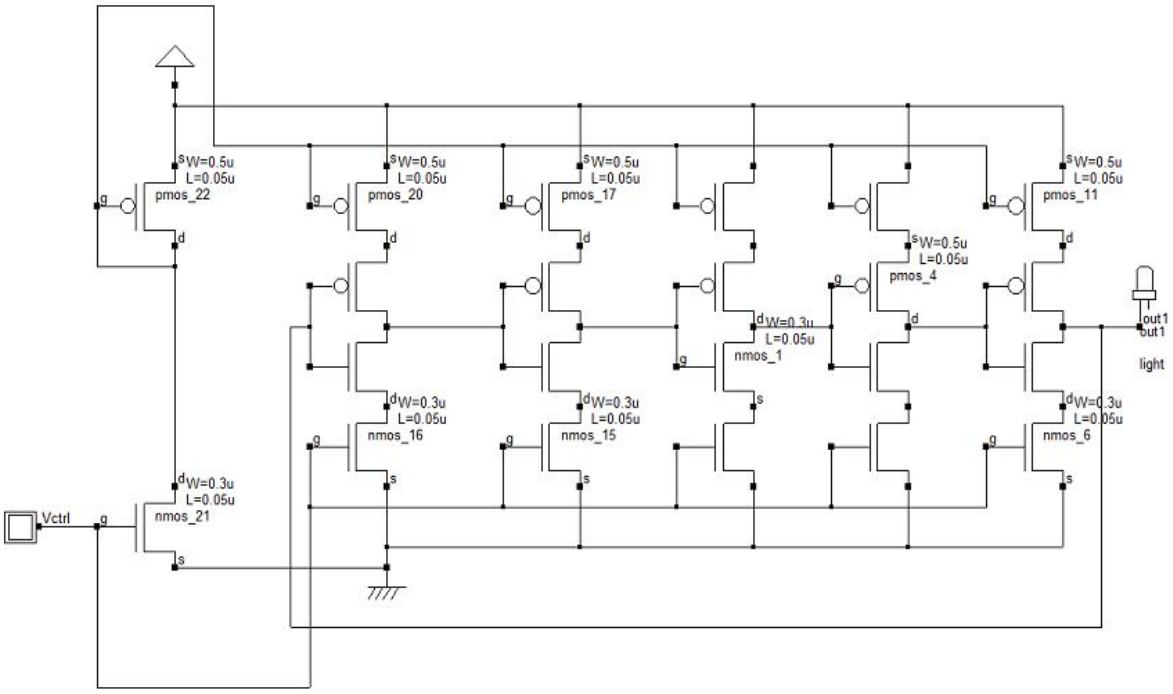

Figure-7 Current Starved VCO

B. Charge Pump

The output of the PFD should be combined into a single output for driving the loop filter. The first method is called tri-state output[5]. When both signals are low, both MOSFETs are off and the output is in a high impedance state. PMOS turns on, if the QA signal goes high and pulls the output to VDD while the output is pulled low through NMOS if the QB goes high.

According to two logical inputs, the charge pump consists of two switched current sources that pump charge into the loop filter or out of the filter. The circuit has three states[8]. If QA=0, QB=0, then both switches are off and output voltage remains constant. If QA=1, QB=0, then current through the PMOS branch charges the capacitor. On the converse, if QA=0, QB=1, then current through the PMOS branch circuit discharges the capacitor. If for example, A leads B, then QA continues to produce pulses and output rises steadily. Conversely B leads A, then QB continues to produce pulses and output falls steadily[10]. The currents through the PMOS branch and NMOS branch are nominally equal.

The loop filter is the brain of PLL is shown in Figure-8. If the loop filter values are not selected correctly, it may take the loop too long to lock, or once locked small variations in the input data may cause the loop to unlock. The group of PFD, CP, LP and VCO contains a pole at the origin. So the unsteadiness arises because the loop gain has two poles at the origin [11]. The stabilized system is formed by adding a resistor in series with the loop filter capacitor and it modifies the phase difference. A current is injected each time into the loop filter, since the charge pump forms the series combination of R1and C1. By this formation control voltage experiences a large jump.

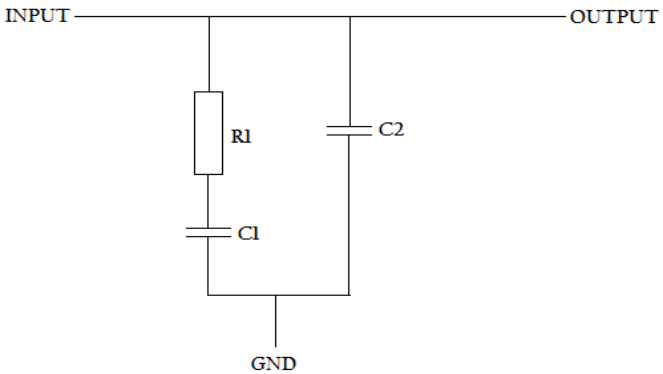

Figure-8 Loop Filter

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V. SIMULATION RESULTS

The Figure-9 shows the schematic view of Phase Locked Loop in Microwind 3.1 Schematic Editor.

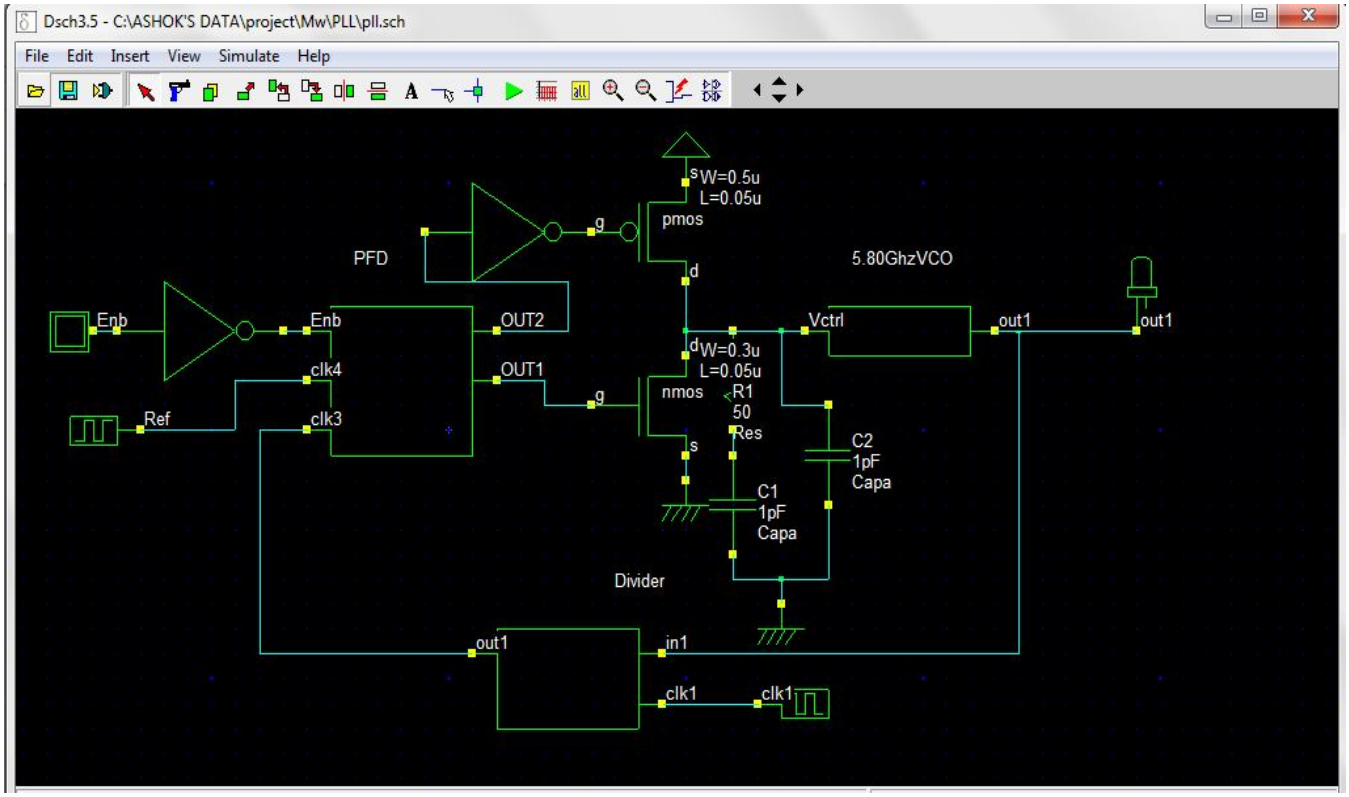

Figure-9 Schematic view of Phase Locked Loop

The Figure-10 is the output of Phase locked Loop and it is simulated in Waveform Analyzer using Microwind.

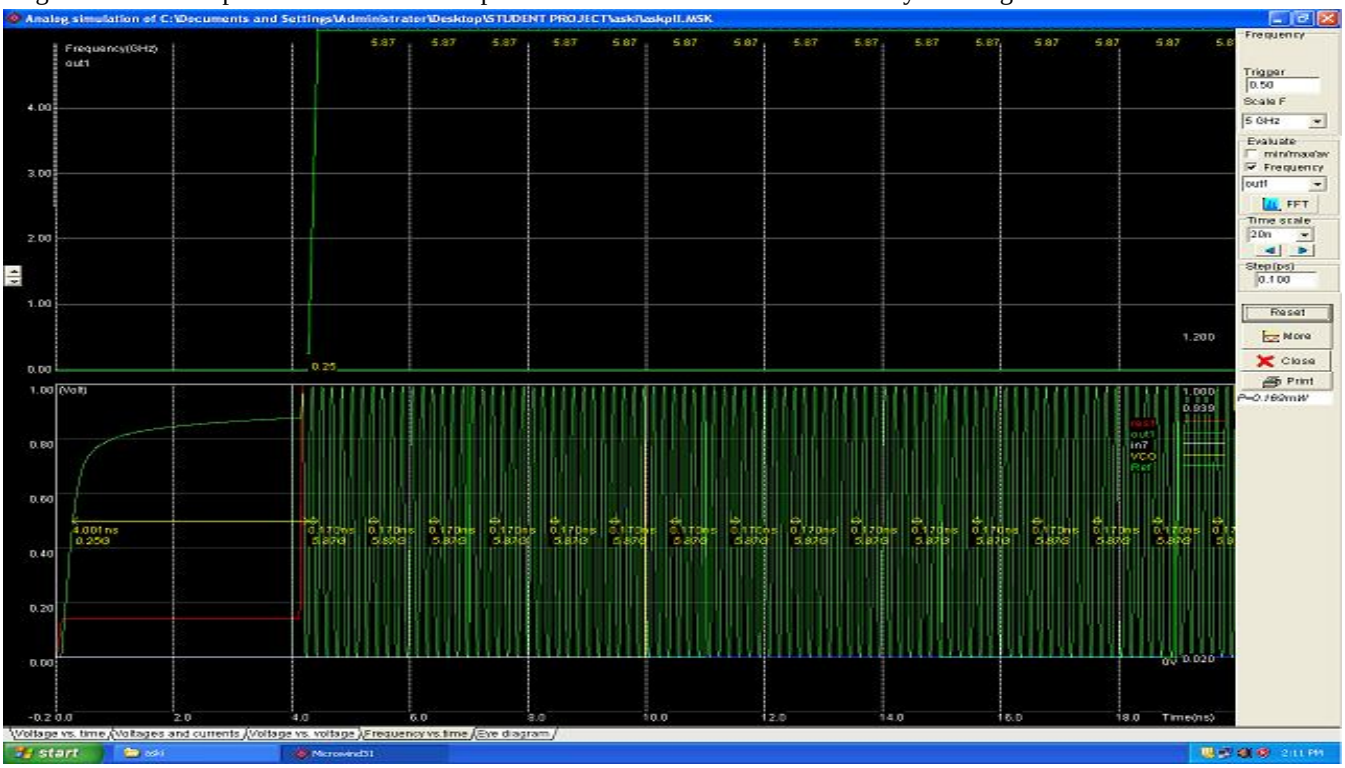

Figure-10 Output of PLL

PLL Specifications and parameters are compared with existing system and proposed system is shown in Table-1.

Table-1 PLL Specifications and parameters

Parameters	Existing System	Proposed System
Input voltage	1.2V	1.2V
Reference Frequency	250MHz	250MHz
Output Frequency	3.3GHz	5.87GHz
Delay time	0.609ns	0.337ns
Average Power	221 µw	201 µw

VI. CONCLUSION

In this paper, Ring oscillator is modified as Current Starved Ring oscillator, so that propagation delay of oscillator gets minimized and wide tuning range is obtained. The XOR phase detector is modified as phase Frequency detector using NAND gate and D-Flip flops so that it cannot lock on the harmonics of the reference signal. The charge pump and loop filter is modified, so that control voltage doesn't experience large jump at the VCO. The average power is obtained as 201µw and delay of VCO is 0.337ns

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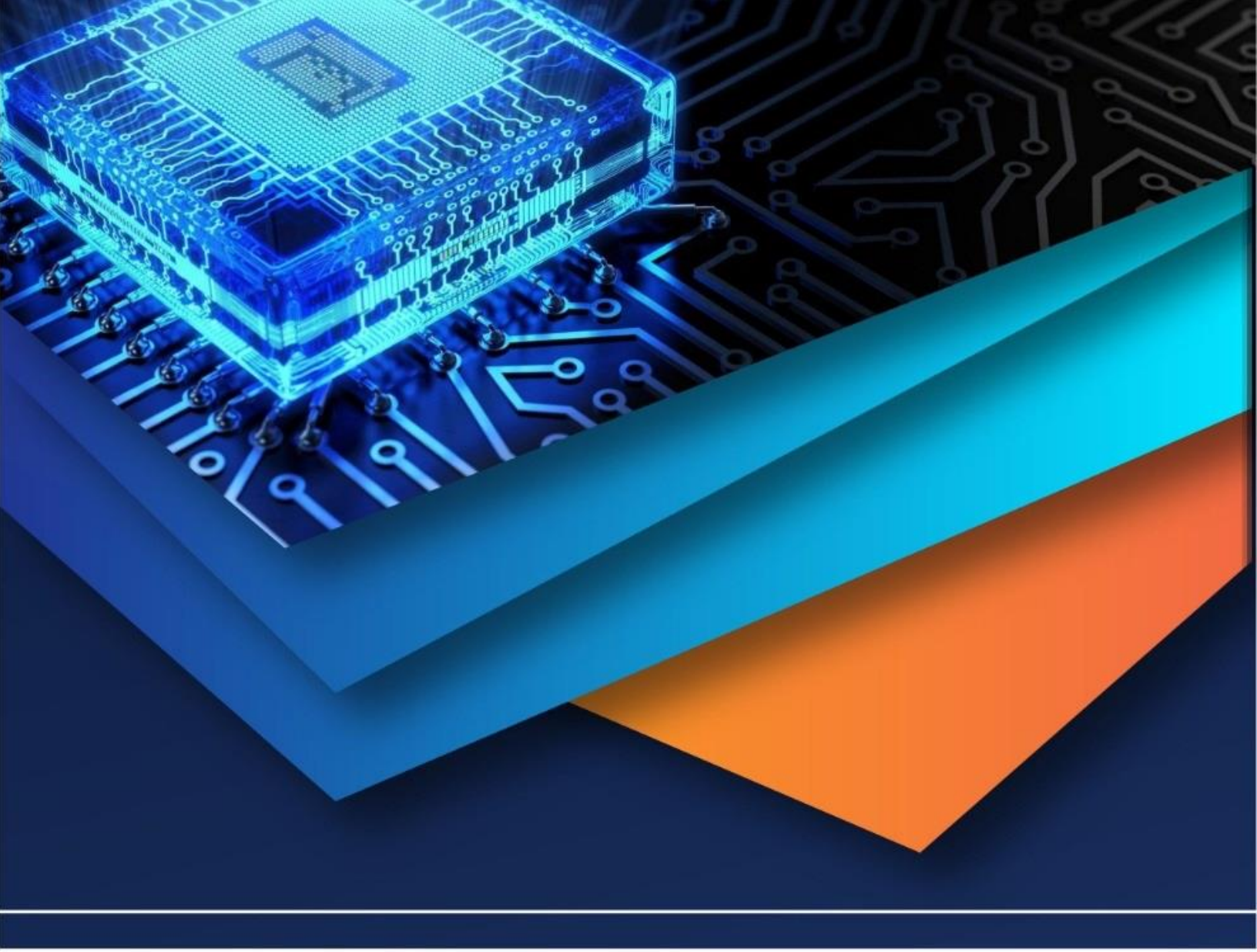

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