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Prediction of Wirelength in Digital Circuits Using Artificial Neural Network

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Abstract: Predicting wire length before placement is called priori wire length estimation. Here we propose a neural network based approach to estimate the total wire length of the digital circuit. Here a three layer neural network is used; a neural network quickly learns the behavior of the placement tool and gives the result similar to the placement tool. Techniques to estimate wire length are becoming important because we need to optimize the circuit in terms of power dissipation, speed and delay when one has freedom to do so. The simulation tools used here are Xilinx and matlab .Xilinx was used to extract the circuit parameters and matlab was used to create a 3 layer neural network.

I. INTRODUCTION

As the technology is improving day by day different parameters are playing important role in the manufacturing of chips[9]. The parameters which were not considered important, and whose power dissipation and speed played negligible role are now given a lot of attention, the evolution which is being focused is that of interconnects for delay.
As more and more transistors are being embedded into the same chip the following effects have been observed[2]:-
Interconnects are playing important role in deciding the device delays
As the width of wire decreases there is increase in interconnect resistance
The total capacitance of interconnect is dominated by the lateral and the fringing components.
Interconnects become more noisy that is interconnect inductance comes into picture.
Here it is analysed how the different components of the interconnect effect the performance of the circuit.

A. Capacitance

Capacitance of the circuit effects the switching speed of the integrated circuits[11]. Capacitive cross talk is one major drawback of the interconnect capacitance, it reffers to the unwanted coupling with the nieghbouring wire which causes interference.If the dynamic circuits with low swing percharge nodes are located in the vicinity of full swing wire they are highly susceptible to cross talk.therefore long and parallel running wires should be spaced out. Technologies today have 5-6 routing layers if wires are interleaved well interwire capacitance reduces.To address cross talks evaluation of design is done after extraction and circuits are modified appropriately to rduce bottlenecks.However if wirelength is estimated from the netlist design these estimations can be made prior extraction and significant design time and iteration cycle can be saved.

B. Resistance

Resistance in the wires causes voltage drop which leads to degradation of signal levels , this is the major problem caused by global interconnects and clock and power rails that are present in circuit. Voltage drop in interconects causes undesirable switching in the transistors and leads to malfunction. As the interconnect causes delay and power dissipation in the circuit various methods to reduce their length have been proposed. Commonly used approach is use of repeaters in the long wires. If we shorten the long interconnects the delay is reduced non linearly but the use of repeaters offsets the delay when wire is long.

C. Inductance

As we move to DSM(deep submicron) technology gate delay can be no longer modeled as RC element. Inductive effects occur from cross talks coupling and oscillation these are changes in waveforms due to overshoots and undershoots[12].
As the traditional techniques are time consuming, new approaches for width and wire length estimation have been introduced. These techniques are based on neural network approach. Once the neural network is trained estimation of any circuit can be done within seconds if the input parameters are known. Input parameters are simple parameters that can be obtained using different EDA tools.

Here In this paper the tool used to extract circuit parameters is Xilinx and the tool used to create and simulate neural network is Matlab. Here we use 7 input parameters to a 3 layer neural network estimate the wirelength of the circuit.

D. The contributions of this paper are

1) Observing a nonlinear relationship between the wirelength and the circuit architecture parameters.

2) Establishing a neural network based approach to quickly estimate the wirelength and as accurate as one can obtain after the placement.

II. BACKROUND

Estimation of circuit wire length before placement is called prioiri wire length estimation .Brief literature review of the previous work has been discussed. Seven of the recent works have been shown in table 1, where the average estimation error has also been shown. The evaluations done in different papers are based on different benchmark circuits. In [1] and [8] a mathematical formula based approach to predict wire length has been introduced, the formula is based on the relation between input and output terminals and total number of gates. This method gives large estimation error of 15%. In [2] also a mathematical formula based approach has introduced, in this method two types of connection have been defined theses are channel i.e. if the cells lie in the same row and feed throughif the cells lie in different rows. In [3],[4] and [5] neural based approach to predict the wirelength has been introduced, neural based approach gives least estimation error, a neural network completely replicates the behavior of the placement tool. In [6] wirelength has been calculated based on three parameters net degree and area, shape distribution of node and range of node.
In this paper the neural network is trained to predict the wirelength of the digital circuits. The estimation has good accuracy and the average estimation errors of 4.161.We use the basic circuit parameters as inputs which are obtained by the Xilninx tool.

Table 1:- Comparison of various techniques

Authors	Technique used	Avg estimation Error
Christie et al. 2000[1]	Wire length estimation using rents rule	15.0%
Liu, Qiang et al. 2016[4]	Estimation of wire length based on pre-placement design methodology	8%
Liu, Qiang et al. 2012[3]	Neural network based pre-placement wire length estimation	2%
Liu, Qiang et al. 2016[4]	Feed forward neural network model for estimation of width	3.98%
Liu, Qiang et al. 2016[5]	Knowledge based neural network model for FPGA width prediction	2%
Hao, Jie et al., 2008[6]	Hierarchical priori wire length estimation	11.6%
Krishnan, Vyas et al., 2006[7]	Design space exploration of RTL data paths using Rent parameter based wire length estimation	4.12%
Our approach	Neural network based approach	4.161%

In this paper the neural network is trained to predict the wirelength of the digital circuits. The estimation has good accuracy and the average estimation errors of 4.161.We use the basic circuit parameters as inputs which are obtained by the Xilninx tool.

III. WIRELENGTH ESTIMATION PARAMETERS

In this paper we consider seven basic aprameters of the digital circuits: number of blocks (n),number of gates(g),number of input (i),maximum fanout(f), total no of outputs(o), no of inputs to the basic block(k) and number of basic blocks (b). These parameters can be easily obtained from the circuit. In this paper Xilinx tool has been used to extract these values. large values of n, g and b repersent a large circuit thus a long wirelength is required. In [2] it is established that the correlation factor among these is really high, it is found that the correlation afctors are 0.996,0.9817,and 0.996 respectivly. This shows that these parameters of the circuit have significant impact on the wirelength of the circuit. These three parameters are themselves correlated as large value of one leads to the large value of the other but this is not always true that is why we take them individually

Maximum blocks interconnected with each other within a net a repersented by fanout it determines the span of net[7]. The large span of net also means large area and also long wirelength. F also indicates inter-net realtionship as more nets directly connected means more nets realted. The correlation factor between wl and f is 0.9799.

Input and outputs also affect the wirelength as input and output have a fixed location on the chip. More number of input and output means larger wirelength . the correlation factor between I,o and wl is .8690

onto one LUT, then number of blocks (k) will decrease and hence the wirelenfdth of the circuit also decreases.

IV. NEURAL NETWORK BASED APPROACH

In the previous section we have presented seven parameters on which the wirelength of the circuit depends. It is also known that the wirelength does not have a lenaer relationship with these parameters infact theses parameters interact with each other making them difficult to formulate.

Wl = f(f,o,I,b,g,k,n)

Neural network approach is perfect for this function as the NN's have the capability of learning complex functions and unknown input output relationships. In this paper we establish a approach to accuratly estimate the wirelength. The wirelength estimation is done without practically running the placement tool to achieve this we train a NN to learn the behaviour of the placement tool.

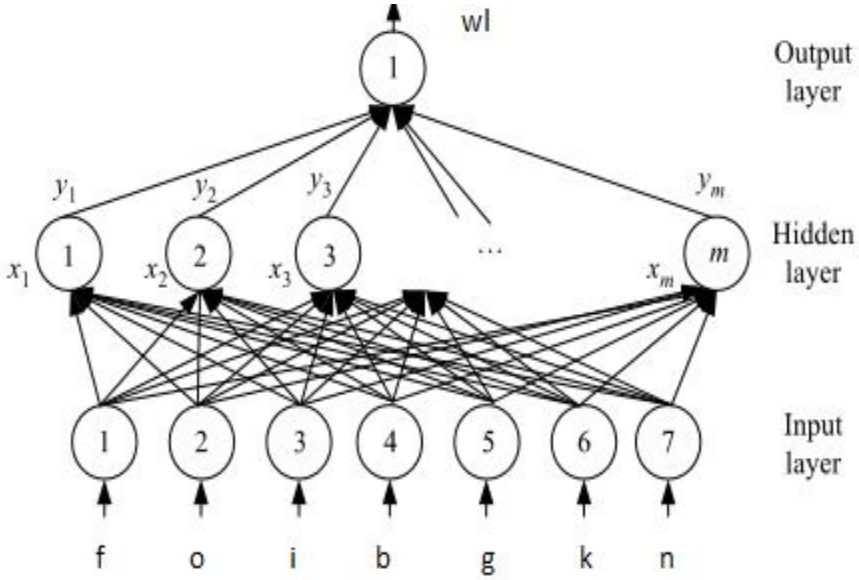


Fig:-1 Three layer neural network

A three layer neural network has been shown in fig.1 it has seven input parameters and thus 7seven neurons in the input layer. The hidden layer has 12 neurons and the output layer has one neuron as we have single output that is the wire length of the circuit. The input to each neuron at hidden layer is the weighted sum of the input parameters.

$$x_1 = w_{11}^1 f + w_{21}^1 o + w_{31}^1 i + w_{41}^1 b + w_{51}^1 g + w_{61}^1 k + w_{71}^1 n$$

In order to replicate the behavior of the EDA tool neural network has to be trained with the help of training data i.e seven input parameters and their corresponding wl, this data is extracted using EDA tools.

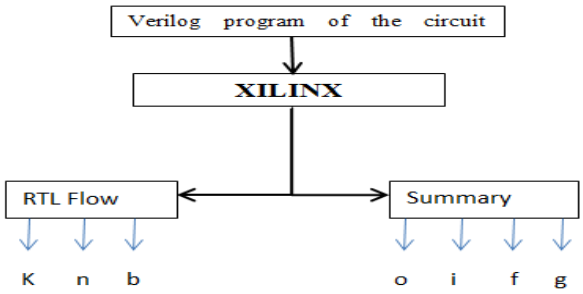


Fig:-2 EDA flow

The EDA flow represents how various circuit elements are extracted.

V. EXPERIMENTAL RESULTS

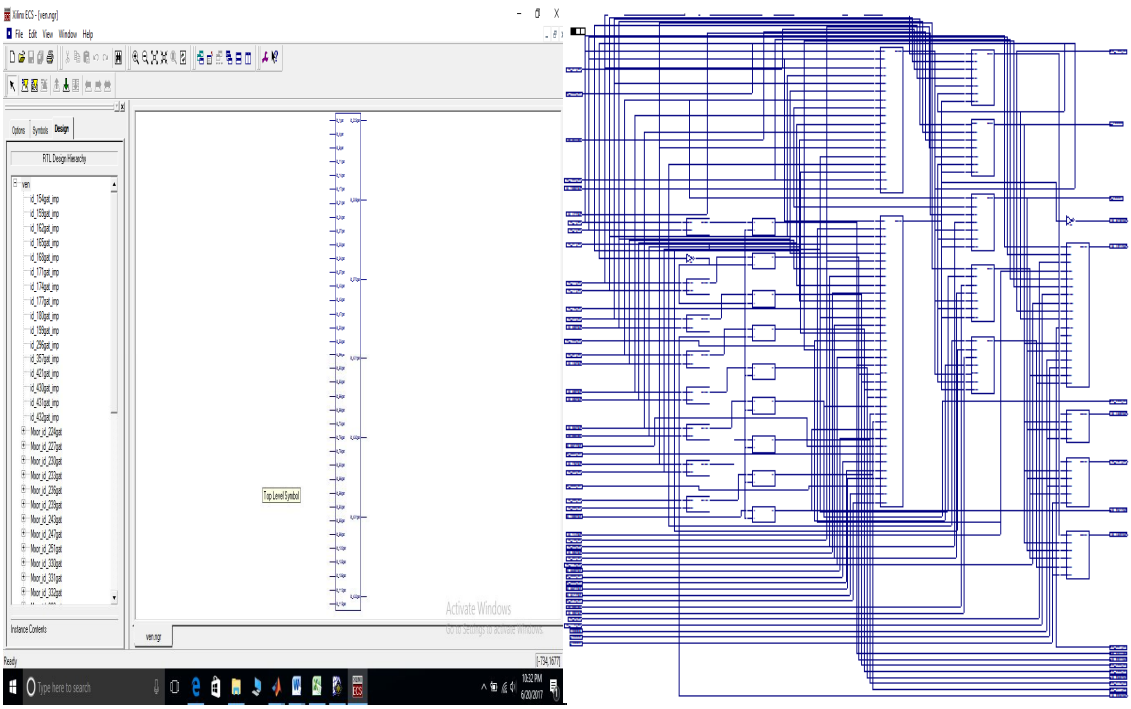
In our experiment we use 25 benchmark circuits for training neural network. These benchmark circuits are listed in table 1.1.

Table 2:- List of the benchmark circuits used for training of the neural network

c432	c432nr	s298	s526
c499	c499nr	s386	s510
c880	c1355nr	s344	s420.1
c1355	c2670nr	s349	s832
c1980	s27	s382	s641
c2670	s208.1	s444	s713

Number of blocks in these circuits varied between 80-200.The general maximum fan out of these circuits came out to be 100.View of the RTL obtained using Xilinx is shown in figure 2 for one of the circuit. Number of input lines for the circuit vary between 5-60.Number of output lines of the circuit varies between 5-30. Number of basic blocks in the circuit each containing LUT vary between 5-20. RTL view of the basic block is shown in figure 2.

(a.) (b.)



(c.)

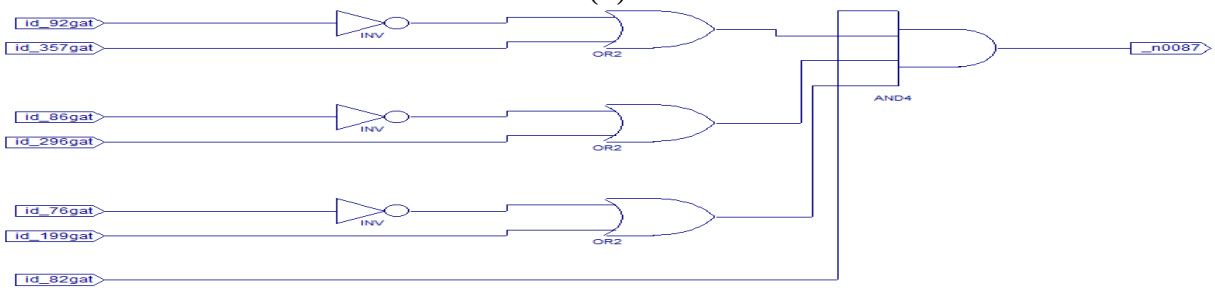


Fig:-3 RTL view of the circuit c432 in xilinx

Neural network is created using Matlab. A three layer neural network is created; input layer has seven neurons corresponding to the seven inputs. The hidden layer has 10 neurons and the output layer has one neuron corresponding to one output that is wirelength of the circuit. Weights of the neural network are adjusted as we train the neural network training of neural network is shown in figure 3. Benchmark circuits mentioned above used for training data.

(a.) (b.)

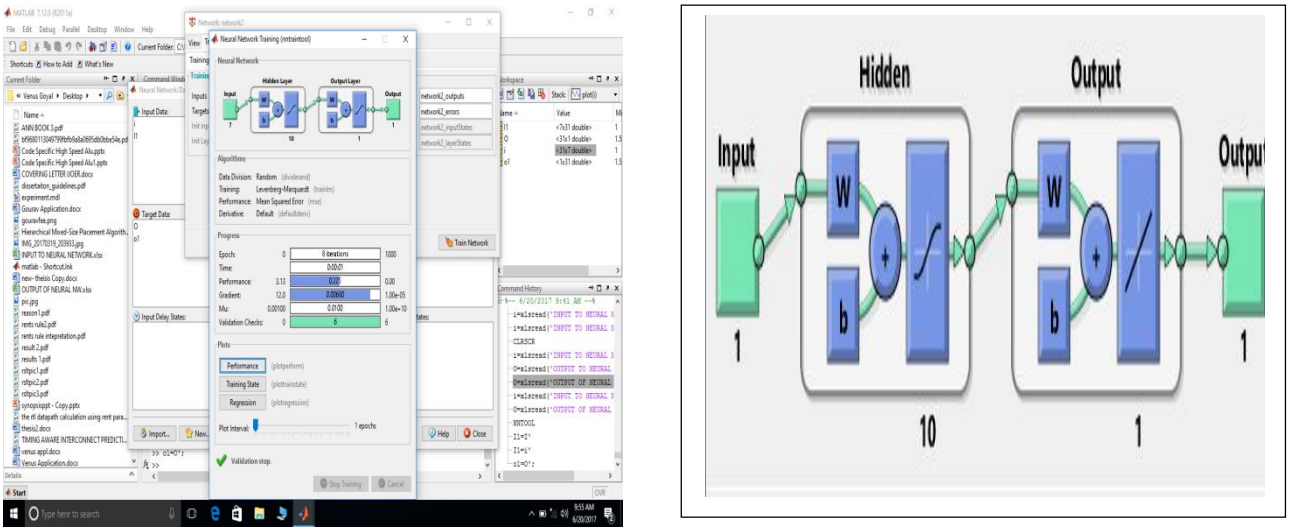


Fig 4:-(a.) Neural network during training
(b.) obtained neural network after training

Training validation and testing graph obtained after the testing of neural network is shown in figure 5.It is observed from the graph error reduces as we train the neural network best validation result is obtained at first epoch with an error of 0.0018489.

(a.) (b.)

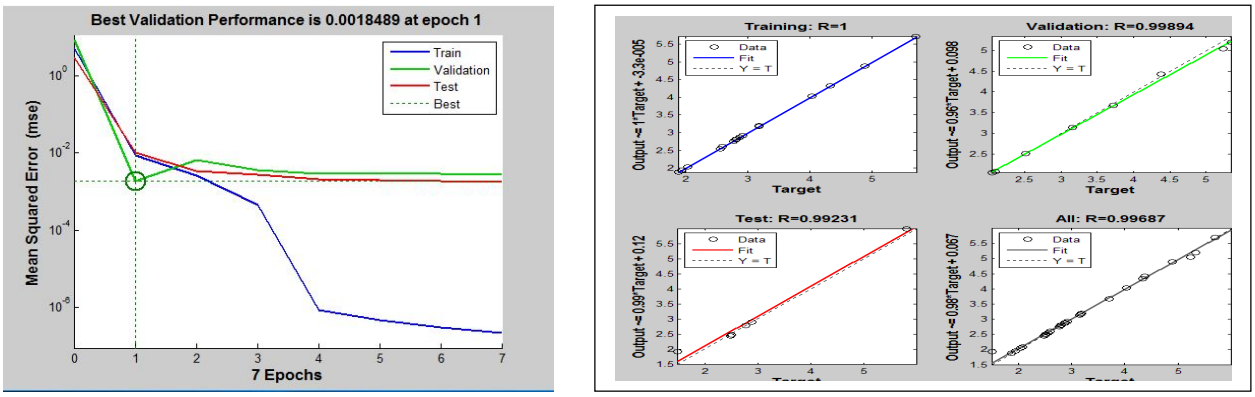


Fig 5:- Simulation results

Simulation of the neural network is done using 7 circuits. Average estimation error is calculated from the results obtained.

Table 3:- Average estimation error of the circuits simulated

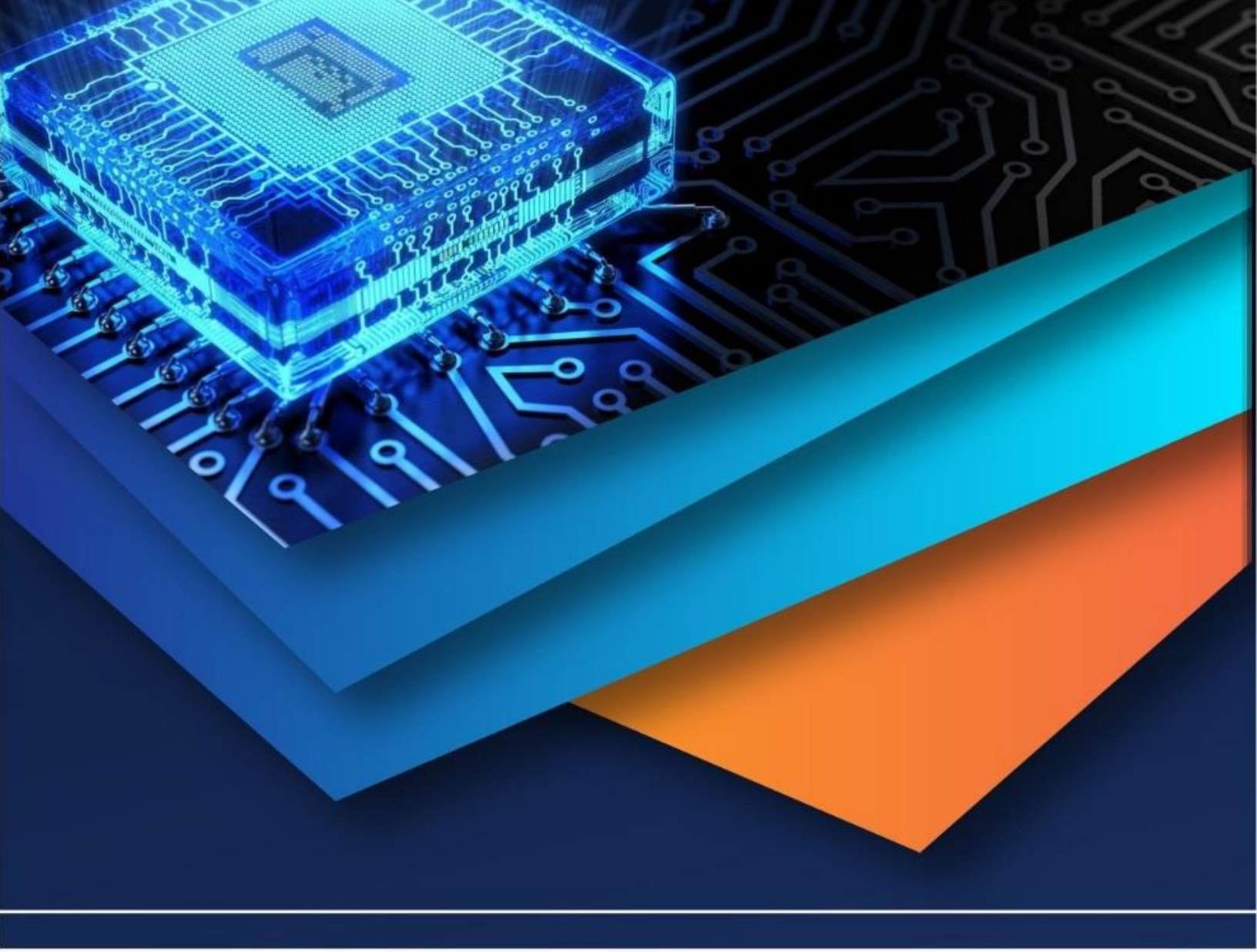
Circuit	Our estimation	Actual wire length [10]	Average estimation error
s953	4.371	4.371	4.66
s1238	4.885	4.885	2.88
s1196	4.33	4.33	4.07
s1494	5.806	5.806	5.5
s1488	5.703	5.703	3.48
s1423	2.552	2.552	4.38

VI. CONCLUSION

In this work we propose a neural network based approach for wire length estimation. In this approach neural network learns the behavior of the placement tool and approximates total wirelength. Approximation is based on seven input parameters and the result is as accurate as the EDA tool. The average estimation error comes out to be 4.161.

REFERENCES

[1] Christie, Phillip, and Dirk Stroobandt. "The interpretation and application of Rent's rule." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 8.6 (2000): 639-648.
[2] Shah, Shweta, NazaninMansouri, and Adrian Nunez-Aldana. "Pre-Layout Estimation of Interconnect Lengths for Digital Integrated Circuits." 16th International Conference on Electronics, Communications and Computers (CONIELECOMP'06). IEEE, 2006
[3] Liu, Qiang, Jianguo Ma, and Qijun Zhang. "Neural network based pre-placement wirelength estimation." Field-Programmable Technology (FPT), 2012 International Conference on. IEEE, 2012
[4] Liu, Qiang, et al. "Feedforward Neural Network Models for FPGA Routing Channel Width Estimation." Chinese Journal of Electronics 25.1 (2016): 71-76.
[5] Liu, Qiang, Ming Gao, and Qijun Zhang. "Knowledge-Based Neural Network Model for FPGA Logical Architecture Development." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24.2 (2016): 664-677
[6] Hao, Jie, and SilongPeng. "HJ-hPl: Hierarchical Mixed-Size Placement Algorithm with Priori Wirelength Estimation." Young Computer Scientists, 2008. ICYCS 2008. The 9th International Conference for. IEEE, 2008.
[7] Krishnan, Vyas, and SrinivasKatkoori. "Design space exploration of RTL datapaths using Rent parameter based stochastic wirelength estimation." Proceedings of the 7th International Symposium on Quality Electronic Design. IEEE Computer Society, 2006.
[8] L.Hagen et.al, "On the intrinsic Rent parameter and spectra-based partitioning methodoligies", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol.13, Jan.1994,pp.27-37.
[9] D.Stroobandt and J. Campenhout. Accurate interconnection length estimations for predictions early in the design cycle. In VLSI Design, Special Issue on Physical Design in Deep Submicron, volume 10, no.1, pages 1–20, 1999.
[10] C. Sechen "Average interconnection length estimation for random and optimized placements"In Proceedings of IEEE International Conference on Computer Aided Design, pages 190–193, November 1987.
[11] J. M.Rabey, A. Chandrakasan, and B. Nikolic. Digital Integrated Circuits, A Design Perspective. Pearson Education Electronics and VLSI Series, 2003.
[12] K. Banerjee and A. Mehrotra. "An interconnect scaling scheme with constant on-chip inductive effects" In Analog IntegratedCircuitsandSignalProcessing,volume35,pages 97–105, 2003.



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