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Zero Temperature-Coefficient Bias Point for Asymmetrical and Symmetrical Double Metal Double Gate MOSFETs

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Abstract*: In this paper, the zero-temperature-coefficient (ZTC) bias point for asymmetrical double metal double gate (ADMDG) and symmetrical double metal double gate (SDMDG) over wide range of temperatures (200-400K) has been identified at nanoscale through 2-D device simulation. The simulation results give the existence of inflection point (ZTC bias point) i.e. ZTC bias point and device parameters become independent of temperature variation. The major FOMs such as trans conductance (g_m), output conductance (g_d), intrinsic gain (A_v), drain insulated barrier lowering (DIBL), subthershold swing (SS), on-off current ratio (I_{on}/I_{off}), and cut off frequency (f_T), shows the impact of temperature. The performance comparison is made for both ADMDG and SDMDG at different values of temperature. From the results, it is confirmed that there are two different ZTC bias points, one for I_D (ZTC_{ID}) and other for gm (ZTC_{gm}). Analysis shows an opportunity for realizing analog and RF circuits for wide range of temperatures.

Keywords: ***ADMDG, Gate engineering, SCEs, SDMDG, Analog and RF FOMs.***

I. INTRODUCTION

Recently, Industries are interested in designing such type of devices or circuits which can be efficiently operated on various range of temperature. Integrated circuits (ICs) are designed for specific application for example high temperature operating devices are always used in nuclear sector, automobile and military application same as for low temperature application in medical field and space field. Industries demand both low and high temperature [1]-[2]. The main motive of designed such type of integrated circuit which can be used in both low temperature and high temperature application. These days trend of ICs designed are shifted from conventional CMOS to SOI based MOSFETs. CMOS technology designed with SOI devices offer reduction in junction capacitance, second order effect and various short channel effect (SCEs) minimize in SOI MOSFETs. At high temperature the problem of leakage current and latch up affect the performances of conventional CMOS and the problem of latch up removed in SOI MOSFETs and leakage current also minimized [3]-[5]. All the digital and analog circuits are always biased about a point where the I-V characteristics show no or little variation with respect to temperature. This point is called ZTC point. Pradhan et al. have identified the ZTC point for SOI MOSFETs of single gate and double gate for 100K-400K temperature range [6]-[8]. Osman et al. [9] have presented both experimental and analytical result for ZTC point over a wide range of temperature for partially depleted (PD) SOI MOSFET. Tan and Goel [10] analysed the fully depleted (FD) SOI n-MOSFET over a wide range of temperature (300K-600K).

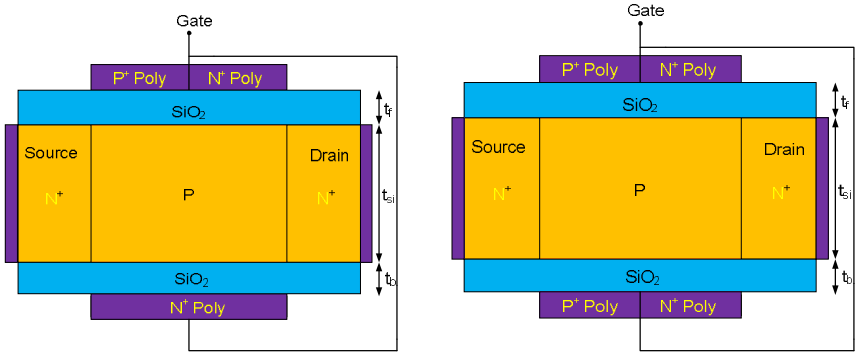
The double metal double gate (DMDG) MOSFET fabricated on SOI shows attractive features of low drain insulated barrier lowering (DIBL), low subthershold swing (SS), low leakage current, high current drivability (I_{on}), trans conductance (g_m), reducing short channel effect (SCEs) and suppression of latch-up phenomenon [11]-[13]. They also offer very good opportunity for analog and RF application [14]-[15]. In recent work [16], ZTC bias point is investigated on single metal for single gate, double gate and double gate with high-k gate dielectric so analysis of ZTC point for DMDG structure provide enough information about impact of temperature on device as well as improved performance over previous structures of SOI MOSFET.

Normally, the behaviour of drain current (I_D) is opposite before and after certain bias point with change in temperature. The value of current depends on temperature due to mobility and high field effect produced by bias voltage [17]. It is very important to have enough information about device performance for analog and RF application over wide range of temperature [18]. To the best of our knowledge, this is probably the recent approach for investigating a detailed analysis of inflection point (ZTC bias point) to examine its reliability issues over a wide temperature range (200-400K) as far as both analog and RF application of a double metal technology are concerned. Performance comparison is made between ADMDG and SDMDG MOSFETs.

In this paper, Section II, describes the devices, which include all the dimensions, materials and doping concentrations. Section III, describes model and method activated for numerical simulation. This is the recent approach to find out ZTC point of ADMDG and SDMDG by using 2-D ATLAS (SILVACO) simulator. In Section IV, various performance metrics of device including the SCEs like DIBL, SS and I_{on}/I_{off} ratio, and analog and RF figure of merit (FOMs) such as trans-conductance (g_m), output conductance (g_d), intrinsic gain (A_v), gate to source capacitance (C_{gs}), gate to drain capacitance(C_{gd}), and cut-off frequency (f_T), are observed subject to temperature variations. Finally conclusion is conferred in section V.

II. DEVICE DIMENSIONS

In this paper two different structures ADMDG and SDMDG are presented as shown in Fig. 1. The structure adopted different physical dimension that is given here with following specification. The thickness of silicon oxide thickness is 1.1 nm with channel length of 40nm technology trend and source and drain length is 20nm which are vertically placed in this structure, the thickness of silicon body is 10nm with width of 0.5µm. The metal gate work function tuned between 4.6eV and 4.8eV with fixed threshold voltage of 0.4V at room temperature [14]. Metal gate technology is used here due to their unique property of eliminating degradation in transistor performance. One of best material used here for metal gate technology is Molybdenum because its work function is adjusted between desired range of 4.5eV to 5eV [15]. Source and drain (S/D) are highly doped (n-type= 1x 10^{20} cm^{-3}) due to minimize effect of mobility degradation by coulombs scattering [16] .The structure followed the 45nm technology node which also fulfil the requirement of international technology road map for semiconductor (ITRS) [19].



(a) (b)

Fig. 1 Schematic of simulated device (a) Asymmetric double metal double gate (ADMDG), (b) Symmetrical double metal double gate (SDMDG) SOI MOSFET

III.SIMULATION SETUP

The 2-D numerical device simulator ATLAS is used to simulate the structure of ADMDG and SDMDG SOI-MOSFET. Drain bias is fixed at numerical value V_{DD}=1.0V and V_{DS}=0.5V [16] with varying gate to source voltage from V_{GS}= 0-1.0V. I_D-V_{DS} transfer characteristics provide the value of threshold voltage (V_{th}). The drift and diffusion approach [20], field dependent mobility, concentration dependent mobility and velocity saturation models are used here for 2-D numerical simulation. The mobility of MOSFET is very complex and associated with temperature variation and defined by scattering parameters. The Berkeley Short Channel IGFET Model (BSIM) combined the scattering parameters into an effective mobility using Mathiessen's rule. The physical models for electric field and temperature depend on mobility are Lombardi models (constant voltage and temperature, CVT) [21], with Shockley –Read-Hall (SRH) [22]-[23] model and Auger recombination model specified here. Shocklay Read Hall (SRH) and auger recombination models used for minority carrier recombination. The model temperature is used for varying operating temperature (100-400K). The impact ionization and band-to-band Auger recombination model are used in the simulation works.

In the structure of ADMDG and SDMDG, interface trapped charge density considered at a semiconductor to insulator interface .The presence of trapped charge develop an extra non-linear potential and varying electric field across the gate dielectrics. This can be reduced by using high permittivity gate material. The trapped charge density also affect threshold voltage of device which can be adjusted by change in supply voltage. However, one of the key is the process induced defect which degrades device mobility resulting in poor performance and reliability. So in this simulation, interface trapped charge density is considered at a semiconductor-insulator interface for both ADMDG and SDMDG is 1 x 10^{11} cm^{-2}. The typical concentration trapped charge density range between 10^{10} cm^{-2} and 10^{11} cm^{-2}. The electron and hole surface recombination velocity is considered as 1 x 10^4 cm/s. In this simulation, all the junctions of structures are assumed as abrupt and doping profiles are uniform.

IV. RESULT AND DISCUSSION

The 2-D numerical device simulator ATLAS is used to simulate the structure of ADMDG and SDMDG SOI-MOSFET. The drain insulated barrier lowering (DIBL), low subthershold swing (SS), and I_{on}/I_{off} are essential parameters to analyze in nanoscale device design. The important analog circuit parameters transconductance (g_m), output conductance (g_d), intrinsic gain (A_v) are concerned here and for evaluation of RF performance cut-off frequency (f_T) is most important parameter. The variation in temperature changes various physical parameters like carrier mobility decreases with increase in temperature as

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-n} \quad (1)$$

where n is an exponent term which varies from 1.6 to 2.4 [24]. The threshold voltage (V_{th}) is varied by temperature. The drain current I_D affected by both parameters mobility and threshold voltage V_{th} as [9]

$$I_D(T) \propto \mu(T)[V_{GS} - V_{th}(T)] \quad (2)$$

Both the term mobility and threshold voltage have opposite behaviour with respect to temperature about a fixed gate bias voltage. The effect of both term cancelled at fixed value of bias voltage, which is defined as ZTC bias point.

At $V_{GS}>V_{th}$, the behaviour of g_m with temperature is just reverse to that of $V_{GS}< V_{th}$ because of mobility degradation. The reduction in V_{th} with temperature increases g_m, while the degradation of mobility decreases g_m. These two phenomena compensate each other to give rise to a ZTC bias point for g_m. From Fig. 2(a)-(b), we can conclude that the value of transconductance ZTC point (0.38 V) is lower than the drain current ZTC bias point (0.50V). ZTC_{ID} and ZTC_{gm} bias points are two important FOMs in analog circuit design for wide range of temperature. The intrinsic gain ($A_V=g_m/g_d$) is precious FOM for amplifier and is shown in fig. 2(c). From the graph, similar type of analysis can be made in case of g_m and g_d. The intrinsic gain can also be expressed in term of early voltage V_{EA} as

$$A_V \cong \frac{g_m}{g_d} \cong \frac{g_m}{I_d} V_{EA} \quad (3)$$

According to (3), high gain device is also responsible for higher value of V_{EA}. From the Fig. 2, it has been observed that performance of SDMDG device is superior as compared to ADMDG device under similar conditions. From the Fig. 2(c) it is also seen that the gain of SDMDG device is about 56dB as compared to 50dB of ADMDG device at a temperature 400K.

Fig. 3(a)-(c) present a comparison plot for all the three important parameters which include the variation of drain insulated barrier lwering (DIBL), subthershold swing (SS) and I_{on}/I_{off} ratio for different temperatures. Drain insulated barrier lowering (DIBL), subthershold swing (SS) and I_{on}/I_{off} ratio are important short channel parameters, essential to analyze in nanoscale device design. In short channel device, however, the source drain potential have a strong effect on the band bending over significant portion of the device. Therefore, the threshold voltage, and consequently subthershold current of short-channel device, varies with the drain bias. The effect is referred to as DIBL. DIBL occurs when the depletion region of surface lower to source potential barrier. When high drain voltage applied to a short- channel device, it lowers the barrier height. The source then injects carriers into the channel surface (independent of gate voltage). DIBL is enhanced at high drain voltage and shorter channel lengths. Major contributors to the gate leakage current are gate oxide tunnelling and injection of hot carrier to the gate oxide. To calculate SS of the devices, the drain current is plotted in logarithmic axis against the gate voltage (V_{GS}). SS is the important parameters for calculating the off state current. These parameters are calculated as per (4), (5) and (6).

$$SS = \frac{kT}{q}\ln(10)\left[\frac{\partial \phi_{s\min}}{\partial V_{GS}}\right]^{-1} = \left[\frac{\partial \log_{10}(I_D)}{\partial V_{GS}}\right]^{-1} = \ln(10)\frac{kT}{q}\left(1+\frac{C_{dep}}{C_{ox}}\right) \quad (4)$$

where C_{dep} is depletion capacitance, C_{ox} is gate oxide capacitance, q is charge of electron, k is Boltzmann's constant, and T is temperature. At room temperature (300 K), the ideal value for SS is 60mV/decade, i.e. a 60mV change in gate voltage bring about a tenfold change in drain current. Also SS can be related to temperature as follows

$$SS\left(\frac{mV}{decade}\right) = 60mV\frac{T}{300K} \quad (5)$$

According to (5), SS will increase or decrease according to T. From the extracted values of SS which is shown in Fig. 3(b). The most important improvement is reduction of SS at 200K. The improvement occurred due to kT/q term. As temperature increases from 300K, the SS values rapidly increase and the reverse can also be observed from the inset values. By comparing the SS values

between ADMDG and SDMDG configurations, at 300K, the ADMDG device shows 63.46 mV/decade where SDMDG devices show around 62.27 mV/decade which is near to ideal value.

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{V_{th1} - V_{th2}}{V_{DS2} - V_{DS1}} \quad (6)$$

where V_{th1} and V_{th2} are two threshold voltages calculated for two different drain bias V_{DS1}=0.1V and V_{DS2}=0.5V respectively. With increase in temperature the carriers are energized and further enhance the carrier transport efficiency. The decrease in on-current and increase in off-current with temperature is shown in Fig. 3(c). The I_{on}/ I_{off} ratio is an important parameter for switching applications. It should be marginally high for a good switch. The off-current is significantly reduced by SDMDG device structures as compared to its counterpart ADMDG as shown in Fig. 3(c). Similarly, because of improved carrier transport efficiency and low leakage current, the SDMDG configurations provide higher on-current. It is clear that the value of on-off current ratio is much higher for SDMDG configurations as compared to that of ADMDG case. It is in the range between 10^8 and 10^9 in case of ADMDG while 10^9 and 10^{10} in case of SDMDG. It can also be observed that I_{on}/I_{off} decreases with increase in temperature. This is because of high I_{off} at higher temperatures. I_{off} shows a very low value for 200K and starts increasing with increase in temperature beyond 200K, which is due to low subthreshold slope (SS) and high V_{th} values at low temperatures. As the off state current is directly related to SS as well as temperature T [24] according to following equation

$$I_{OFF} = 100\frac{W}{L}e^{-qV_{th}/\eta kT} = 100\frac{W}{L}10^{-V_{th}/SS} \quad (7)$$

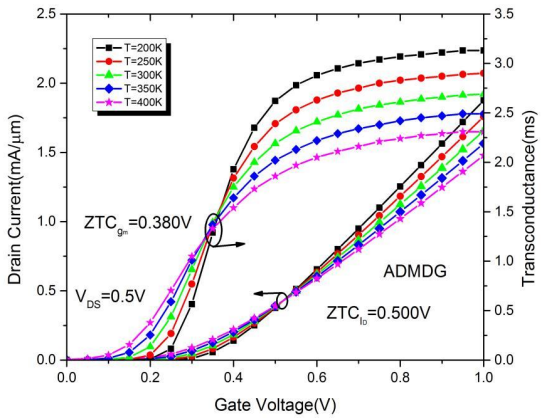
where W, L, q, V_{GS}, V_{th}, k, T, SS and η are width of the channel, channel length, charge of electron, gate to source voltage, threshold voltage, Boltzmann's constant, temperature in Kelvin, subthreshold slope, and body factor respectively.

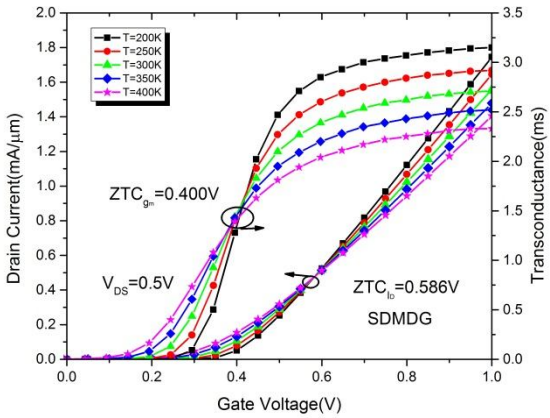
Fig. 4(a) shows the intrinsic capacitances (C_{gs} and C_{gd}) as a function of V_{GS} for both sub-threshold or weak inversion and super-threshold or strong inversion regions. The capacitances between each pair of electrode for all devices are calculated by a single AC frequency (1MHz) when a DC ramp voltage swing from 0 V to 1 V with a step of 0.025 V is applied From the figure, it is clear that the re-exists source-to-gate capacitance ZTC point (ZTC_{Cgs}) without the existence of source-to-drain capacitance ZTC point (ZTC_{Cgd}). The ZTC_{Cgs} points are identified with a lower value as going from ADMDG (0.40 V) to SDMDG (0.45V). In sub-threshold region (below ZTC point), the value of C_{gs} is more for higher T and it gradually decreases as T decreases. However, the reverse situations have been observed in the superthreshold region (above ZTC point). In case of C_{gd}, the parameter remains constant in the subthreshold region and starts increasing gradually in superthreshold region.

Cut-off frequency (f_T) plays a vital role in evaluating the RF performance of the device which is plotted in Fig. 4(b). Generally, f_T is the frequency at which the current gain is unity.

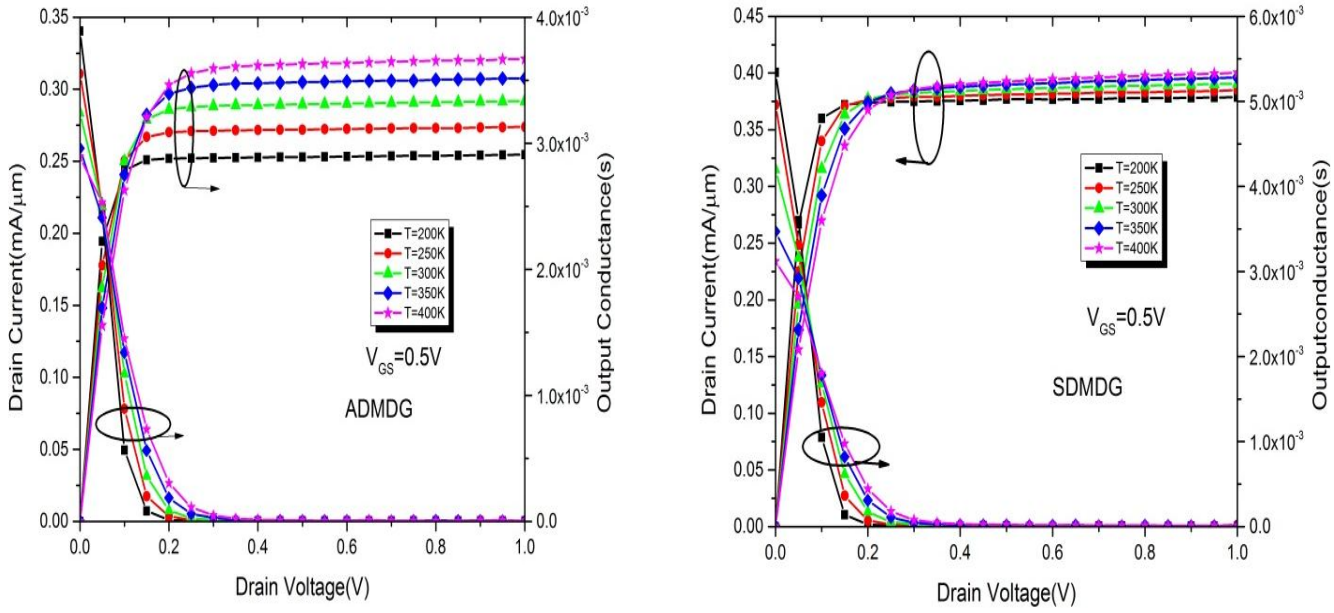
$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (8)$$

where g_m, C_{gs} and C_{gd} are the trans conductance, the total gate capacitance gate to source capacitance, and gate to drain capacitance respectively. At low temperature, there is improvement in cut-off frequency. The crucial parameters for SCEs, analog and RF performances are tabulated in TABLE I. From the observations, SDMDG have edge over ADMDG for all the performances at wide range of temperature.





(a)



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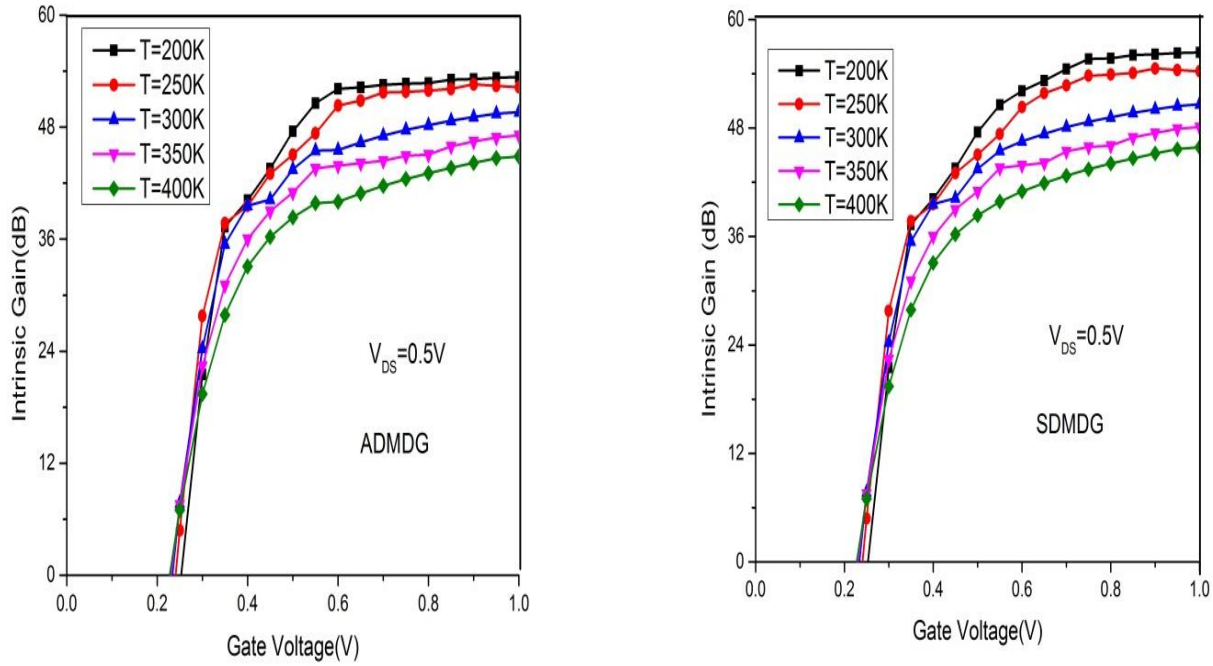


(c)

Fig. 2 (a) Drain current (I_D) and transconductance (g_m) as a function of gate voltage (V_{GS}), (b) Drain current (I_D) and output transconductance (g_d) as a function of drain voltage (V_{DS}), (c) Intrinsic gain (A_V) as a function of gate voltage (V_{GS}) for different configurations as ADMDG and SDMDG SOI MOSFETs

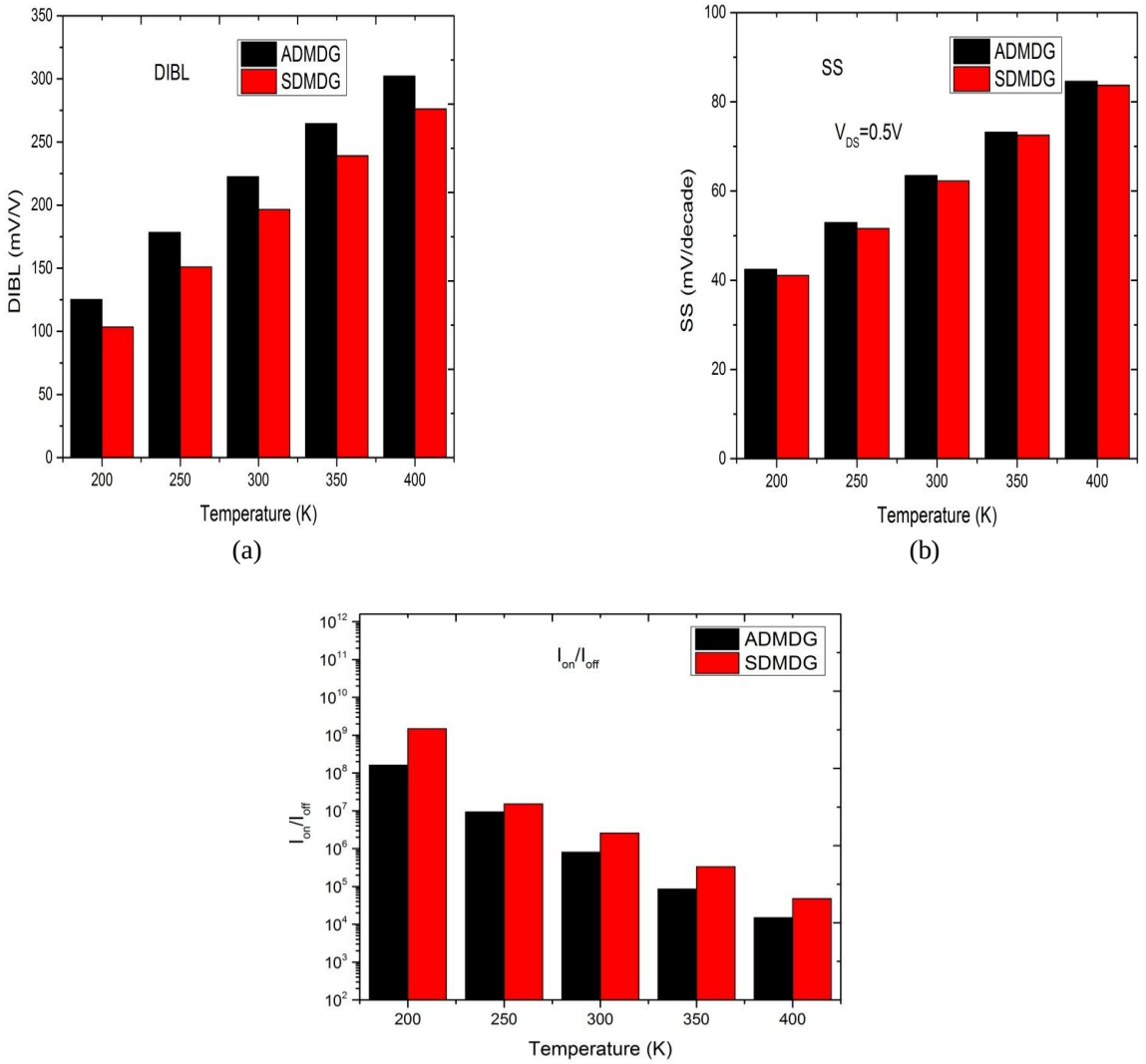
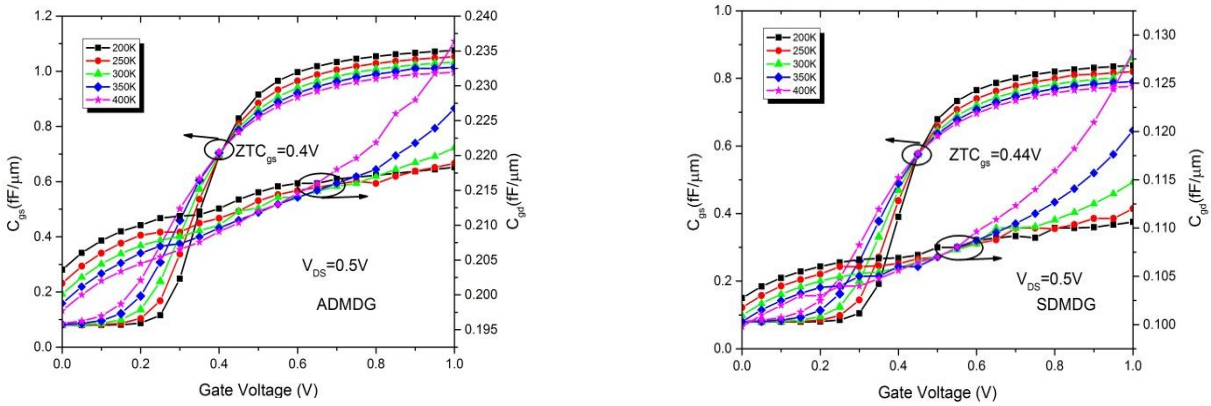
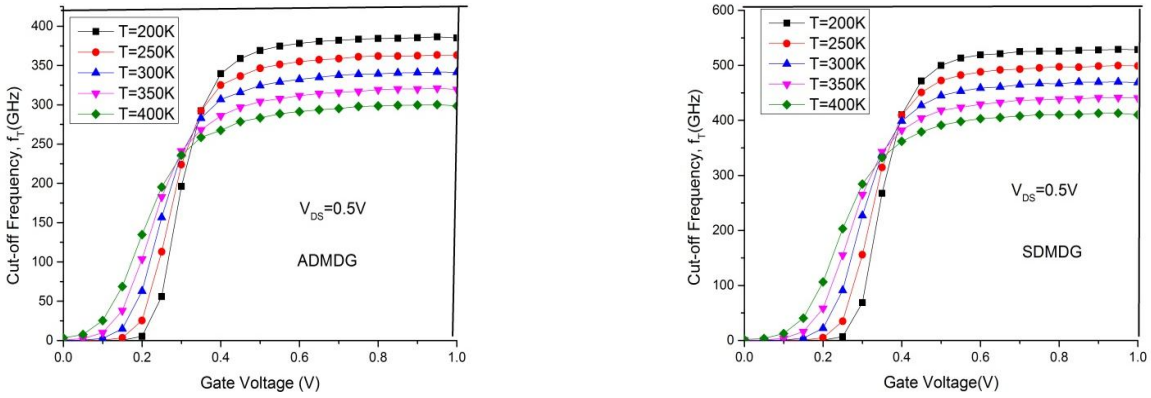


Fig. 3 (a) Drain insulated barrier lowering (DIBL), (b) Subthershold swing (SS), (c) On-Off current ratio (I_{on}/I_{off}) as a function of temperature for different configurations as ADMDG and SDMDG SOI MOSFETs





(b)

Fig. 4 (a) Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}), (b) Cut-off frequency (f_T) as a function of gate voltage (V_{GS}) with different value of operating temperature for ADMDG and SDMDG structures

TABLE I
DIFFERENT CRUCIAL PARAMETERS COMPARISON WITH TEMPERATURE VARIATION FOR ADMDG AND SDMDG CONFIGURATIONS

Temperature (K)	I_{on}/I_{off}		A_V (dB)		f_T(GHz)	
	ADMDG	SDMDG	ADMDG	SDMDG	ADMDG	SDMDG
400K	1.0×10^4	1.8×10^4	40.6	42.3	301.5	400.6
350K	1.0×10^4	1.2×10^5	45.8	46.5	312.4	440.9
300K	1.5×10^5	1.6×10^6	47.0	52.2	333.2	455.3
250K	1.0×10^7	1.0×10^8	51.9	53.7	350.7	500.5
200K	1.3×10^8	1.4×10^9	54.0	58.0	380.6	550.0

V. CONCLUSIONS

In this paper, the ZTC bias points of the ADMDG and SDMDG, SOI MOSFETs are investigated using the 2-D numerical simulation. The simulation results presented in this work gave a detailed idea about the ZTC bias point for parameters like I_D, g_m, C_{gs}, and f_T. Also the comparison is made between various parameters like I_{on}/I_{off}, A_V, and f_T for ADMDG and SDMDG over a wide range of temperatures. It is observed that at a particular temperature (300 K), the SDMDG device shows nearly 10 times more in I_{on}/I_{off}, 11.07% increase in A_V, and more than 37% rise of f_T as compared to ADMDG device. The results provided in this paper can be used as a good reference tool for designing circuits meant for wide range of temperature variation applications. From the investigation on ZTC, it is evident that SDMDG configurations lead to a significant improvement in DC, analog, and RF performances as far as nanoscale MOSFET modeling is concerned. Finally, authors have presented the most important aspects of parameter variations with temperature and left scopes for further investigation.

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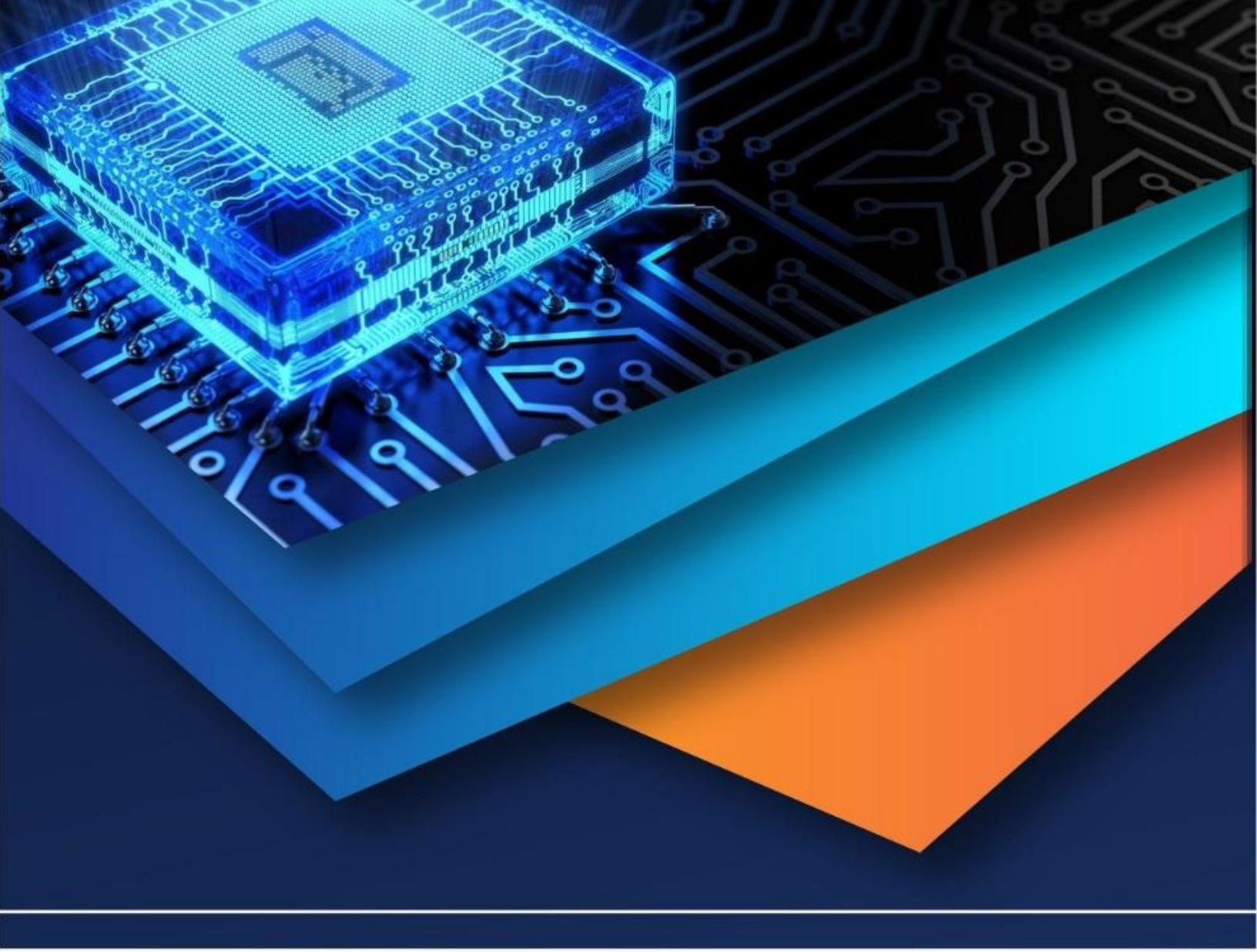

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