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Design and Implementation of Multiple Sic Vectors Theory and Application in BIST Schemes

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Abstract: ***Test pattern generators are the vital blocks in Built-in self-test. In this paper a new approach which is multiple single input changes (MSIC) is used to generate the random patterns for applying it to CUT for testing applications. A reconfigurable Johnson counter and a scalable SIC counter are developed to generate a class of minimum transition sequences. The proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes. The generated patterns based on this approach are applied to the ISCAS benchmark designs. Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to TPG and TRA. Simulation results show the functionality of the pattern generator. The synthesis is carried out on XILINX ISE and the simulation is performed on the ISE simulator. The obtained test results are comparing with the primary one to demonstrate the target fault coverage.***
Index Terms—Built-in self-test (BIST), low power, single-input change (SIC), test pattern generator (TPG).

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, and power dissipation. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% P more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges. To reduce the power consumption generates the test vectors with less number of transitions. Generally the random sequence at the output of the flip-flops can be used as a test pattern. Flip-flop's connected in series with feedback taps defined by the generator polynomial. The seed value is loaded into the outputs of the flip-flops. The only input required to generate a random sequence is an external clock where each clock pulse can produce a unique pattern at the output of the flip-flops. This test pattern is run on the circuit under test for desired fault coverage. The number of inputs required by the circuit under test must match with the number of flip-flop outputs. The power consumed by the chip under test is a measure of the switching activity of the logic inside the chip which depends largely on the randomness of the applied input stimulus. Reduced correlation between the successive vectors of the applied stimulus into the circuit under test can result in much higher power consumption by the device than the budgeted power. A new low power pattern generation technique is implemented using a multiple single input change method.

A. Need for using BIST technique

Today's highly integrated multi-layer boards with fine-pitch ICs are virtually impossible to be accessed physically for testing. Traditional board test methods which include functional test, only accesses the board's primary I/Os, providing limited coverage and poor diagnostics for board-network fault. In circuit testing, another traditional test method works by physically accessing each wire on the board via costly "bed of nails" probes and testers. To identify reliable testing methods which will reduce the cost of test equipment, a research to verify each VLSI testing problems has been conducted. The major problems detected so far are as follows:

- Test generation problems
- Gate to I/O pin ratio

B. *Test Generation Problems*

The large number of gates in VLSI circuits has pushed computer automatic-test-generation times to weeks or months of computation. The numbers of test patterns are becoming too large to be handled by an external tester and this has

resulted in high computation costs and has outstripped reasonable available time for production testing.

C. The Gate to I/O Pin Ratio Problem

As ICs grow in gate counts, it is no longer true that most gate nodes are directly accessible by one of the pins on the package. This makes testing of internal nodes more difficult as they could neither no longer be easily controlled by signal from an input pin (controllability) nor easily observed at an output pin (observe ability). Pin counts go at a much slower rate than gate counts, which worsens the controllability and observe ability of internal gate nodes.

II. PROPOSED MSIC-TPG SCHEME

This section discuss about the introduction of MSIC and how the test patterns are generated using this scheme. First, the SIC vector is decompressed to its multiple code words. Meanwhile, the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

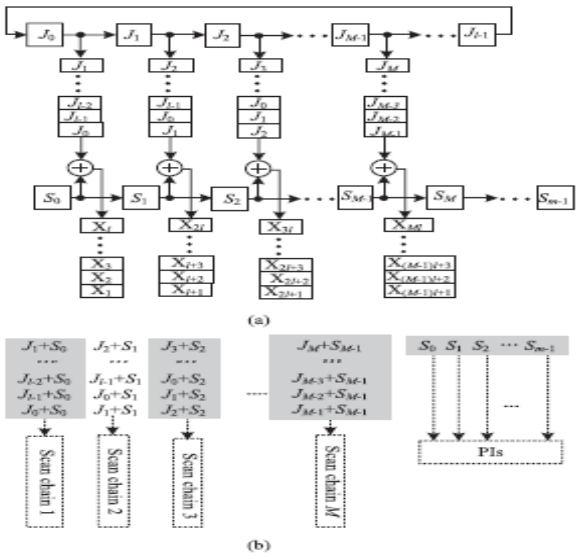


Fig.1(a) Symbolic simulation of an MSIC pattern for scan chains.
(b) Symbolic representation of an MSIC pattern.

A. Test Pattern Generation Method

Assume there are m primary inputs (PIs) and M scan chains in a full scan design, and each scan chain has l scan cells. Fig. 1(a) shows the symbolic simulation for one generated pattern. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as S(t) = S0(t)S1(t)S2(t), . . . , Sm−1(t) (hereinafter referred to as the seed), and the vector generated by an l-bit Johnson counter can be expressed as J (t) = J0(t)J1(t)J2(t), . . . , Jl−1(t).In the first clock cycle, J = J0 J1 J2, . . . , Jl−1 will bit-XOR with S = S0S1S2, . . . , SM−1, and the results X1Xl+1X2l+1, . . . , X(M−1)l+1 will be shifted into M scan chains, respectively. In the second clock cycle, J = J0 J1 J2, . . . , Jl−1 will be circularly shifted as J =Jl−1 J0 J1, . . . , Jl−2, which will also bit-XOR with the seed S = S0S1S2, . . . , SM−1. The resulting X2Xl+2X2l+2, . . . , X(M−1)l+2 will be shifted into M scan chains, respectively. After l clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed S0S1S2, . . . , Sm−1 will be applied to m PIs. Since the circular Johnson counter can generate l unique Johnson codewords through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Fig. 1 actually constitute a linear sequential decompressor.

B. Reconfigurable Johnson Counter

According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and

Johnson codewords, i.e., the reconfigurable Johnson counter and the scalable SIC counter.For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain.As shown in Fig. 2(a), it can operate in three modes.

1) Initialization: When RJ_Mode is set to 1 and Init is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l times.

2) Circular shift register mode: When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 l times.

3) Normal mode: When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate 2l unique SIC vectors by clocking CLK2 2l times.

C. Scalable SIC Counter

When the maximal scan chain length l is much larger than the scan chain number M, we develop an SIC counter named the "scalable SIC counter." As shown in Fig. 2(b), it contains a k-bit adder clocked by the rising SE signal, a k-bit subtractor clocked by test clock CLK2, an M-bit shift register clocked by test clock CLK2, and k multiplexers. The value of k is the integer of log2(l − M). The waveforms of the scalable SIC counter are shown in Fig. 2(c). The k-bit adder is clocked by the falling SE signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 2(b), it can operate in three modes.

1) If SE = 0, the count from the adder is stored to the k-bit subtractor. During SE = 1, the contents of the k-bit subtractor will be decreased from the stored count to all zeros gradually.

2) If SE = 1 and the contents of the k-bit subtractor are not all zeros, M-Johnson will be kept at logic 1 (0).

3) Otherwise, it will be kept at logic 0 (1). Thus, the needed 1s (0s) will be shifted into the M-bit shift register by clocking CLK2 l times, and unique Johnson codewords will be applied into different scan chains.

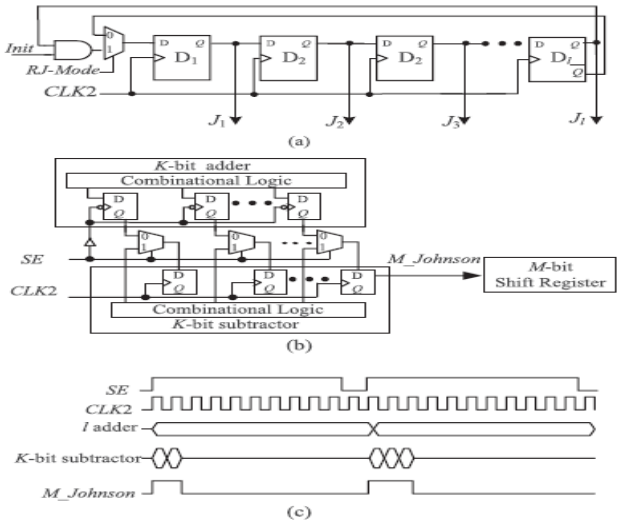


Fig.2. SIC generators. (a) Reconfigurable Johnson counter (b) Scalable SIC counter (c) Waveforms of the scalable SIC counter.

D. MSIC-TPGs for Test-per-Clock Schemes

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 3(a). The CUT's PIs X1 − Xmn are arranged as an n ×m SRAM-like grid structure. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed generator is an m-stage conventional LFSR, and

operates at low frequency CLK1. The test procedure is as follows.

1) The seed generator generates a new seed by clocking CLK1 one time.

2) The Johnson counter generates a new vector by clocking CLK2 one time.

3) Repeat 2 until 2l Johnson vectors are generated.

4) Repeat 1–3 until the expected fault coverage or test length is achieved.

E. MSIC-TPGs for Test-per-Scan Schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 3(b). The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is not smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter and their outputs are applied to M scan chains, respectively.

The outputs of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows.

1) The seed circuit generates a new seed by clocking CLK1 one time.

2) RJ_Mode is set to 0. The Reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.

3) After a new Johnson vector is generated, RJ_Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates l codewords by clocking CLK2 l times. Then, a capture operation is inserted.

4) Repeat 2–3 until 2l Johnson vectors are generated.
5) Repeat 1–4 until the expected fault coverage or test length is achieved.

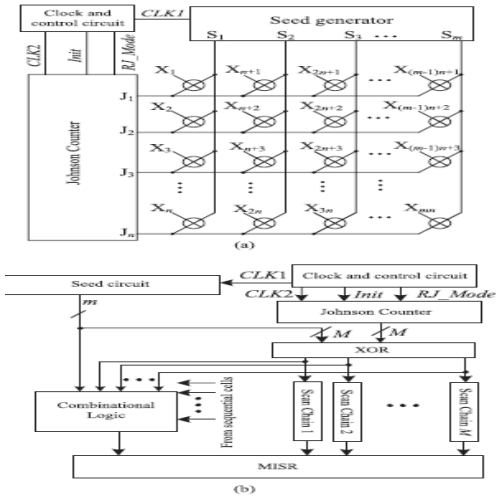


Fig 3. MSIC-TPGs for (a) test-per-clock and (b) test-per-scan schemes.

III. STRATEGY DESCRIPTION

The MSIC Test pattern generator architecture internally consists of a control circuit, seed circuit, SIC counter, scan chain and MISR modules. Here the control unit is used to initiate the seed value and enable the counter and to control the scan design. CUT is the circuit or chip in which we are going to apply BIST for testing stuck at zero or stuck at one error. Tapping can be taken according to the specification but as per taping change the TPG output generate will also change and as we change in number of flip-flop the

probability of repetition of random number will reduce. The initial value loading to the TPG is known as seed value.

A. Classification of test strategies

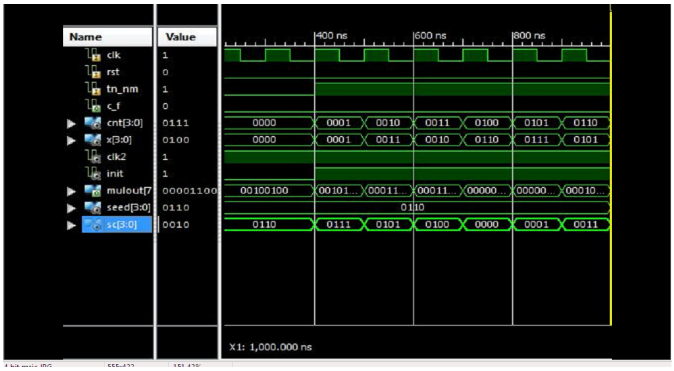
1) Weighted Pseudorandom Testing: In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudorandom testing. Thus, the test length can be effectively shortened.
2) Pseudo exhaustive Testing: Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flaws within the sub circuits can be detected. However, such a method involves extra design effort to partition the circuits and deliver the test patterns and test responses. BIST is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. BIST is the commonly used design technique for self testing of circuits.
3) Pseudorandom Testing: Pseudorandom testing involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order. The test length and the contents of the patterns are used to impart fault coverage.
4) Exhaustive Testing: Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT). It guarantees that all detectable faults that divert from the sequential behavior will be detected. The strategies are often applied to complex and well isolated small modules such as PLAs.
5) Stored Patterns: Stored-pattern approach tracks the pre generated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self test of a computer and microprocessor functional testing using micro programs.

BIST is a design for testability (DFT) technique in which testing is carried out using built –in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR).A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks.The circuit introduces more switching activities in the circuit under test (CUT)during test than that during normal operation[5].It causes excessive power dissipation and results in delay penalty into the design[6].

Using BIST Technique the portability can be achieved very easily than the Automatic Test pattern generator. Generally the Automatic Test pattern generators are used externally while a BIST uses internally. Due to advantages of BIST the concept of ATPG is vanishes but it also has its own advantages.

IV. RESULTS

WAVEFORM FOR 4BIT MISC



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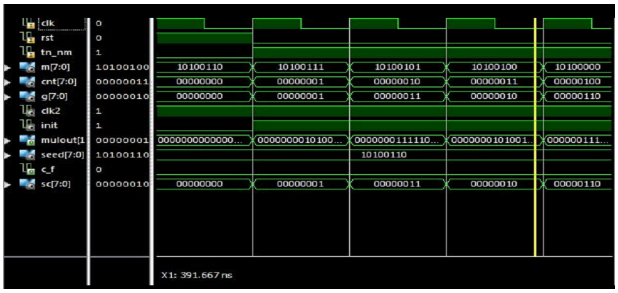
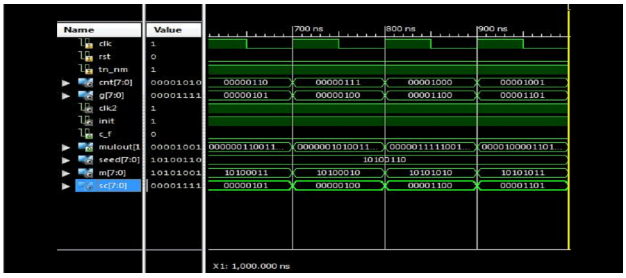
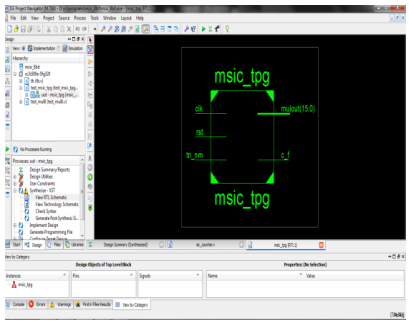
WAVEFORM FOR 8 BIT LOW POWER LFSR



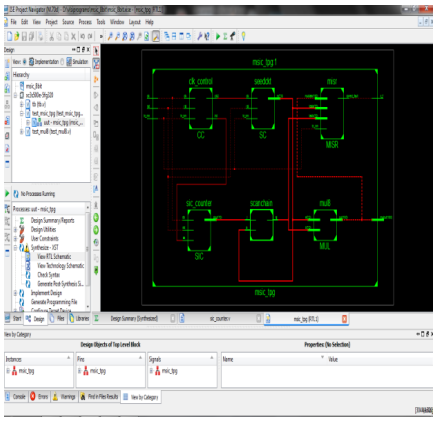
WAVEFORM FOR 8 BIT MSIC



Schematics



RTL Schematics:



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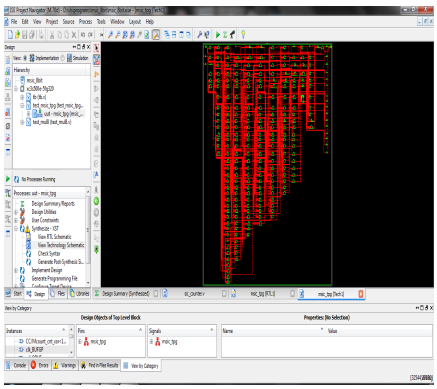
Technology schematics:



V. CONCLUSION

The proposed approach shows the concept of reducing the transitions in the test pattern generated. The transition is reduced by increasing the correlation between the successive bits. The simulation results shows that how the patterns are generated for the applied seed vector. This paper presents the implementation of MSIC approach based pattern generator with regard to verilog language. Synthesizing and implementation (i.e. Translate, Map and Place and Route) of the code is carried out on Xilinx - Project Navigator, ISE suite. The power reports shows that the proposed low power lfsr consumes less power during testing by taking the benchmark circuit. In future there is a chance to reduce the power somewhat more by doing modifications in the proposed architecture.

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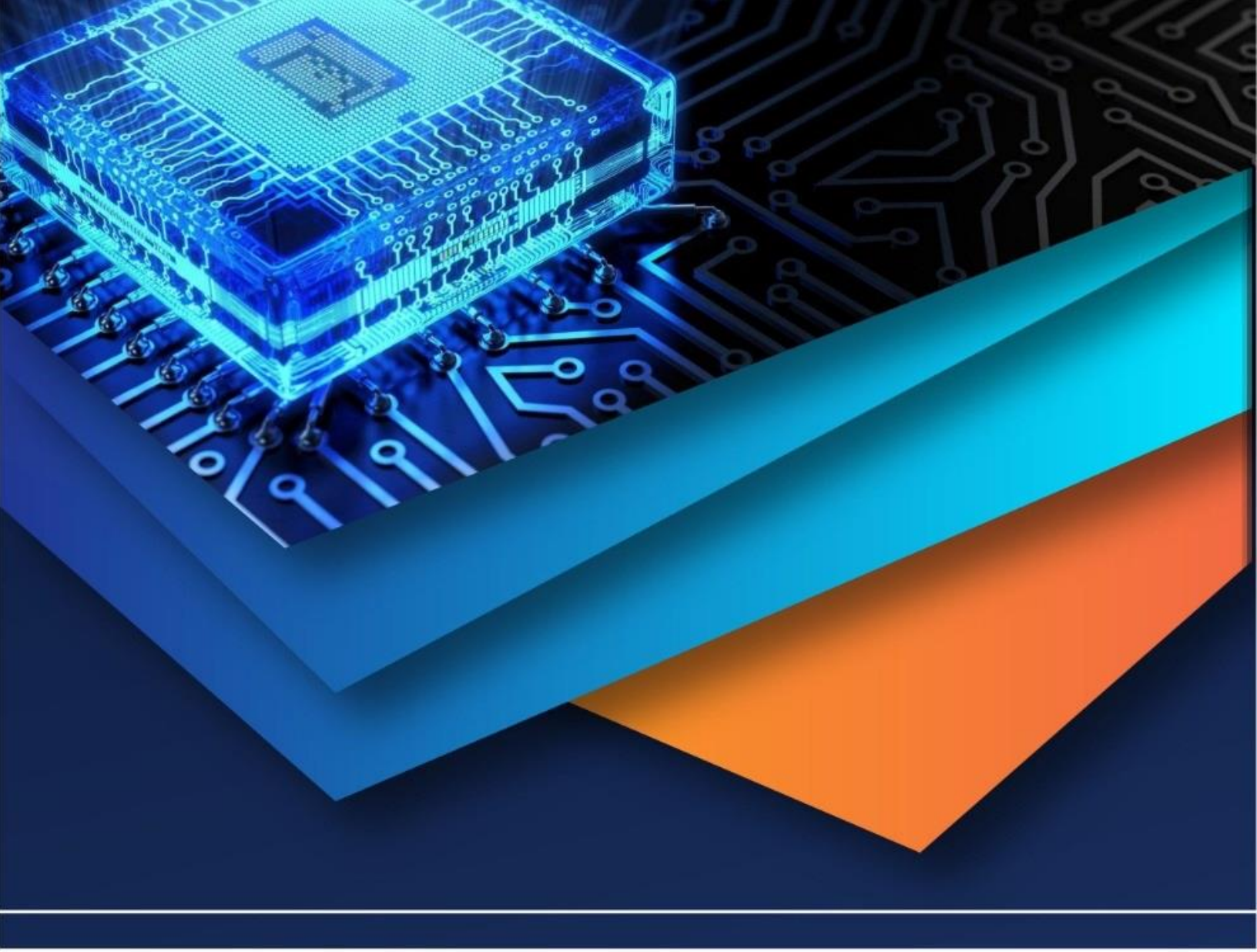

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