iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 2 **Issue:** Issue- III **Month of publication:** November 2014

DOI:

www.ijraset.com

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Special Issue-3, November 2014
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

A Design of FPGA with LEDR encoding and dual rail Architecture

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Abstract: ***This project proposed design of asynchronous FPGAs presented with power optimization techniques. The important challenge in IC industry is low power consumption, low cost, better timing. Asynchronous FPGAs having advantage is low power consumption. Proposing two techniques here to reduce power consumption, one is fine grain power gating and reducing the dynamic power by using the level encoding dual rail (LEDR) architecture. Generally power consumptions are two types, static and dynamic. If consider fine grain power gating it consists of sleep resistor and a controller. When a lookup table is inactive, it automatically goes to sleep mode. LEDR encoding is used to data flow at the input and output of FPGAs.***

Keywords: LEDR, FPGA, lookup table.

I. INTRODUCTION

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). Contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA designs employ very fast I/Os and bidirectional data buses it becomes a challenge to verify correct timing of valid data within setup time and hold time. Floor planning enables resources allocation within FPGA to meet these time constraints. FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design[1]and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications.[2] On the other hand, FPGAs are cost-effective and flexible since FPGAs consist of programmable logic blocks and pro-gram able switch blocks to make design modifications after production. The major disadvantage of FPGAs is its low perfor-mance because of the following reasons.

1. The area and delay of a switch block become large for a switch block consists of many programmable switches.
2. The time for data transfer between logic blocks becomes large since data from one logic block usually traverse through FPGAs are programmable, so they allow product differentiation. Selecting an appropriate FPGA architecture is critical in achieving the best static and dynamic power consumption. Flash-based FPGAs by Micro semi are the low-power leaders in the industry. In addition to utilizing the low-power attributes of flash-based FPGAs, you can deploy several design techniques to further reduce overall power. The important FPGA power components to consider in

The following sections: Power-up (inrush power): Inrush power is the amount of power drawn by the device during power-up. And Configuration power: Configuration power is the amount of power required during the loading of the FPGA upon power-up (specifically to SRAM-based programmable logic devices).

II. FINE GRAIN POWER GATING

Overcome the problems of coarse grain power gating; we introduce the Fine grain power gating technique. In fine grain power gating technique each lookup table having own sleep controller and related to sleep transistor, so any of the lookup table active states all other lookup tables are going to sleep state [l]. In this paper reduce the both standby power and dynamic power. Asynchronous Architecture Design The asynchronous architecture, it detects the activity of a power gated domain. The activities are: 1) To determine Logic block is standby state, when sleep state & when Active state. 2) It compares the phase of the input data and Output data 3) It determines the function of lookup table. Dynamic power, reducing purpose introduce dual rail encoding

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(existing) [2] and level encoding dual rail (proposed) architecture. Standby power, reducing purpose introduced autonomous fine grain power gating technique.

III. DUAL RAIL ENCODING

They use four-phase dual-rail encoding because of relatively small hardware cost. In four-phase dual-rail encoding, a spacer must be inserted between two consecutive valid data Values. This results in low throughput and high dynamic power consumption because of the large number of signal transitions.

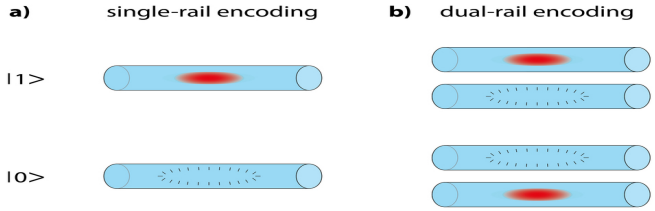

Fig 1.0 Dual and single rail encoding

IV. FPGA

Field Programmable Gate Arrays are two dimensional arrays of logic blocks and flip-flops with an electrically programmable interconnection between logic blocks. The interconnections consist of electrically programmable switches which is why FPGA differs from Custom ICs, as Custom IC is programmed using integrated circuit fabrication technology to form metal interconnections between logic blocks. In an FPGA logic blocks are implemented using multiple level low fan-in gates, which gives it a more compact design compared to an implementation with two-level AND-OR logic. FPGA provides its user a way to configure:

1. The intersection between the logic blocks and
2. The function of each logic block.

Logic block of an FPGA can be configured in such a way that it can provide functionality as simple as that of transistor or as complex as that of a microprocessor. It can used to implement different combinations of combinational and sequential logic functions. Logic blocks of an FPGA can be implemented by any of the following:

1. Transistor pairs
2. Combinational gates like basic NAND gates or XOR gates
3. n-input Lookup tables
4. Multiplexers
5. Wide fan-in And-OR structure.

Routing in FPGAs consists of wire segments of varying lengths which can be interconnected via electrically programmable switches. Density of logic block used in an FPGA depends on length and number of wire segments used for routing. Number of segments used for interconnection typically is a tradeoff between density of logic blocks used and amount of area used up for routing. The ability to reconfigure functionality to be implemented on a chip gives a unique advantage to designer who designs his system on an FPGA It reduces the time to market and significantly reduces the cost of production.

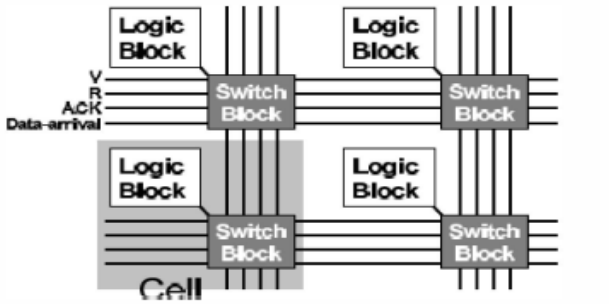

Fig 2.0 FPGA architecture

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V. LEDR ENCODING DESIGN

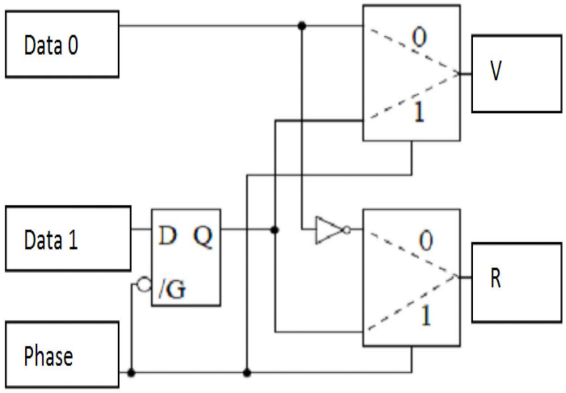
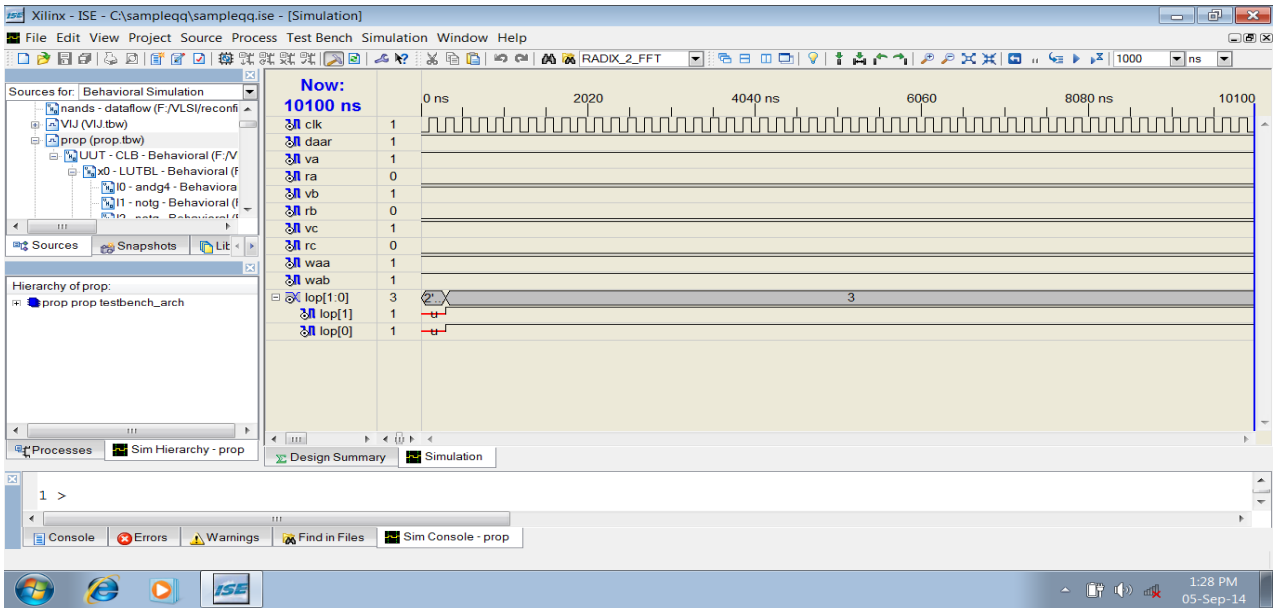


Fig 3.0 Architecture of LEDR

This architecture operation based on data's and phase signal. The D latch signal given to selectors and selectors produce the output of level encoding signal. In LEDR encoding, no spacer is required. Table 1 shows the code table of LEDR encoding. In LEDR encoding, each data value has two types of code words with different phases. Above example shows the data values "0,""0," and " 1" are transferred. The main feature is that the sender sends data values alternately in phase 0 and phase 1. Because no spacer is required, the number of signal transitions is half of four phase dual-rail encoding. As a result, the throughput is high and the power consumption is small. Based on this observation, in the proposed FPGA, LEDR encoding is employed for implementing the asynchronous architecture to reduce the dynamic power.

V. FULL ADDER SIMULATION RESULT

The full adder logic block in the full adder circuit there are two Xor gate and two AND gate and one OR gate are used to perform the full adder. The corresponding logic blocks are active state all other logic blocks are sleep state. The first logic block worked on Xor gate that time the same logic block generate the sleep signal is zero. The output of the first logic block and third input given to the next logic block that time the second logic block worked on Xor operation and sleep signal is one its given to the third logic block, so the third logic block goes to sleep state



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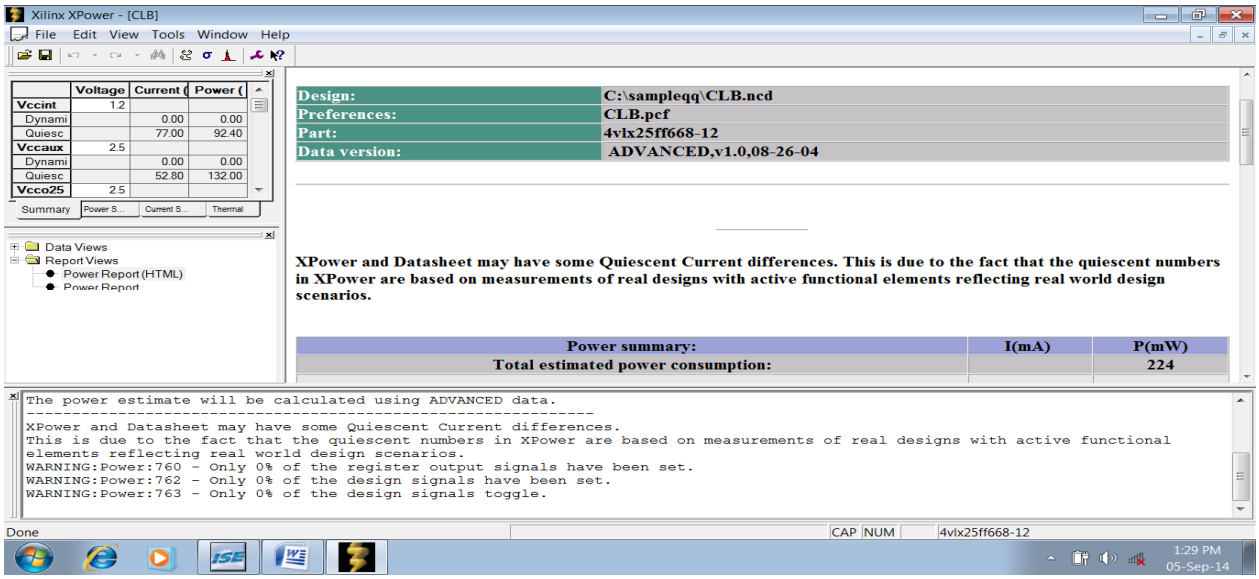
VI. POWER REPORT



VII. CONCLUSION

This paper consists of an autonomous fine-grain power gating with small overheads of an asynchronous FPGA architecture has been developed and analyzed. The implementation of the FPGA has been done efficiently using the standby power to wake up the Logic block before the data arrives and power OFF the Logic block only when the data does not come for quite a while. As a result, the wake-up time has been reduced. Since their data paths change dynamically and frequently, it is more difficult than FPGAs to determine the transistors for each Logic block using offline analysis. The power analysis also has been carried out and it has been found that using the proposed fine-grain power gating method, the FPGA consumes 7 m W powers

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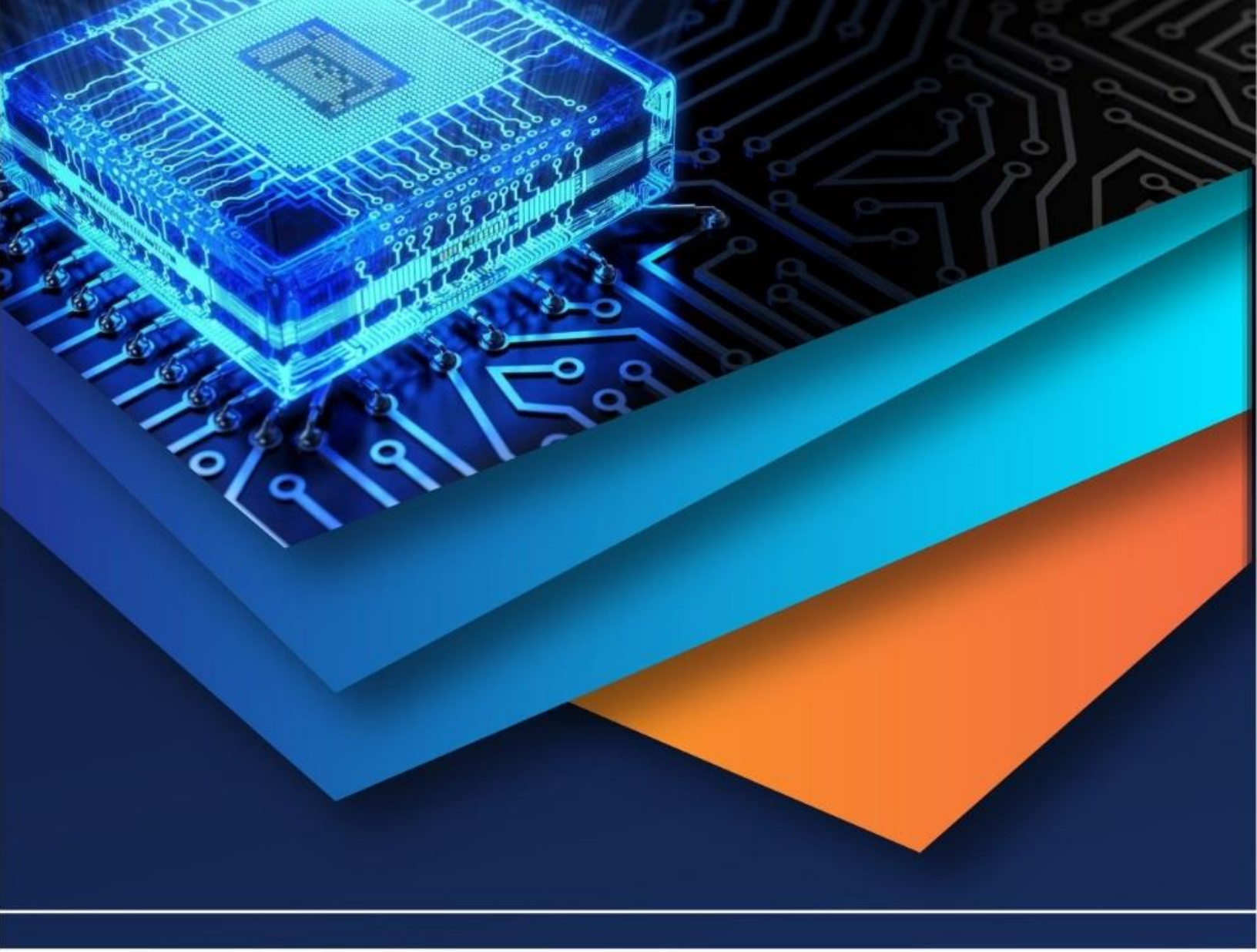

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