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Design of Digital FIR Filter using Modified MAC Unit

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Abstract*: Finite impulse response (FIR) filter is one of the important components in any DSP and communication systems. The output from the DSP processor is depends on the FIR filter, so need an efficient FIR filter design, to achieve an efficient output. Filter architecture contains many components; one of the main components is multiplier. Different types of multipliers are available in the digital circuits, but need an efficient multiplier design to get efficient filters. Wallace tree multiplier was designed and implemented using verilog HDL. This multiplier needs many gates to implement the design. So it takes more area and delay. To reduce the drawbacks, to propose a new efficient multiplier named as Birecoder multiplier. It is one of the best multiplier in the digital circuit design. This multiplier overcomes the existing multiplier drawbacks. Multiplier is designed by verilogHDL, after the design Wallace tree multiplier is compared with Birecoder, and analyzes the performance of the multiplier.
Keywords*: FIR Filter, DSP Processor, Verilog HDL, Wallace Tree Multiplier, Xilinx ISE, Bi-Recoder.

I. INTRODUCTION

One of the most extensively used functions executed in DSP is Finite Impulse Response (FIR) filtering. In several applications, in order to attain high spectral suppression and noise reduction, FIR filters are used. A lot of prior efforts for decreasing power consumption of FIR filter usually focus on the miniaturization of the filter coefficients whereas maintaining a fixed filter order. FIR filter structures are simplified to minimizing the number additions, subtractions and add & shift operations. Though, one of the problems encountered is that one time the filter architecture is determined, the coefficients cannot be altered; consequently, those are not appropriate to FIR filter with programmable coefficients.

A. Finite Impulse Response

Finite impulse response (FIR) filter is one of the important components in any DSP and communication systems. The output from the DSP processor is depends on the FIR filter, so need an efficient FIR filter design, to achieve an efficient output. Filter architecture contains many components; one of the main components is multiplier. Different types of multipliers are available in the digital circuits, but need an efficient multiplier design to get efficient filters

B. Very Large Scale Integration

Very Large Scale Integration (VLSI) is the process integrating thousands of transistors into a single chip. The major concerns of the VLSI design were area, performance and power. In the past, the designers were directed towards increasing the speed of the digital system; hence the present day technologies posses computing capabilities that make possible personal work stations, sophisticated computer graphics and multi-media capabilities such as real time speech recognition and real time video.

C. *Digital Signal Processing*

Digital signal processing (DSP) is the use of digital processing, such as by computers, to perform a wide variety of signal processing operations. The signals processed in this manner are a sequence of numbers that represent samples of a continuous variable in a domain such as time, space, or frequency. Digital signal processing and analog signal processing are subfields of signal processing. DSP applications include audio and speech signal processing, sonar, radar and other sensor array processing, spectral estimation, statistical signal processing, digital image processing, signal processing for telecommunications, control of systems ,biomedical engineering, sesmic data processing, among others.

D. XILINX ISE

The Integrated Software Environment (ISE) is the Xilinx design software suite that allows us to take our design from design entry through Xilinx device programming. The ISE Project Navigator manages and processes our design through the following steps in

the ISE design flow. The Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly- coupled to the architecture of chips. The Xilinx ISE is primarily used for circuit synthesis and design, while the modelism logic simulator is used for system level testing. The Xilinx ISE system is an integrated design environment that that consists of a set of programs to create (capture), simulate and implement digital designs in a FPGA or CPLD target device.

II. WALLACE TREE MULTIPLIER

The block diagram of Wallace tree multiplier is shown below in the figure 1.

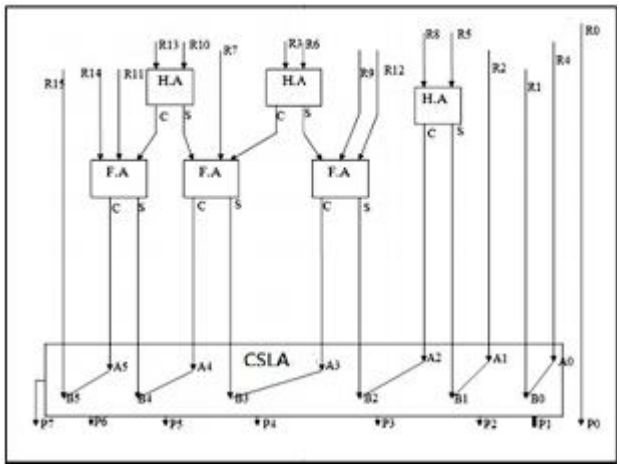

Fig. 1 Wallace Tree Multiplier

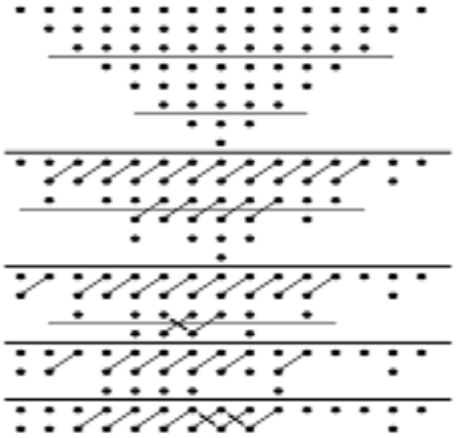

Fig. 2 Example of Wallace tree reduction

A. The Wallace tree has three steps:

1) Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding results.

2) Depending on position of the multiplied bits, the wires carry different weights.

3) Group the wires in two numbers, and add them with a conventional adder.

Wallace multiplier uses full adders and half adders to reduce the partial product tree to two rows, and then a final adder is used to add these two rows of partial products. The final adder that is used in the Wallace tree multiplier is Carry select adder the diagram of reduction of wallace tree is show below in the figure 2.

III. MAC BI-RECODER MULTIPLIER

In this paper, uses the Multiply and Accumulate (MAC) bi-recoder multiplier and the final stage of the addition is done by Square Root Carry Select adder (SRCSA). In order to overcome the disadvantages, such that the Area(LUT and Slice) ,delay Finite Impulse Response (FIR) filter is used to filter the noise/unwanted signals at finite impulse durations.

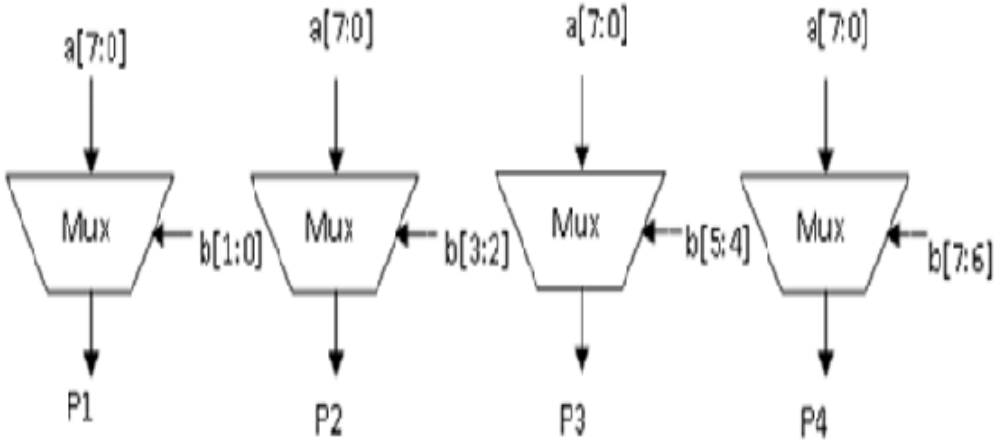

Fig. 3 Bi-Recoder Multiplier

B. Bi-Recoder Based Fir Filter

Finite Impulse Response (FIR) filter is considered for improving the performance of digital filtering process in wireless communication technology. Large endeavours have been worked on direct form digital FIR filter to improve the performance in terms of high speed and throughput. The relationship of input- output of Linear Time Invariant (LTI) System is represented as in equation,

$$yout(n) = \sum Coeff\ p\ Xin\ (n - 1)$$

Where, xin(n) represents the input samples of FIR filter, yout(n) represents the output samples of FIR filter, N is the order of the filter or length of the filter, Coeff denotes the coefficient of filter

Impulse response of FIR filter must be finite and therefore, Periodical multiplication and accumulation structures are used to maintain the impulse response of FIR filter as finite.

C. Square Root Carry Select Adder(Srcsa)

In figure 4.SRCSA is one of the best VLSI based adders, because it utilizes less hardware complexity and high speed. The combination of Ripple Carry Adder (RCA) and Binary to Excess1 Conversion (BEC) unit is to reduce the propagation delay of addition process. In SRCSA, N-bit data can be divided into √N groups for performing parallel addition process. Reduced complexity Wallace multiplier is developed for the design of digital FIR filter..

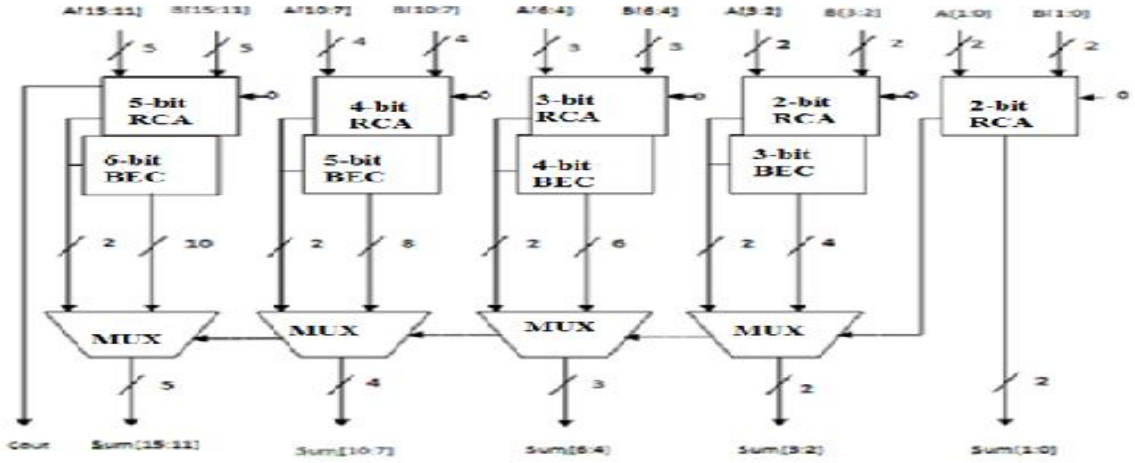

Fig.4 Square root carry select adder

RCA circuits of SRCSA reduce the performance in terms of speed. Hence, one set of RCA circuits is replaced by BEC circuits (have same functionality with less number of gates) to increase the speed of the adder significantly. The circuit diagram of 16-bit BEC based SRCSA circuit is illustrated in the figure 5. Every group structures have RCA, BEC and Multiplexer circuits.

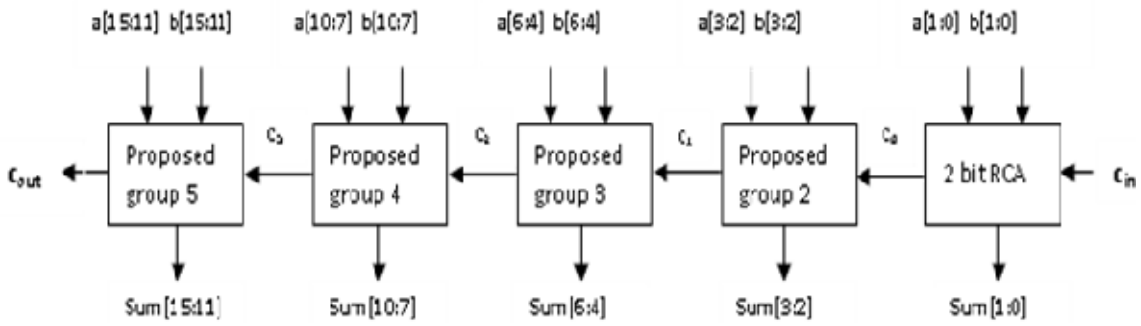

Fig.5 16-bit BEC based square root carry select adder

IV. RESULTS

A. Wallace Tree Multiplier:

The simulation output of the Wallace tree multiplier is shown in the figure 8. and this shows the overall performance of the Wallace tree multiplier.

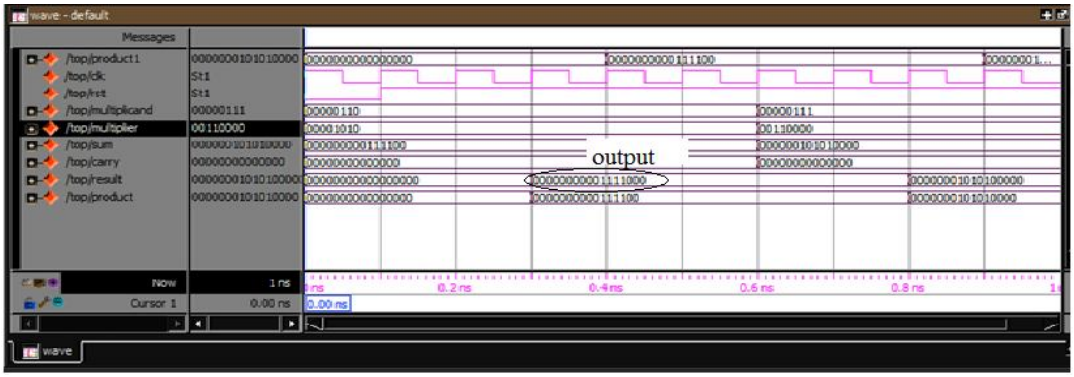

Fig.6 Simulation output of Wallace tree multiplier.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	45	3,840	1%	
Number of 4 input LUTs	144	3,840	3%	
Logic Distribution				
Number of occupied Slices	94	1,920	4%	
Number of Slices containing only related logic	94	94	100%	
Number of Slices containing unrelated logic	0	94	0%	
Total Number of 4 input LUTs	144	3,840	3%	
Number of bonded IOBs	34	141	24%	
Number of BUFGMUXs	1	8	12%	

Table.1 Area of Wallace tree multiplier

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.288	1	---	---
Logic	0.000	144	3840	3.8
Signals	0.027	191	---	---
IOs	0.130	34	141	24.1
Total Quiescent Power	0.116			
Total Dynamic Power	0.778			
Total Power	0.894			

Table .2 Power consumption of Wallace tree multiplier

B. Bi-recoder Multiplier

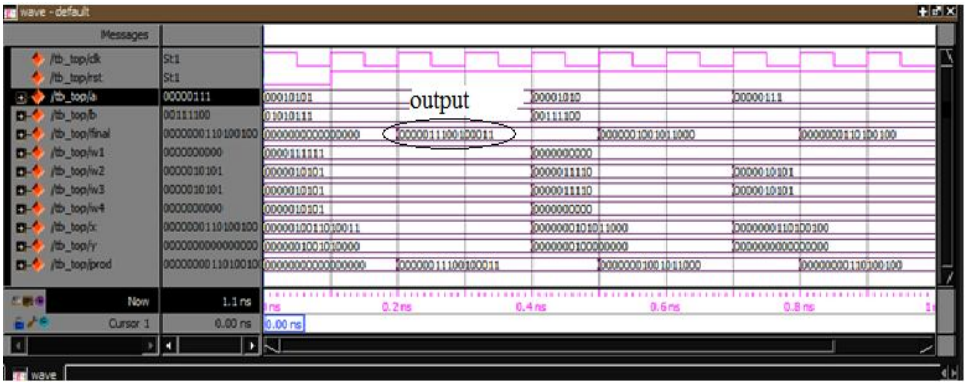

Fig.7 Simulation output of Bi-recoder multiplier

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	130	3,840	3%	
Logic Distribution				
Number of occupied Slices	72	1,920	3%	
Number of Slices containing only related logic	72	72	100%	
Number of Slices containing unrelated logic	0	72	0%	
Total Number of 4 input LUTs	130	3,840	3%	
Number of bonded IOBs	34	141	24%	
IOB Flip Flops	16			
Number of BUFGMUXs	1	8	12%	

Table .3 Area of Bi-recoder multiplier

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.084	1	---	---
Logic	0.001	130	3840	3.4
Signals	0.004	128	---	---
IOs	0.494	34	141	24.1
Total Quiescent Power	**0.043**			
Total Dynamic Power	**0.702**			
Total Power	**0.746**			

Table.4 Power consumption of Bi-recoder multiplier

C. Comparison Between The wallace Tree And Birecoder Multiplier

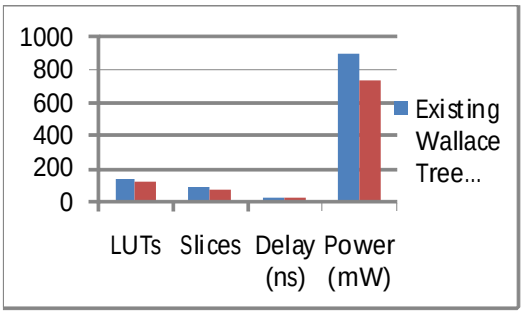

Fig. 8 Comparison between the Wallace tree and birecoder multiplier

V. CONCLUSION

This paper presents a Bi-Recoder multiplier with help of multiplexer. This reduces N rows of partial products into N/2 rows of partial products with slight increase in bit-lengths. Due to lesser number of partial products, the number of adders used to make partial product addition is also less. It reduces slices by 6% and LUT by 7% compared to Wallace tree multiplier. Power consumption of Bi-Recoder multiplier reduces up to 60% than Wallace tree multiplier.

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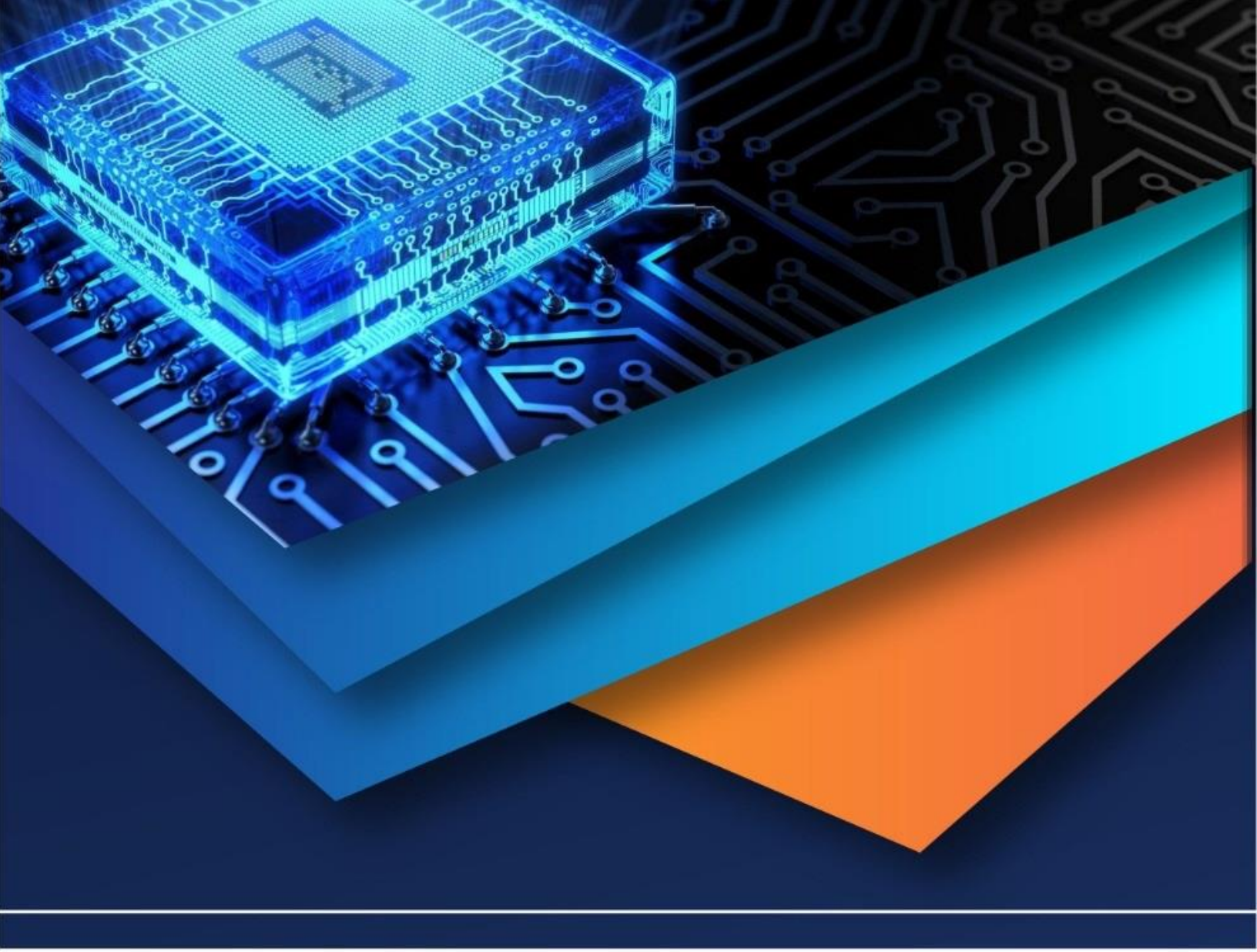

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