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# Transformer less MOSFET Inverter for Single Phase Drive and Grid-Tied Photovoltaic System

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***Abstract:*** ***The grid tied photovoltaic system suffers a great loss because the performance of the transformer present in the inverter. The cost of the transformer is high and the maintaince cost is also high. Therefore transformer less inverter are widely used in grid tied photovoltaic system, due to the benefits of achieving high efficiency and low cost. The sinusoidal pulse width modulation of full bridge transformer less inverters can achieve high efficiency by using metal oxide semiconductor field effect transistor. Various topology has been implemented for transformer less inverter, but in that there is a problem of losses and reverse recovery characteristics. In our paper we are going to implement the centre tapped H bridge transformer less inverter topology for grid tied photovoltaic system to avoid the losses and leakage current. A clamped branch is added in the transformer less inverter. The added clamping branch clamps the freewheeling voltage at the freewheeling period. As the common mode voltage is kept constant for the whole grid period that reduces the leakage current. The splitting structure of inductor at the region of grid side avoids reverse recovery voltage and this improves the efficiency of the system. The detailed analysis of our topology with the operational modes, leakage current analysis and design consideration were implemented and the proposed inverter is applied for single phase induction motor.***

***Keywords: common mode voltage, inverter, Photovoltaic (PV) grid-connected system, PWM control, transformerless, leakage current.***

## I. INTRODUCTION

Transformer less inverters are widely used in grid-tied photovoltaic (PV) generation systems, due to The benefits of achieving high efficiency and low cost. Various transformer less inverter topologies have been Proposed to meet the safety requirement of leakage currents, when no transformer is used in a grid connected Photovoltaic system, a galvanic connection between the grid and PV array exists. In these conditions, dangerous Leakage currents (common-mode currents) can appear through the stray capacitance between the PV array and the ground. In order to avoid these leakage currents, different inverter topologies that generate no varying common-mode voltages have been proposed.

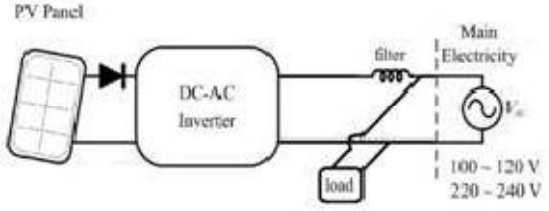
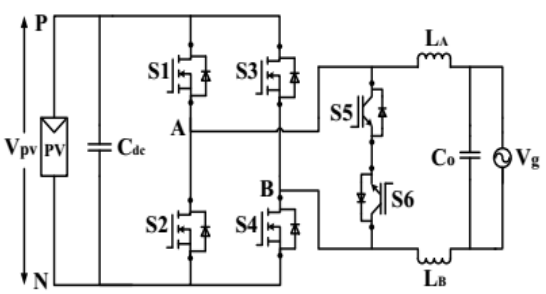



Fig.1Schematic diagram of PV panel connected to Grid connected loads

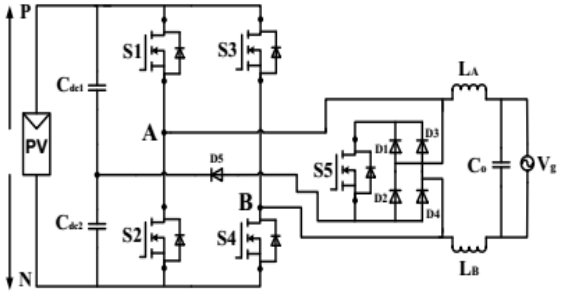
The CM voltage needs to be clamped to the mid-point of dc input voltage instead of only disconnecting the PV module from the grid. On the other hand, to improve the efficiency, transformer less inverter can be implemented using super-junction MOSFET and SiC diodes. The super-junction MOSFETs can avoid the fixed voltage drop and turn-off losses caused by tail current, thereby reducing the conduction and switching losses.

However, due to poor reverse recovery of MOSFETs slow body-diode, it is limited to use in transformer less inverter. In the following, MOSFET based transformer less topologies for grid-tied PV application will be reviewed and discussed based on their circuit structure, efficiency and CM voltage clamping capability.

The most attractive transformer less topology is the Highly Efficient and Reliable Inverter Concept (HERIC) to pology which is shown in Fig.1(a). This topology has been implemented in some commercial inverters, especially those from Sunway's converter. Two switches are added in the ac side of full-bridge (FB) topology to decouple the PVmodule from the grid during the freewheeling period. Though the PV module is decoupled from the grid, a fluctuating CM voltage could be observed because the freewheeling path potential is not clamped at the half of dcinput voltage. As seen in Fig.1(b), the topology which has been proposed in [10] replaces the two switches freewheeling branch with one bi-directional switch and four diodes called H-bridge zero voltage rectifier (HB-ZVR) topology. Also, another diode (D5) has been added for better eliminating the leakage current. The clamping function of this topology has been done using D5 which allows one-directional clamping, only if the freewheeling path potential (VAN≈VBN) is higher than the dc link mid-point voltage. As a result, CM voltage fluctuation could be observed when the reverse condition is occurred which is very less than HERIC topology. In these two topologies, the grid current flows through two switches during the whole grid period; as a result, conduction loss is low.




(a)

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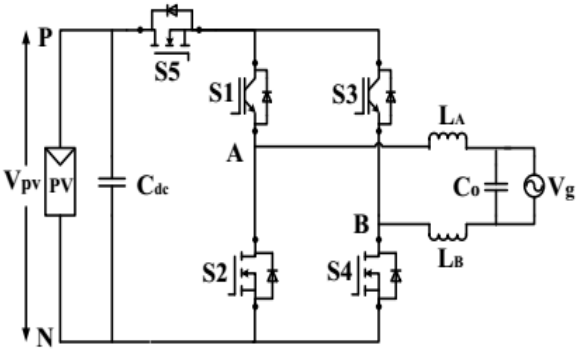


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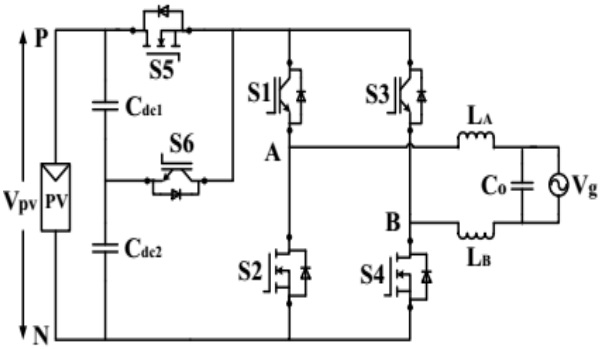


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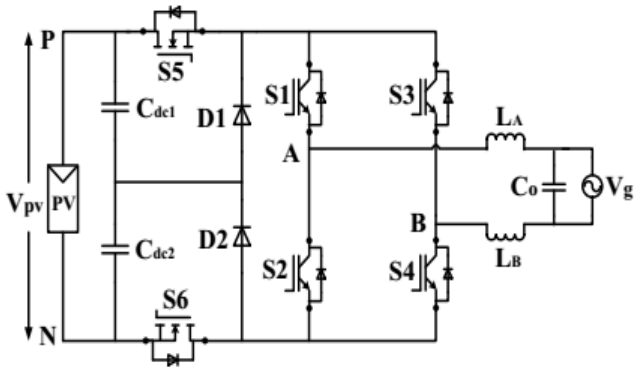


(e)

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Fig.1. Some existing MOSFET based transformer less topologies for grid tied PV application: (a) HERIC topology proposed in [12] (b) HB-ZVR topology proposed in [10] (c) H5 topology proposed in 157] (d) oH5 topology proposed in [9] (e) H6 topology[20]

Fig.1(c) shows another explicit transformer less topology proposed called H5 topology, made up by adding anextra switch in the dc side of FB inverter. In this topology, the freewheeling current flows through $S_1$ and body diode of $S_3$during positive half cycle, and $S_3$ and body diode of $S_1$ during negative half cycle. As a result, the switches S1 and S3 could not be implemented with MOSFETs due to the low reverse recovery of the MOSFET body diode. Another disadvantage isthat the output current flows through three switches in the active mode for the complete grid cycle, thus higher conduction losses are present. A fluctuating CM voltage couldalso be observed because the freewheeling path potential isnot clamped at the mid-point of dc link. An extension of H5topology is presented called optimized H5 (oH5)topology, where an extra switch (S6) has been added with theH5 topology to clamp the CM voltage at the half of input voltage as demonstrated in Fig.3.1(d). Unfortunately, a dead time must have to be added between the gate signals of the switches S5 and S6 to avoid the short circuit of the input split capacitor Cdc1. As a result, CM voltage fluctuates in dead time[9]. Another disadvantage of this topology is that higher conduction losses still remain due to the grid current flows through three switches in the active mode. Gonzalez et al. proposed another topology in [16] called full-bridge with dcbypass (FB-DCBP) which is also named as H6 topology. Item ploys two switches and two diodes in the dc side of FB inverter. The CM characteristics of this topology are better than other topologies because of the bi-directional clamping branch. During freewheeling mode, either diode D1 or D2 can be conducted based on whether the freewheeling pathpotential (VAN≈VBN) is higher or lower than half of the dc link voltage. In this topology, leakage current removal effect depends only on the turn-on speed of the clamping diodes. However, this topology can be implemented with two MOSFET switches (S5 & S6) only. In addition, the grid current flows through four switches, thus higher conduction losses are also present.

Considering the advantages and the drawbacks of the transformer less inverter mentioned earlier, a family of new transformer less topologies for single-phase grid-tied PV system is proposed based on two asymmetric phase legs in this work. The key features of the proposed inverter are: (1)no dead time is required because the switches in the same phase-leg are never all turned-on during the same SPWM cycle; as a result, current distortion at output is lower, (2) the CM voltage is kept constant at the half of dc input voltage because of the added clamping branch, (3) during the positive and negative half cycle, the inductor current flows throughtwo and three switches respectively, thus the conduction lossis lower. The detailed operation principles and the control scheme to reduce the dc current injection are described. An investigation has been conducted to calculate the device power losses and to make a detail comparison with thetopologies presented in Fig.1.

## II. PROPOSED TOPOLOGY AND MODULATION STRATEGY

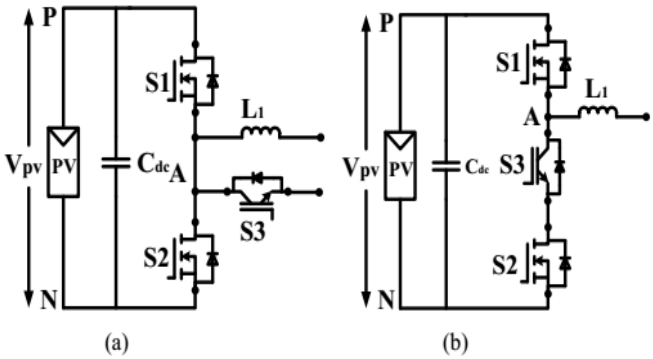
### *A. Derivation method of the proposed topology*

The traditional MOSFET based phase legs of transformerless inverter are shown in Fig.2 (a) & (b). In orderto ensure high efficiency, a modification is made in Fig.2(a)& (b) by replacing IGBTs with MOSFETs and diodes whichis shown in Fig.2(c) & (d). By combining these two phaselegs, a family of new transformerless topologies is derived based on the ac decoupling and asymmetric phase legs. The followings are the derivation steps of the proposed new topologies:

First, IGBT switches of the HERIC and H5 methods are replaced with MOSFETs and diodes to boost the efficiency.

Next, combine these two phase legs to derive newtopology. By changing the position of the free wheelings witches (S3 & D1), the family of the new topologiesis derived.

Finally, to clamp the CM voltage at the half of the dcinput voltage, a clamping branch consisting of a switch and a diode with a capacitor divider is introduced.



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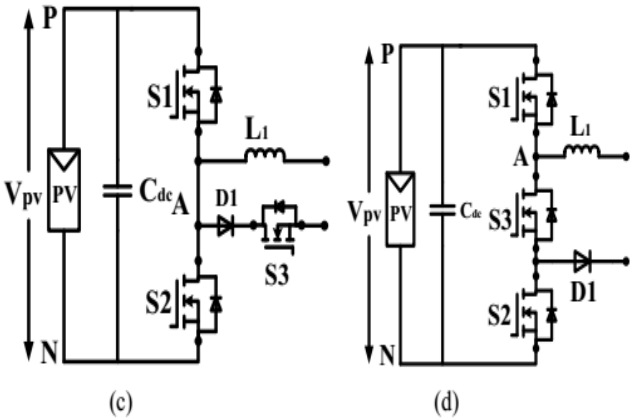


Fig..2. MOSFET based phase legs for transformerless inverter: (a) HERIC method (b) H5 method (c) modification of HERIC method (d) modification ofH5 method

*B. Circuit Configuration*

The family of the proposed transformer less PV inverter topology is depicted in Fig..3 which is derived according tothe derivation method described in the prior section, where S1,S2, S4, & S5 are high frequency switches, and S3 & S6 arelow frequency freewheeling switches. The unidirectional clamping branch is constructed using switch S7 and diode D3with a capacitor divider (Cdc1 & Cdc2) which clamps the CMvoltage at the midpoint of dc link. LA, LB, and Co make up the LC type filter connected to the grid and Vpv represent the input dc voltage. The unipolar SPWM can be employed to the proposed topology with three-level output voltage. The MOSFET power switches are utilized as no reverse-recovery issues are required for the proposed configuration of the inverter for unity power factor operation. Consequently, the efficiency of the entire PV system is increased.

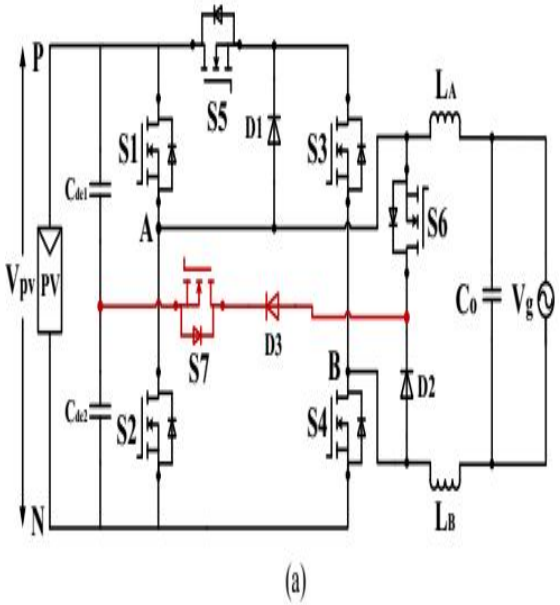


Fig...3. The family of the proposed transformerless grid connected PV inverter topologies: (a) circuit structure A

*C. Operating Principle*

In order to analysis and verify, the circuit structure A is taken as an example. Fig.4 shows the switching pattern forunity power factor operation, where the G1, G2, G3, G4, G5,G6, and G7 are the gate signals of the switches S1, S2, S3, S4,S5, S6, and S7. As can be seen, (S1, S4) and (S2, S5)commutate at the switching frequency with the identical commutation order in the positive and negative half cycle of the grid current, respectively. In Fig.3.5, the operating principles of the proposed topology are shown. Four operation modes are proposed to generate the output voltage state of+VPV, 0, and -VPV, which can be explained as follows:

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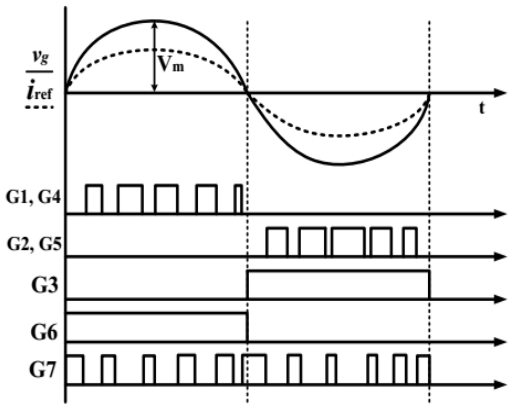



Fig.4. Gate drive signals of the proposed topology for circuit structure A

Mode 1 is the active mode in the positive half cycle ofthe grid current. When S1 and S4 are turned-on, the inductor current iL increases linearly through grid. In this mode, VAN = VPV and VBN = 0, thus VAB = VPV and the inductor current:

$$i_L(t) = \frac{V_{PV} - v_g}{L}(t) \quad (1)$$

Mode 2 is the freewheeling mode in the positive half cycle of the grid current, as indicated in Fig.5(b). The inductor current iL flows through S6 and D2, and reduces linearly under the effect of grid voltage. In this state, VAN falls and VBN rises until their values are equal. If the voltages (VAN≈VBN) are higher than half of the dc link voltage, freewheeling current flows through S7 and D3 to the mid-point of the dc link, results VAN and VBN are clamped at VPV/2. Therefore, at mode 2, VAN = VPV/2,VBN= VPV/2, the inverter output voltage VAB = 0 and the inductor current:

$$i_L(t) = \frac{-v_g}{L}(t) \quad (2)$$

Mode 3 is the active mode in the negative half cycle ofgrid current. Similar to mode 1, when S2, S3 and S5 are turned-on, the inductor current increases in the opposite direction. In this mode, the voltage VAN = 0 and VBN =VPV, thus VAB = -VPV and the inductor current:

$$i_L(t) = \frac{V_{PV} - v_g}{L}(t) \quad (3)$$

Mode 4 is the freewheeling mode in the negative half cycle of grid current. When S5 and S2 are turned-off, the inductor current flows through S3 and D1. Similar to mode 2, If the voltages (VAN≈VBN) are higher than half ofthe dc link voltage, freewheeling current flows through S7and D3 to the mid-point of the dc link, results the voltages VAN and VBN are clamped atVPV/2. Therefore, in this mode, VAN = VBN = VPV/2, VAB = 0, and the inductor current:

$$i_L(t) = \frac{-v_g}{L}(t) \quad (4)$$

The freewheeling path potential isclamped at the mid-point of the dc link during free wheeling period of positive and negative half cycle. As a result, the inverter hardly generates any leakage current. It can also be seen that the anti-parallel diodes of the MOSFETs remained inactive during the whole operation period. Therefore, the proposed topology could be implemented utilizing MOSFET switches. However, the body-diode will be activated if a phase shift is occurred in the inverter output voltage and current. Accordingly, the dependability of the system will be reduced because of the MOSFET anti-parallel diode low reverse recovery issues.

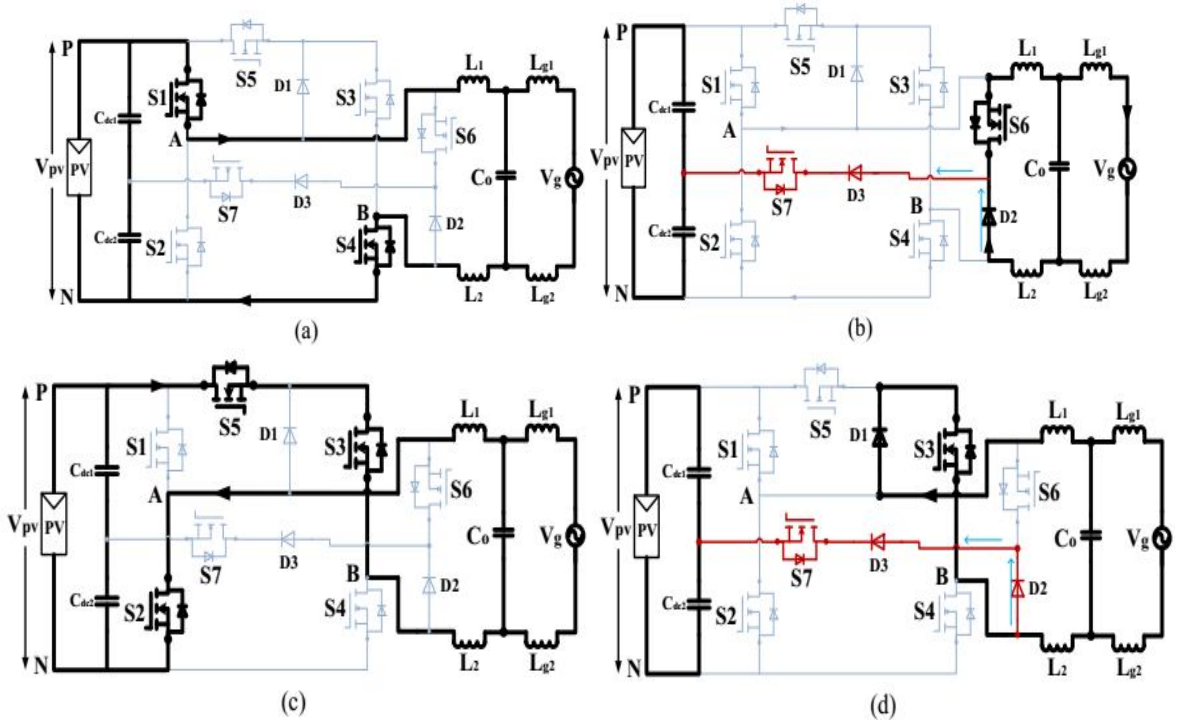



Fig.5. Operating principle of the proposed topology: (a) active and (b)freewheeling modes in the positive half cycle of the grid current; (c) active and (d) freewheeling modes in the negative half cycle of the grid current.

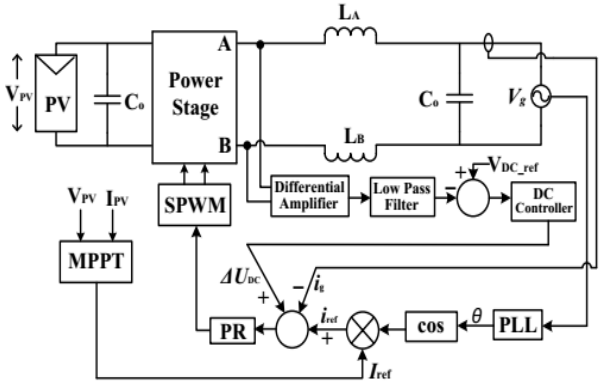



Fig.6. Control block of the proposed topology

*D. Control Technique*

In case of transformer less inverter, dc current injection into the utility grid is an important issue that may cause saturation of distribution transformer, increased loss, and abnormal operation of the load connected to the grid. In order to suppress the dc current injection into the utility grid, several control strategies have been investigated in the literature. Based on the control technique proposed an improved control strategy as depicted in Fig.6, is implemented to control the proposed topology. The control block consists of a dc suppression loop, a grid current controller, and a phase locked loop to synchronize with the grid current. The dc suppression loop is composed of a differential amplifier, a low pass filter and a dc controller. Since the output of the low pass filter of dc suppression loop is constant in steady state, so a proportional integral (PI)controller is used to control the dc offset voltage. On the other hand, grid current is sinusoidal and the proportional resonant(PR) controller has better performance of tracking the reference signal if compared to the normal PI controller and repetitive controller (RC). Therefore, if compared with the control scheme proposed a PR controller is selected to control the grid current of the proposed topology. The block diagram of the PR controller and dc suppression loop is shown in Fig.7, where GPR(s), Gd(s) and GPI(s) are the transfer function of fundamental current controller, processing and PWM delay, and offset voltage controller, respectively. The transfer functions are given below:

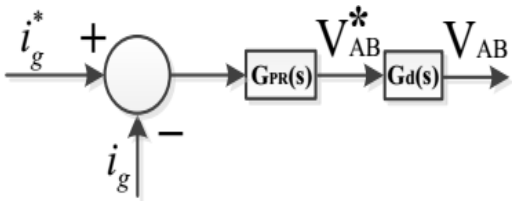
$$G_{PR}(s) = K_{pi} + K_{ii} * \frac{s}{s^2 + \omega_f^2} \quad (5)$$

$$G_d(s) = \frac{1}{1 + 1.5T_s s} \quad (6)$$

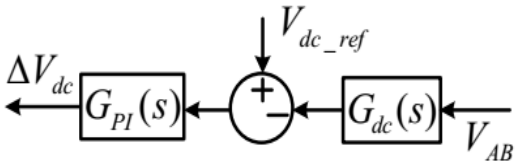
$$G_{PI}(s) = K_{pdc} + K_{idc} * \frac{1}{s} \quad (7)$$

Where Kpi and Kii are the proportional and resonant gain of the current controller, Kpdc and Kidc are the proportional and integral gain of the offset voltage controller, ωf is the fundamental frequency, and Ts is the sampling period.
Since an LC filter ($LC_f$) has been used as output filter, thus the system at ac side can be described as follows:

$$\frac{di_g(t)}{dt} = \frac{v_{AB}(t)}{L} - C_f \frac{d^2 v_g(t)}{dt^2} - \frac{v_g(t)}{L} \quad (8)$$




(a)




(b)

Fig.7. (a) Block diagram of PR controller (b) Block diagram of the dcsuppression loop

In Laplace domain, equation (8) can be re-written as

$$I_g(s) = \frac{V_{AB}(s)}{Ls} - C_f s^2 V_g(s) - \frac{V_g(s)}{Ls} \quad (9)$$

Whereig and vg are grid current and voltage, VAB is the inverter output voltage. Consequently, the equivalent model of the output filter can be drawn as Fig.8.

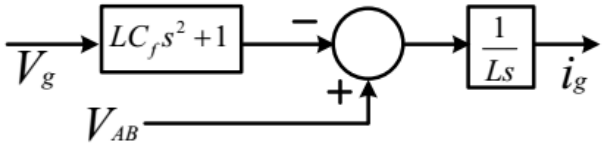



Fig.8. Equivalent model of the output filter in Laplace domain

Henceforth, according to the above illustration, the overall control diagram can be depicted as shown in Fig.9, where Gdc(s) is the feedback gain of the dc suppression loop.

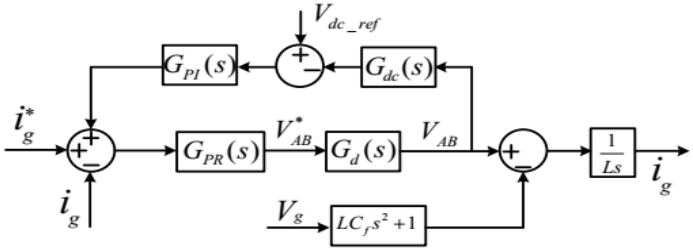



Fig.9. The complete control diagram of the proposed topology in Laplacedomain

## III. LEAKAGE CURRENT ANALYSIS AND POWER DEVICES LOSS CALCULATION

### *A. Leakage Current Analysis For The Proposed Topology*

The PV module generates an electrically chargeable surface area which faces a grounded frame. In case of such configuration, a capacitance is formed between the PV module and the ground. Since this capacitance occurs as an undesirable side effect, it is referred as parasitic capacitance. Due to the loss of galvanic separation between the PV module and the grid, a CM resonant circuit can be created. Analternating CM voltage that depends on the topology structure and control scheme, can electrify the resonant circuit and may lead to high ground leakage current. In order to analyze the CM characteristics, an equivalent circuit of the proposed topology as shown in Fig.10 can be drawn, where VAN, and VBN are the controlled voltage source connected to the negative terminal N, LCM and CCM are the CM inductor and capacitor, CPVg is the parasitic capacitance, and Zg is the grid impedance.

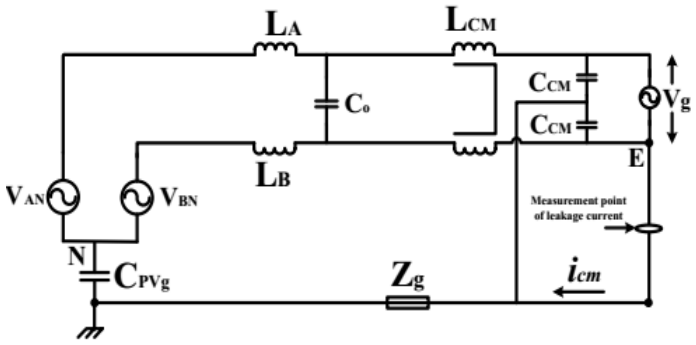



Fig.10. Equivalent CM model of the proposed topology

According to the definition of common-mode (CM) and differential-mode (DM) voltage:

$$V_{CM} = \frac{1}{2}\left(V_{AN} + V_{BN}\right) \tag{10}$$

$$V_{DM} = V_{AN} - V_{BN} \tag{11}$$

where VCM and VDM are respectively the CM and DMvoltages. Solving (10) and (11), VAN and VBN can be expressedas follows:

$$V_{AN} = V_{CM} + \frac{1}{2}V_{DM} \tag{12}$$

$$V_{BN} = V_{CM} - \frac{1}{2}V_{DM} \tag{13}$$

In order to illustrate the CM model at switching frequency, equation (12) and (13) have been replaced for the bridge-leg inFig.10. The grid is a low frequency (50-60Hz) voltage source; thus the impact of grid on the leakage current can be neglected. The DM capacitor Co can also be removed since it has no effect on the leakage current. Consequently, the simplified high frequency CM model of the proposed topology could be drawn as Fig.11. The equation for the total CM voltage can easily be derived from Fig.3.11 as:

$$V_{tCM} = V_{CM} + \frac{V_{DM}}{2}\frac{L_B - L_A}{L_A + L_B} \tag{14}$$

Where VtCM represent total CM voltage. Finally, the simplified single loop CM model of the proposed topology is derived inFig.12. In the proposed inverter if LA = LB for a well-designed circuit with symmetrically structured magnetic, equation (14)can be rewritten as follows:

$$V_{tCM} = V_{CM} = \frac{1}{2}\left(V_{AN} + V_{BN}\right) = \text{constant} \quad (15)$$

$$\textbf{Mode 1: } V_{tCM} = \frac{1}{2}\left(V_{AN} + V_{BN}\right) = \frac{1}{2}\left(V_{PV} + 0\right) = \frac{1}{2}V_{PV} \quad (16)$$

$$\textbf{Mode 2: } V_{tCM} = \frac{1}{2}\left(V_{AN} + V_{BN}\right) = \frac{1}{2}\left(\tfrac{1}{2}V_{PV} + \tfrac{1}{2}V_{PV}\right) = \frac{1}{2}V_{PV} \quad (17)$$

$$\textbf{Mode 3: } V_{tCM} = \frac{1}{2}\left(V_{AN} + V_{BN}\right) = \frac{1}{2}\left(0 + V_{PV}\right) = \frac{1}{2}V_{PV} \quad (18)$$

$$\textbf{Mode 4: } V_{tCM} = \frac{1}{2}\left(V_{AN} + V_{BN}\right) = \frac{1}{2}\left(\tfrac{1}{2}V_{PV} + \tfrac{1}{2}V_{PV}\right) = \frac{1}{2}V_{PV} \quad (19)$$

It is clear from equations (16)-(19) that the total CMvoltage for the proposed topology during the whole operationperiod is kept constant at VPV/2. Therefore the ground leakage current is reduced significantly.

## IV. SIMULATION RESULTS

### A. *Grid tied inverter*

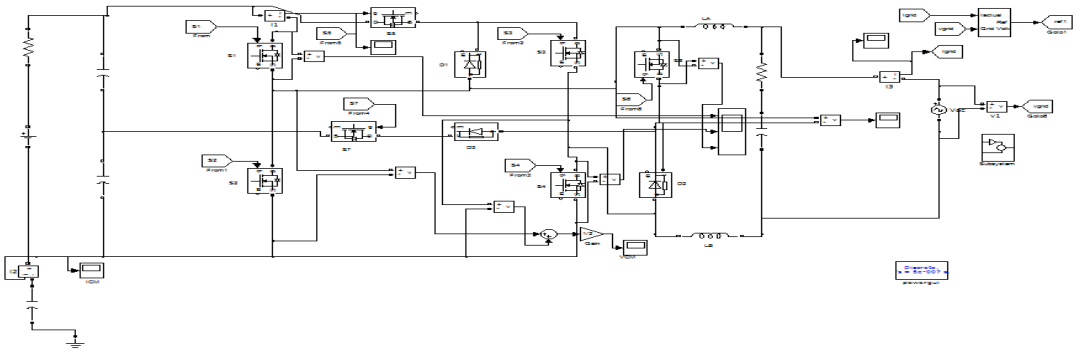


Fig.10Matlab/simulink model of Grid Tied inverter

### B. *Induction Motor Load*

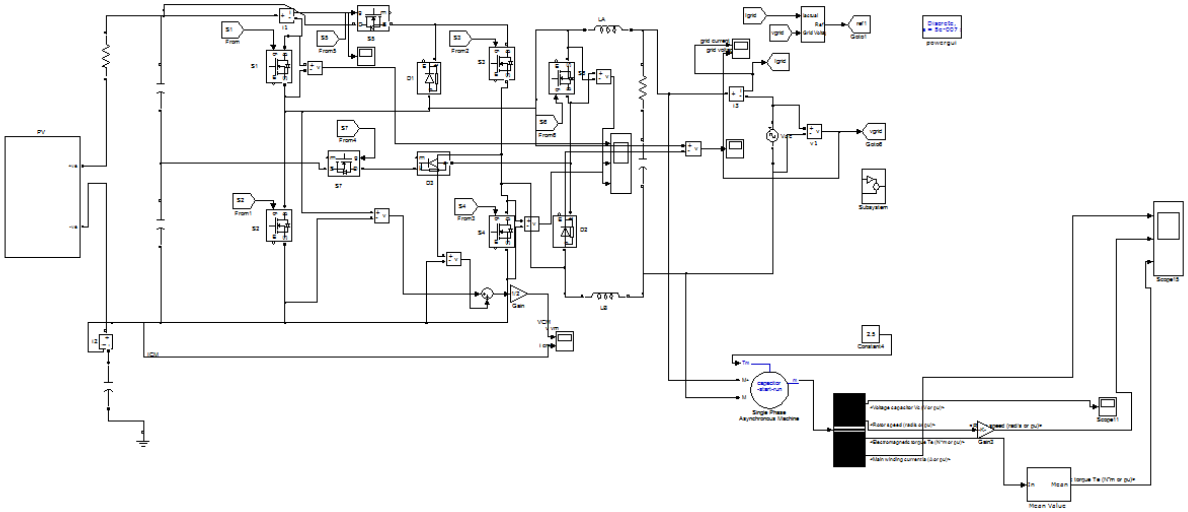


Fig.11Matlab/Simulink Model of Induction motor Load

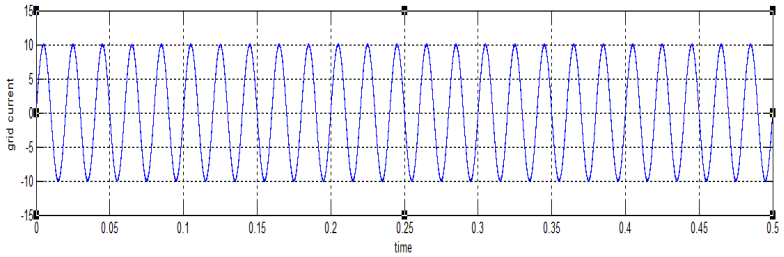



Fig.12 output grid current

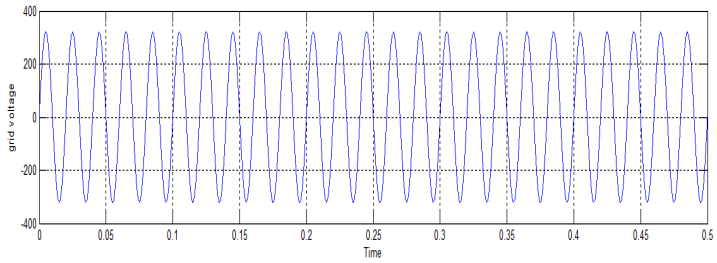



Fig.13 output grid voltage

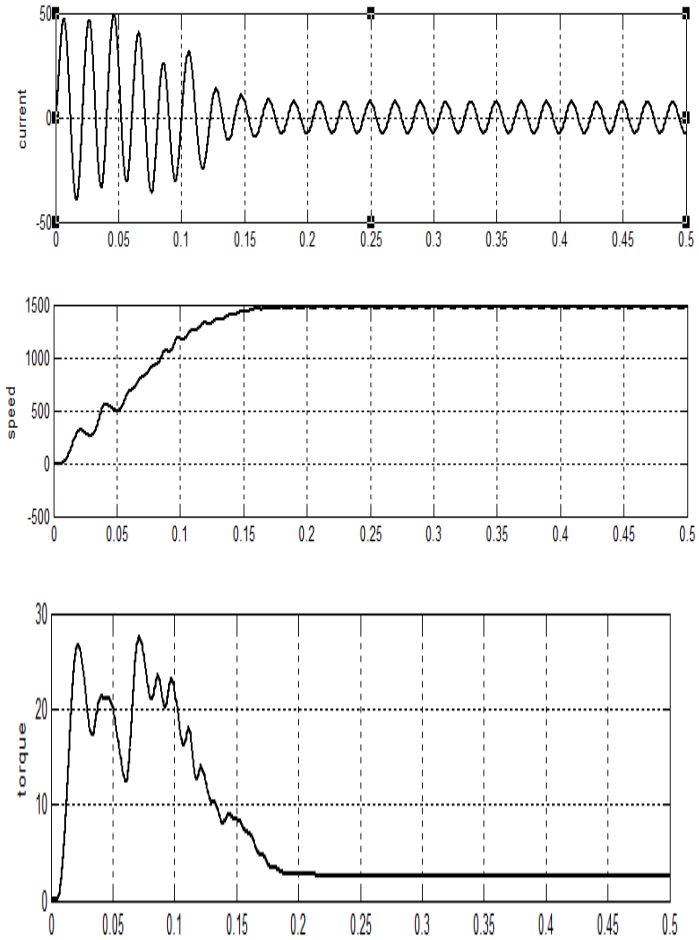



Fig.14 induction motor transient state and steady state characterstics.1)current. 2)speed.and 3)torque

## V. CONCLUSION

In this paper, a family of new efficient transformer less inverter for grid-tied photovoltaic power generation system is presented using super-junction MOSFETs as main power switches. The main advantages of the proposed topology are as follows: (1) High efficiency over a wide load range is achieved by using MOSFETs and SiC diodes, (2) Like as isolated full-bridge inverter, excellent DM characteristics are achieved with uni polar SPWM, (3) PWM dead time is not required for main power switches, results low distortion at output. Therefore, it can be concluded that the proposed inverter is very suitable for a single-phase grid-tied PV application.

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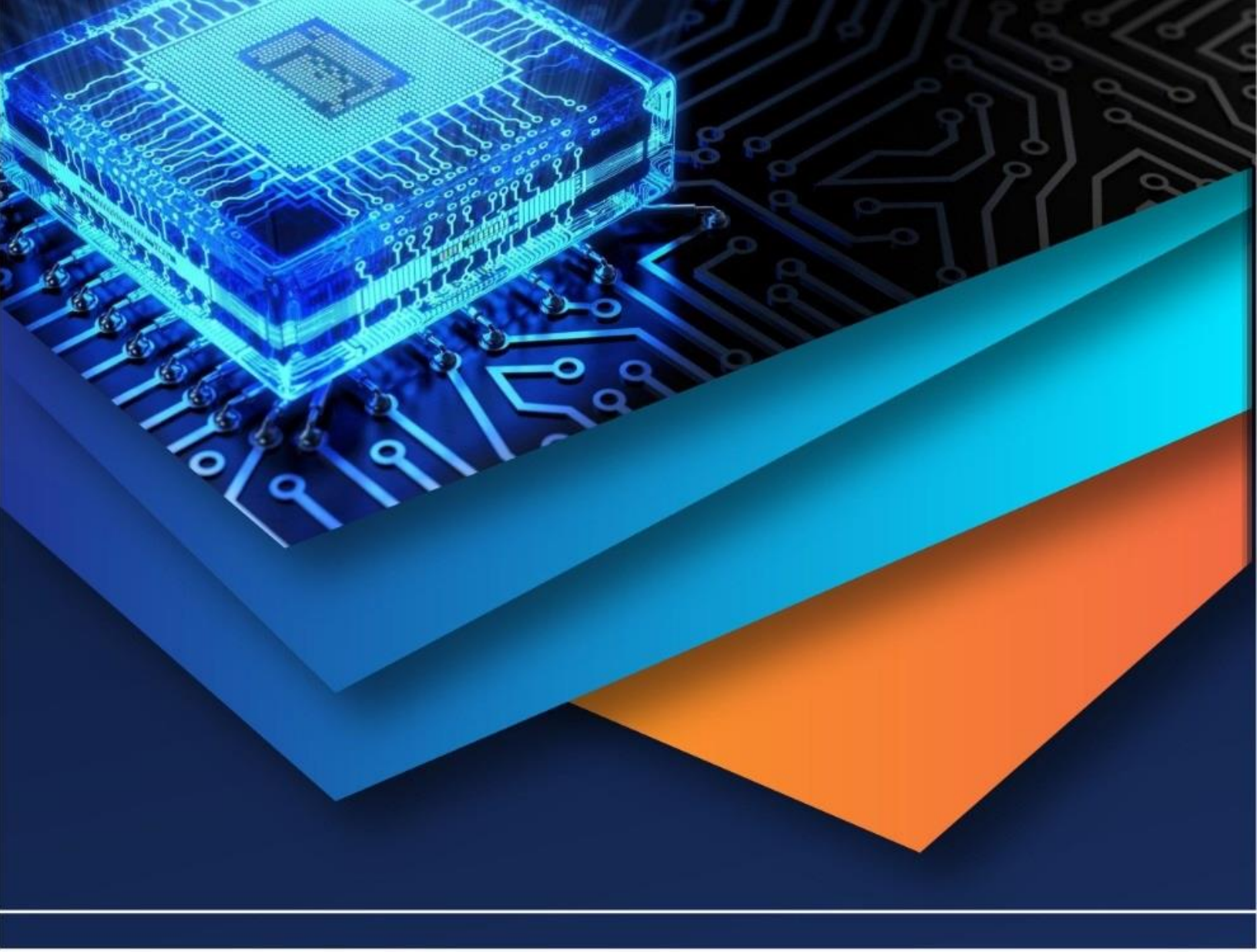

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