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Clock Gate Cloning and Methodology of Redistribution

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Abstract*: *This paper proposes a technique for clock gate optimization to aid clock tree synthesis. The technique enables cloning and redistribution of the fan-out among the existing equivalent clock gates. The technique is placement aware and hence reduces overall clock wire length and area. The method involves employing the "K means clustering algorithm" to geographically partition the design's registers. This enables better clock tree quality entitlement during clock tree synthesis in terms of clock tree area, power and better local skew distribution. Most widely used low power technique for reducing dynamic power is Clock Gating. The clock gating strategy employed has a huge bearing on the clock tree synthesis quality along with the impact to leakage and dynamic power.

Keywords*: *Clock gate, cloning, Redistribution, Methodology

I. INTRODUCTION

Typically clock gates are inserted into an integrated circuit design to save dynamic power on banks of similar registers. These clock gate cells are built as shown in Fig 1. These clock gates are typically inserted during synthesis when no placement information is available. Often during timing driven placement the grouping of sinks under clock gates is not optimal. This sub optimality in the clock gates leads to degraded clock tree synthesis quality in clock wire length, insertion delay and clock tree divergence. Subsequently, the paper showcases the clock tree synthesis quality improvements observed with this technique when tried on a complex high speed processes sub system design. The paper concludes with the future work that this work could extend to. But there are a lot of design considerations that crop up during the actual implementation of the clock gates. Disabling the clock signal to the registers in an integrated circuit when they are not in use in a digital synchronous design reduces the active power of the circuit. This clock gating may be implemented in Resistor-Transistor Logic (RTL) by the designer using knowledge of the design's activity. When the data to a register is gated by an enable signal, the design can be converted into an alternative design where the enable signal could be used to gate the clock to the register. This reduces register active power.

II. PROBLEM STATEMENT

A. The following are a few critical aspects that need to be considered while coming up with the clock gating strategy.

1) Dynamic power and leakage power trade-off.

2) Trade-off between dynamic power savings and setup timing closure to the enable pins.

3) Effect of clock gating on the clock tree divergence.

Each of these considerations has a huge impact on the quality of the clock tree in terms of insertion delay, area and divergence. The positioning of the clock gate with respect to the flops in its fan-out is very critical is a very important aspect of handling clock gates. The placement of flops is typically driven by their connectivity and timing characteristics. In such a scenario, it is extremely important to have grouping of the flops under the clock gates based on their physical proximity to ensure lower divergence and local skew. This paper proposes a physical placement aware technique for cloning and redistribution of clock fan-out among equivalent clock gates.

This paper presents an improved cloning methodology that is physical placement aware to ensure good clock tree synthesis (CTS) quality of results (QOR). The paper also proposes a clock gate fan-out redistribution technique based on physical proximity of the registers for previously cloned designs.

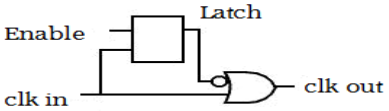


Fig 1 Clock Gate Cell

III. CLOCK GATE CLONING

A. Proposed Clock Gating Scheme

The methodology involves inserting clock gates in RTL with a suitable minimum fan-out limit constraint but with no upper bound on the fan-out of the clock gates. During layout implementation, when the placement data is available, the clock gates can be cloned using the proposed algorithm. This makes the solution fully aware of placement and ensures good CTS QoR subsequently. A simple clock gate cell driving all fan-out is shown in Fig 3.

B. Placement Aware Cloning Algorithm

Cloning of a clock gate involves creating multiple equivalent clock gates and distribution of the fan-out of the clock gate among the newly created clock gates. The proposed technique identifies clock gates for cloning if it satisfies any of the following criterions:

1) Fan-out of the clock gate is higher than a upper bound.
2) If the fan-out of the clock gate is spread over a large area.

Once the clock gates to be cloned are identified, the clones are created and the fan-out of the parent clock gate is partitioned geographically and assigned to the clock gate and its clones. The technique employs ”k-means clustering algorithm” to partition the registers.

C. 1 K-means Clustering Algorithm

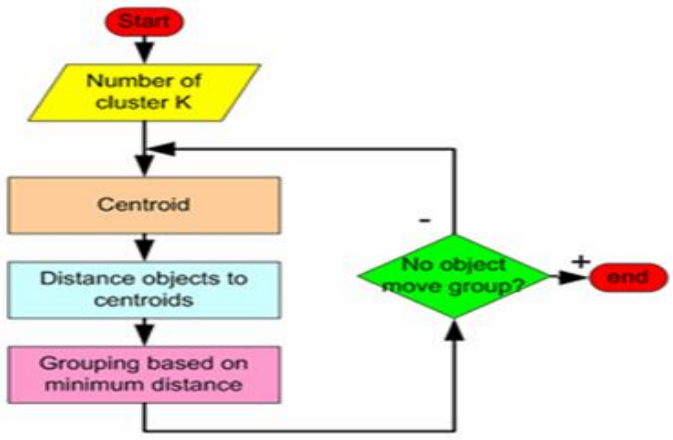
K-means clustering is a method of cluster analysis which aims to partition n observations into k clusters in which each observation belongs to the cluster with the nearest mean. It iteratively refines the clustering and the means to arrive at the cluster partition. Given a set of observations x1, x2, ..., x n, where each observation is a d-dimensional real vector, k-means clustering aims to partition the n observations into k sets ($k \leq n$) S = S1, S2, ..., S k so as to minimize the Within-Cluster Sum of Squares (WCSS):

$$\arg\min_{\mathbf{S}} \sum_{i=1}^{k} \sum_{\mathbf{x}_j \in S_i} \|\mathbf{x}_j - \boldsymbol{\mu}_i\|^2$$

Eq.1 Within-cluster sum of square deviation from mean.

where μ_i is the mean of points in S_i. Given an initial set of k means m1, m2 ...mk, the algorithm converges on the partitions and by alternating b/w the following 2 steps:

1) *Assignment step:* Assign each observation to the cluster with the closest mean (i.e. partition the observations according to the Voronoi diagram generated by the means).
2) *Update step:* Calculate the new means to be the centroid of the observations in the cluster.



D. 2 K-means Clustering Adaptation for Clock Gate Cloning

The K-means algorithm represented in Eq.1, can be directly used to physically partition the flops of a design into a few clusters each driven by a clock gate.

The observations x1, x2, ..., xn will be the location of the flops, S1, S2, ..., Sk will be the k clusters that the flops will be partitioned into and m1, m2, ..., mk will be the mean location of each cluster where the clock gate of that cluster can be placed. The flowchart in Fig.4 describes how the standard k-means algorithm is adopted for partitioning flops under the clock gates/clones. Initially the clock gate and its clones are placed on the diagonal of the smallest rectangle containing all the registers in the fan-out of the parent clock gate. This forms the initial locations of the means for the algorithm Each register is then attached to the nearest clock gate. In case the clock gate has already reached its fan-out limit, it is attached to next nearest clock gate. Once all the registers are assigned to the clock gates, the location of the clock gates are recalculated as the mean location of the registers it is assigned. The register assignment and clock gate location relocation steps are repeated iteratively to obtain the best physical partition of the registers. The iterations can be stopped as soon as the following 2 criterions are satisfied.1) The registers are not getting reassigned any more.2) The locations of the clock gates are not changing anymore.

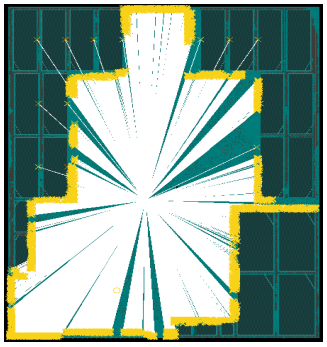


Fig 3 Clock gating cell driving all fan-out

This is done for every clock gate that has been identified for cloning. This technique ensures that all the clock gates are driving registers that are clustered together on the layout and also that the clock gate is placed exactly at the load center of its fan-out, These make the clock gating structure very conducive for good CTS QoR entitlement. Fig 1 illustrates the results of placement aware cloning on a sample design. The single clock gate driving all the flops is efficiently cloned to handle smaller and more physically localized collection of flops.

Fig 4 Clock Gate Cloning done using K means clustering

IV. RESULTS

The proposed methodology was used for optimizing the clock gating on a 28nm processor subsystem and the results were bench marked against the other solutions. The run time to clone a little over thousand clock gates was less than 15 minutes when executed on a Linux box. The memory overhead of the algorithm is insignificant. Table 1 shows the clock tree synthesis results with the various options of handling clock gates.

	Without any clock gate optimization	Clock gates cloned with an EDA solution	Clock gates cloned usisng the proposed technique
Max insertion delay	595ps	486ps	281ps
Skew	65ps	57ps	70ps
Clock gate area	2340	3140	1982
Clock gate area	1254	2345	1454
Total clock tree area	3594	5485	3436

Table 1 Clock Tree Synthesis (CTS) Quality Of Results (QOR) comparison.

V. CONCLUSION

The results highlight the value the technique brings into the design in terms of clock tree area. This in turn reduces the leakage power of the design. In addition to the area improvement, the methodology also sets up the design for implementing relative placements for the flops and clock gates. The relative placement is a commonly used practice to reduce leaf clock power and also area reduction. Using the proposed method ensures that the regular placement implementation can be implemented without big register displacements. As a future work to this effort, we need to develop an efficient methodology to declone clock gates. In scenarios where we already have a design with clock gates already cloned, merging equivalent clock gates to optimize area and also satisfy all the above requirements mentioned in the paper earlier.

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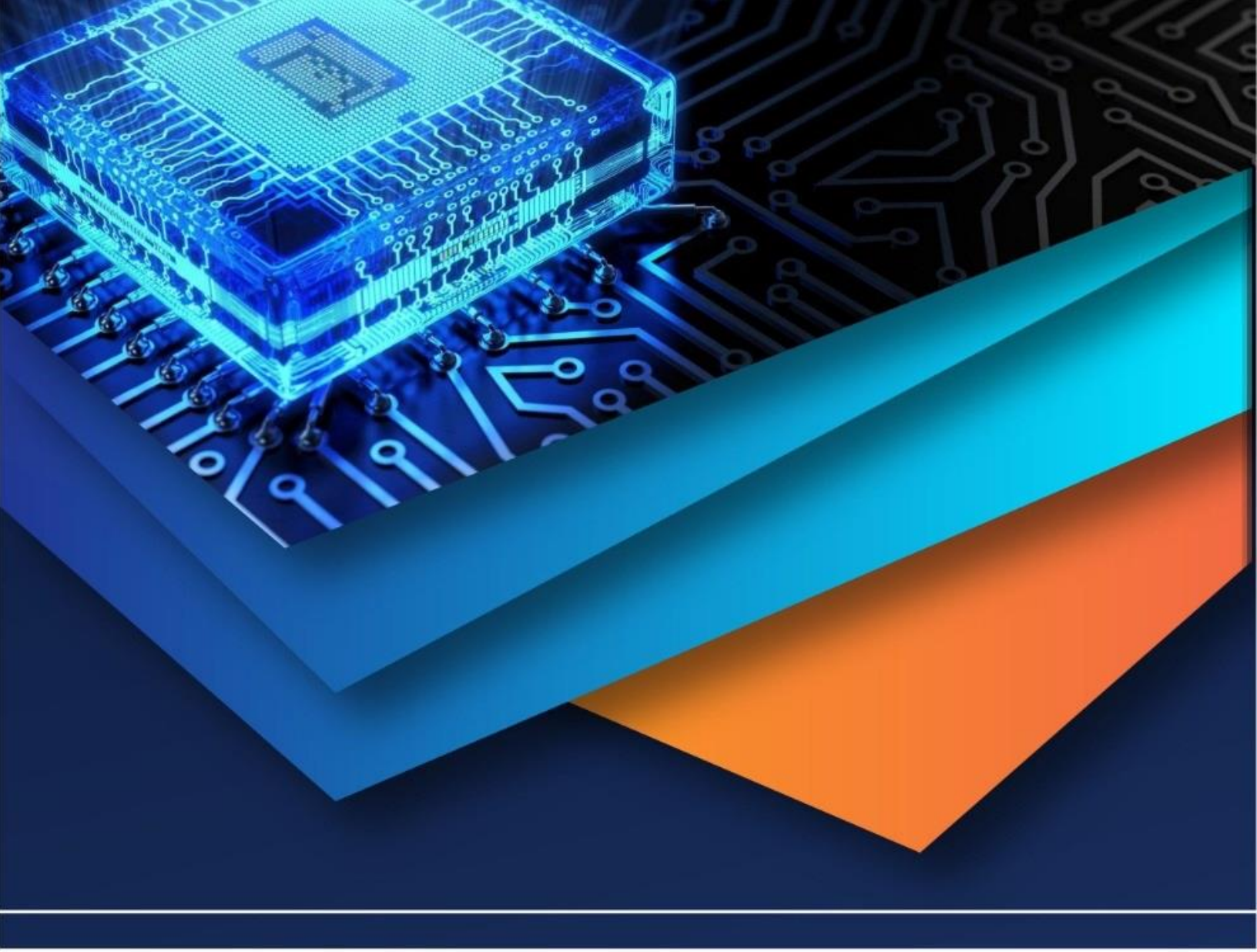

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