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Design and Operational Synthesis of 64-bit Adder and Subtractor Unit using Delay Efficient Parallel Prefix Technique

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Abstract*— Digital design of the various arithmetic circuits often finds the applications in various devices and processes. Various circuits like adder, Subtractors, and multipliers are being used in various digital circuits. BCD arithmetic circuits are also widely used in various communication devices and often find the advantages in a lot of storage media and compatible for various industrial devices. In this work, we have proposed the design of the 64-bit BCD Adder and Subtractor using reversible logic circuits and high speed modified design has been presented. Here, we have used Peres gate for the design using Kogge-stone adder which decreases the delay in addition processes. For the adder, we have used the converter modules. Here, we have simple binary adder module, in combination with the error correction circuit and low power binary to BCD modules. We have used parallel prefix architecture for the adder/Subtractor design and delay efficient algorithm for the Subtractor. The suggested system design has been design using Model sim 10.3d, synthesized using Xilinx 14.1 for the low power KINTEX-7 KC705 FPGA Evaluation Platform as target module and for power consumption X power analyser has been utilized. The Kintex family uses 28nm (nanometer) design technology which utilizes only half of the lower power than the other compared technologies.

Keywords*— BCD arithmetic circuit, Cryptography, Kogge-stone adder, Low power, Parallel Prefix, Reversible logic circuits.

I. INTRODUCTION

The decimal arithmetic receives a huge focus of attraction since economic, money related and World Wide Web connection related applied fields which usually never bear any such type of faults in the system during conversions from binary form to decimal or vice versa. It is mainly considered to implement the BCD arithmetic devices so as to enhance the speed as much as possible. Reversible computing is an attractive research area. The Bidirectional computing is a model of computing where the calculation process up to some level is reversible in nature such as time invariant. Basically, in a computational design which uses the concept of deterministic transformation from one level of the existing device to another one the most important condition for a system to be bidirectional is the relationship between mappings from a non-zero probability state to its succeeding state must be in one to one mapping condition. The concept of bidirectional or a reversible system is that it always follows the process of running the device in both forward as well as backward directions. It means that in a reversible system the computation process generates input from output and as when required it stops and get back to any desired place in the previous level or stage of computational calculation. The bidirectional circuit is a kind of unconventional mathematical and logical procedure. We have two most popular types available namely the Physical reversibility and Logical reversibility techniques that can handle such type of computational process. If we compare a simple conventional circuit with the bidirectional circuit then we would love to prefer the second one because a bidirectional or reversible circuit has equal number of logic gates at both the input as well as the output port. An output is said to be “Garbage” if it is not being able to be used as a input source for the further next stage or unable to be utilized as a primary output and commonly referred as garbage output in a particular condition in which it adds mirror circuit as well as spy gates and the output being neglected. In a bidirectional logic, output from a gate or device can be used as a input to its next gate with no fan out. The whole research paper involves the designing of 64 bit adder and subtractor circuit using a special parallel prefix bidirectional circuit which is none other than Kogge stone adder. A reversible logic design will not lead to information loss and this in turn avoids the useless heat generation. The power will never degrade in an impulsive or arbitrary circuit if it is made of bidirectional or reversible circuit. If a circuit draws each incoming information signal say a input to a very different or in a unique format then the digital circuit is referred as a bidirectional circuit. The reversible 64 -bit BCD addition unit is designed using reversible logic gates such as peres gate. Here, we will be using 4-bit module of the Kogge-stone adder to integrate it using parallel pipelining architecture. Here, we have prepared a parallel prefix Kogge stone adder. Similarly, delay efficient algorithm has been used for the development of the Subtractor design. We have been using 9’s complement module for the Subtractor and thus efficient borrow algorithm for the 64-bit has been integrated for the final module design.

II. REVERSIBLE LOGIC CIRCUITS

Reversible or bidirectional computing had played a very significant and influential role from the last few decades. Actually a lot of logical implementation and analysis techniques have been successfully accomplished for the bidirectional circuit devices. In

the year 1973 an International Business Machines (IBM) researcher Bennett a well known and highly reputed leader in the fastest emerging environment of quantum science in the information technology field and boomed the scientific world. If a logical port A is bidirectional for any output q, there is a unique input p such that it operates as A(p)q. If the logical port L is bidirectional in nature then there will be an inverse port L′ which draws q to p for the function and operate as A(q)p. From common logic gates, NOT is reversible, as the inputs are 0 or 1 and the outputs are also 1 or 0 but the common AND gate is not reversible. However a bidirectional computational technique in any electronics devices can be carried out only in one condition that when such devices or system has system the availability of all the bidirectional gates or circuits.
A circuit or gate is said to be bidirectional if the information source can be differently restored from the final output signal and there is a relation among the incoming and outgoing signals as one on one format. The quantum computers have such type of reversible circuit that makes the basic structure of it. Some of the most common bidirectional logic circuits are Feynman, BJN, SCN, Peres, Toffoli and NOT.

*A. **NOT Gate***

Not gate is a 1×1 gate with quantum cost value of zero. It is the only bidirectional circuit when comparing and analysing with the other conventional logical circuits.

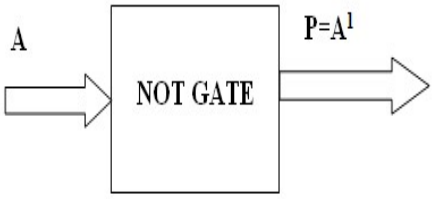

Fig.1. NOT Gate

*B. **Feynman Gate***

Feynman Gate is also known as CNOT or controlled CNOT Gate and also its one of the input bits acts as a control signal. Suppose if the input A=1 then the second input B is shifted at the output Q. It is a 2×2 bidirectional circuit having two inputs and two outputs with a single quantum cost. It is a circuit having mapping of the type I(A,B) and O(P=A, Q=A⊕B) where A,B are the inputs and P, Q are the outputs.

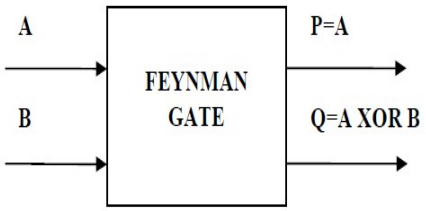

Fig.2. Feynman Gate

*C. **Peres Gate***

The Peres Gate is a 3×3 kind of bidirectional or reversible circuit having three inputs as well as the three outputs at both the ends with having the lowest price value of only 4. We can design the Peres gate by using two XOR and one AND circuits with the map marked from the incoming signal I(A,B,C) as well as the outgoing signal which can be defined as O(P=A, Q=A⊕B, R=AB⊕C) among them there are (A,B,C) and (P,Q,R) are the inputs as well as outputs respectively.

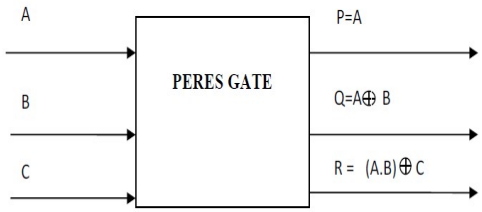

Fig.3. Peres Gate

D. ***Toffoli Gate***

Toffoli gate is one of the most important and very popular bidirectional circuits which have a quantum cost value of about 5. This bidirectional circuit has 3×3 value which implies that it uses three input as well as three output out of which two of its outputs are as used as input in which the map draws from incoming signal say I(A,B,C) up to the outgoing signal say Q(P=A, Q= B, R=AB⊕C) among them signals (A,B,C) as well as (P,Q,R) are the inputs and outputs respectively.

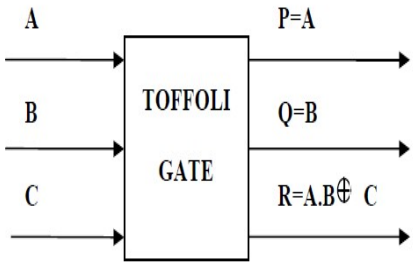

Fig.4. Toffoli Gate

III.CONCEPT OF PARALLEL PREFIX

The advancement in each and every sector of human being is due to the continuous efforts and leading an innovative and creative thought creates tremendous applications for Very Large Scale Integration (VLSI) in the field of high speed computing technologies such as in Microprocessors, Arithmetic and Logic Unit (ALU), memory addressing units, etc. The time period of a clock cycle is somehow directly depends on the speed of the adders used in the circuit. The concept of parallel prefix adders or simply PPA arises as they are faster than ripple carry adder. PPA are derived from carry look ahead adders and has wide word length. They uses tree network to reduce response time. The Kogge stone adder, Skylansky adder, Brent Kung adder as well as the Han Carlson adder are the highly accepted and appreciable adders among the other bidirectional circuits.

IV. KOGGE STONE ADDER

The Kogge–Stone adder circuit is also referred as parallel prefix kind of CLA adder or simply abbreviated as carry look-ahead adder. Some of the most popular and well known parallel prefix adders are Han Carlson adder, Brent Kung adder and the fastest known one is the Lynch-Swartzlander Spanning Tree adder. The Kogge–Stone adder in terms of comparison takes more area for implementation than the Brent–Kung adder but has a lower fan-out value at each and every stage which increases the performance for mostly CMOS process nodes or junction. However, wiring congestion or overcrowding is often a problem for Kogge–Stone adders. This is the most delay efficient adder.

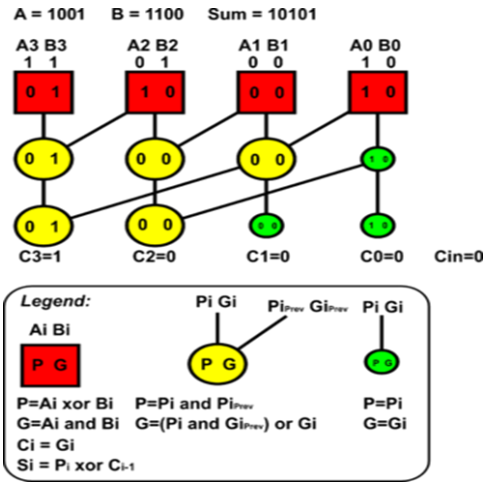

Fig5. 4 bit Kogge stone adder with Carry input signal

V. PROPOSED ARCHITECTURE

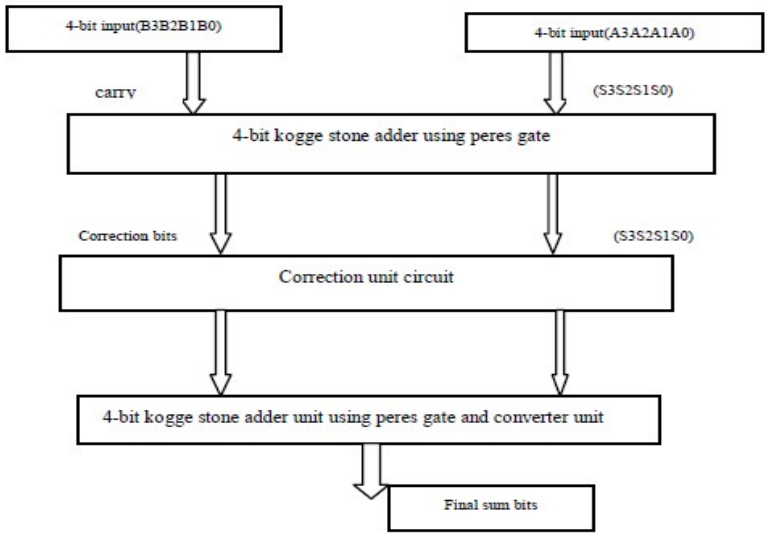

Fig.6. Proposed 4-bit BCD Adder design

Here, in the above fig.6, we have proposed the design of the BCD adder (4 bit). It is capable of adding the two BCD 4-bits. It consists of the adder module implemented using the Kogge-stone adder using reversible Peres gate only. The design is utilized using the compact algorithm for correction unit for 4-bit and its capable of generating the carry bit and utilize in the correction unit.

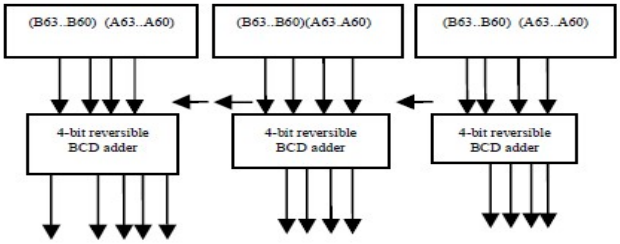

Fig.7. Proposed 64-bit BCD Adder design

In fig 7, by cascading the 4-bit adder module of BCD, we can obtain the final 64-bit design. Thus, 64-bit design has been implemented by cascading the design units.

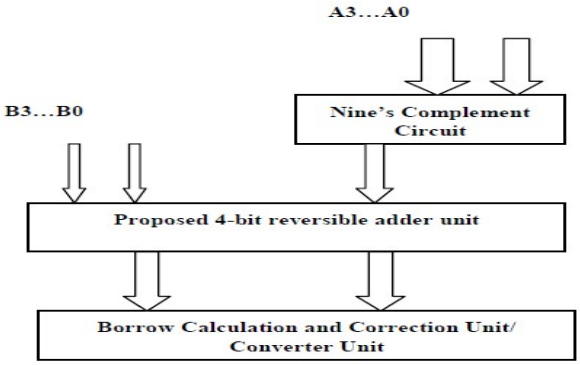

Fig.8. Proposed 4-bit BCD Subtractor Design

In fig.8, the design of the 4-bit Subtractor has been presented. The unit consists of the nine's complement circuit using the reversible gates followed by the 4-bit Kogge stone adder. Similarly, final we have optimized the design for the borrow and converter design in the final unit. Thus, the final design is reversible design and capable of subtracting the two 4-digits BCD numbers and can handle the negative as well as borrow bit, if generated.

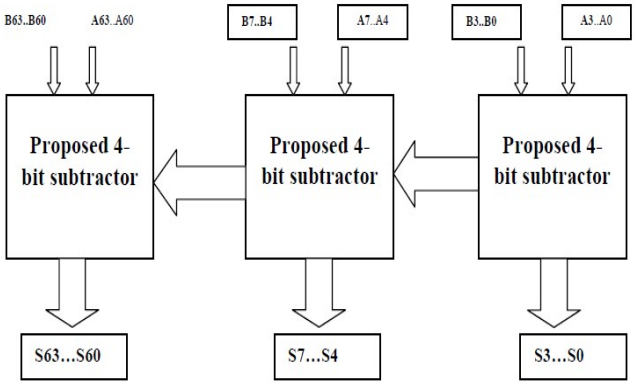

Fig.9. Proposed 64-bit BCD Subtractor Design

Thus, by cascading the Subtractor design, we can implement the 64-bit design as shown as in fig.9.

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VI. RESULT AND DISCUSSION

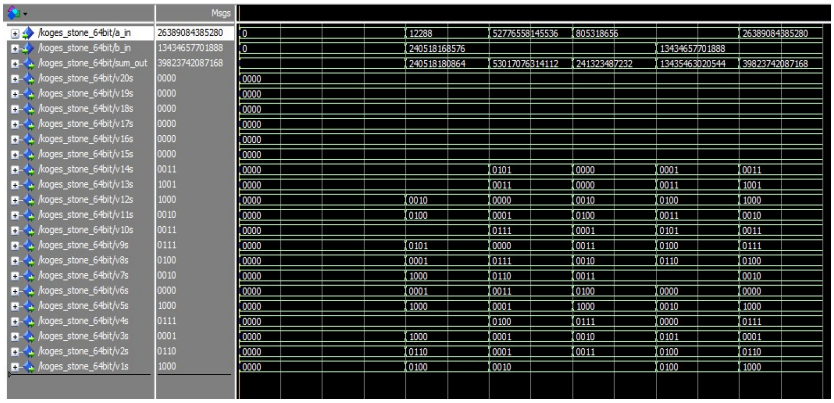

Fig.10. Simulation result of 64-bit BCD Adder unit

In figure 10, the simulations for the 64-bit BCD adder have been presented. The simulation result has been presented for the final design of the BCD adder. The various numbers have been shown to be added in the design. The final sum has been generated.

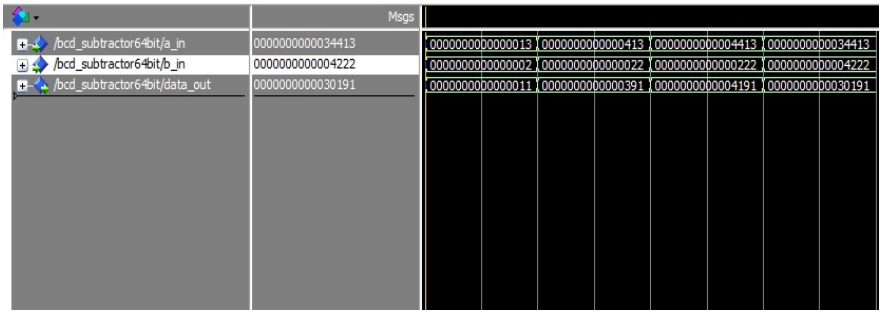

Fig.11. Simulation result of a 64-bit BCD Subtractor unit

Similarly, in figure 11, the simulations for the 64-bit BCD Subtractor have been presented. The simulation results have been presented for the final design of the BCD sub tractor. The various numbers has been shown to be subtracted in the design. The final sum has been generated. Thus, it is shown that it is capable of handling the two 64-bit BCD numbers as presented above.

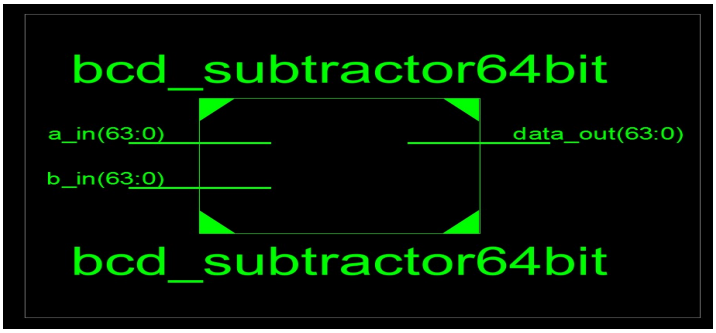

Fig.12. RTL1 Schematic view of a 64-bit Subtractor unit

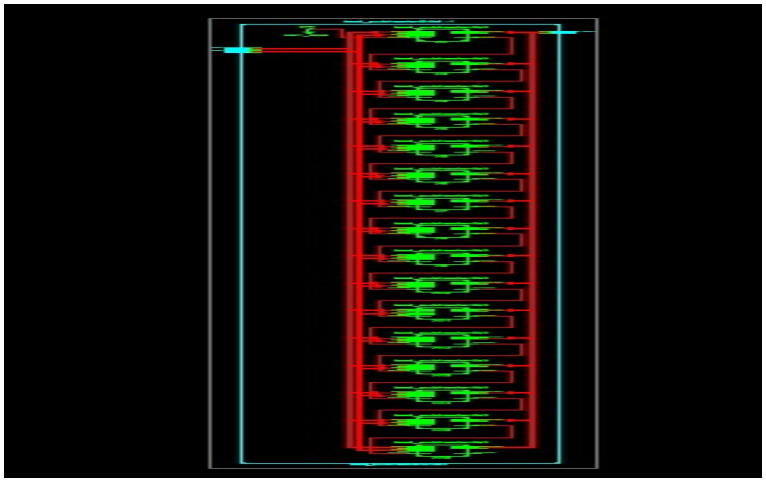

Fig.13. RTL2 Schematic view of 64-bit Subtractor unit

In figure 13, the RTL structure has been presented for the 64-bit sub tractor design. As per the designed blocks, the blocks have been synthesized.

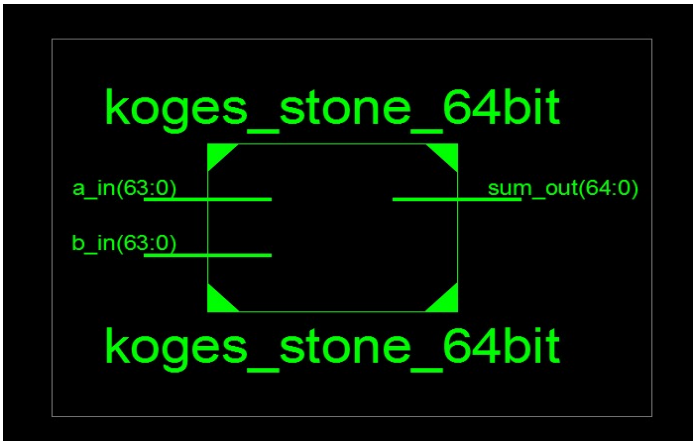

Fig.14. RTL1 Schematic view of 64-bit Adder unit

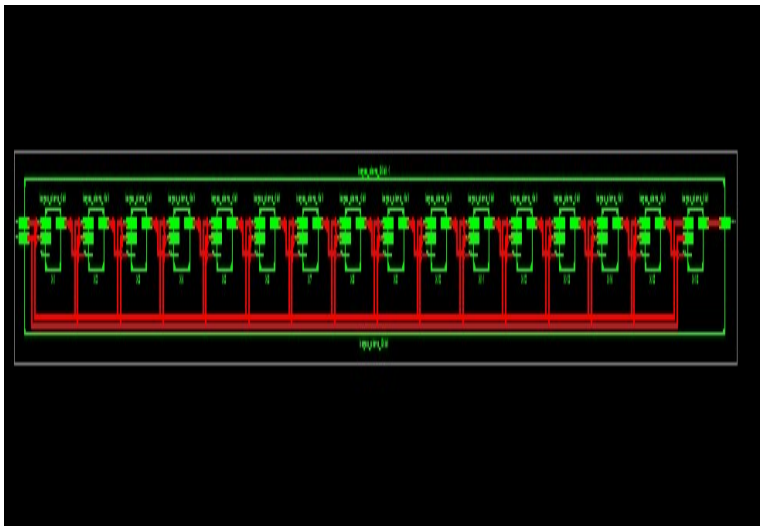

Fig.15.RTL2 Schematic view of 64-bit Adder unit

In figure 15, the RTL structure has been presented for the 64-bit adder design. As per the designed blocks, the block has been synthesized.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	218	960	22%
Number of 4 input LUTs	379	1920	19%
Number of bonded IOBs	273	83	328%

Fig.16. Device Resource Summary of 64-bit Adder unit

In figure 16, the device utilization summary for the final design of 64-bit BCD adder has been presented.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	190	203800	0%
Number of fully used LUT-FF pairs	0	190	0%
Number of bonded IOBs	192	500	38%

Fig.17. Device Resource Summary of 64-bit Subtractor unit

In figure 17, the device utilization summary for the final design of 64-bit BCD sub tractor has been presented.

Thus we can also implement and generate the final result through the x power analyzer as,

Device	
Family	Kintex7
Part	xc7k325t
Package	ffg900
Temp Grade	Commercial
Process	Typical
Speed Grade	-2
Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA
Characterization	
Advance	v0.6,2012-01-12

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	64	203800	0
Signals	0.000	224	---	---
IOs	0.000	193	500	39
Leakage	0.122			
Total	0.122			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	1.8	84.8	25.2

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.068	0.000	0.068
Vccaux	1.800	0.028	0.000	0.028
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.122	0.000	0.122

Fig.18. Generation of final result through X power analyzer.

VII. TABLE I. COMPARISON TABLE

Reversible Logic	Input Bits	Delay (ns)
Existing 32-bit BCD Adder	32	17.42
Proposed 64-bit BCD Adder	64	15.79
Existing 32-bit BCD Subtractor	32	17.42
Proposed 64-bit BCD Subtractor	64	19.25

Table1. Comparison table of the proposed and the reference design

In table 1, the final comparison has been presented. The proposed design for the sub tractor has been found to have the critical path delay of 19.25ns. Thus, it is very much efficient as compared to the existing reference design. Similarly, the adder shown has the critical path delay of the 15.79ns. Thus, our design is proved to be more delay efficient and speedy due to the use of the Kogge stone adder.

VIII. CONCLUSION AND FUTURE SCOPE

In the proposed work, we have proposed the 64-bit reversible design of the BCD adder and subtractor circuit. The design have been implemented using the Kogge stone adder unit for increasing the speed and reduce the delay in the circuit. The 4-bit adder unit has been presented. Similarly, various units like error correction circuits, converters have been used for adder. Similarly, nine's complement unit and borrow correction unit has been implemented by the reversible gates as presented in the proposed design. Similarly, the power efficient design has been presented using the reversible logic unit for development of the desired gates. Hence we have successfully done the system simulation and having the result using Modelsim software and also analysis of circuit synthesis has been accomplished. As per the results presented, our proposed design has been verified for the delay functionality. We can design some more advance and much energy as well as power efficient resource devices or structural circuits that takes less input but gives sufficient output for the development of the human being. It can be improved further by increasing the number of bits in the circuit or by using some more efficient circuit or gates so as to reduce the power loss which usually takes place in the devices.

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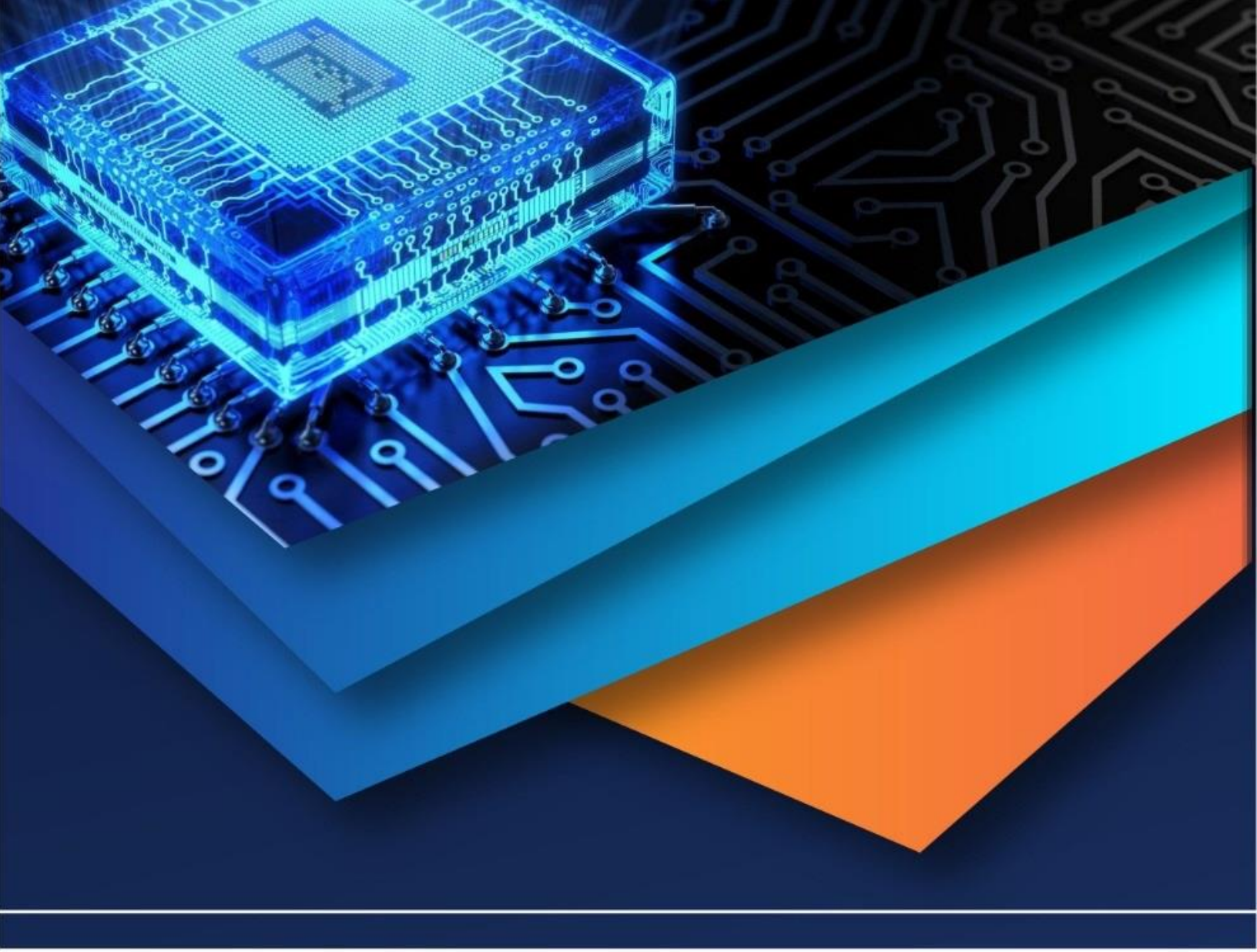

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