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Performance Modeling of Cluster Tree based IWSNs for Time Critical Applications

Dr. Ganesh Babu T.V.J.[1], Mrs. Anuradha T[2]
[1]Dept. of ECE, St. Martin's Engineering College, Hyderabad,.[2]Dept. of ECE, MLR Institute of Technology, Hyderabad

Abstract: Industrial Wireless Sensor Networks (IWSNs) need to provide deterministic performance and hence uses the MAC standards based on slotted super frame structure such as IEEE 802.15.4 LRWPAN. In this paper, the designing of the super frame structure of the slotted MAC is investigated by two means: 1) a mathematical model of the MAC access latency based on the queue theory and 2) an easy-to-use software tool based on packet-level simulation. The mathematical model contributes an overall estimation of the average MAC access latency and delay to reach sink through multiple MACs of the whole network. The software tool evaluates the latency of each packet and then can derive the optimal super frame structures of the network based on network latency. The two means are corroborated accordingly. With the methods suggested in this paper, IWSN designers can minimize the mean delay to reach sink and MAC access latency, while satisfying the requirements at different generating rates of packets, packet buffer length of each node and number of clusters and nodes in the network satisfying the required QoS.

Keywords: LR-WPAN, IEEE 802.15.4, Cluster Tree, Latency, Delay, QoS, Super frame

I. INTRODUCTION

The recent advents in wireless communications trigger the development of standard protocols specifically designed for a particular range of applications. The IEEE 802.15.4 protocol has been proposed with updated version in 2015, as a wireless communication standard for low-rate, low power consumption Wireless Personal Area Networks(LRWPANs)([1]-[3], [5]). To allow time-critical applications, IEEE 802.15.4 extends a guaranteed time slot (GTS) allocation mechanism at the network coordinator to provide certain guarantees on eventual delivery and delivery times of packets to be transmitted by local devices to the network coordinator. Specifically, in IEEE 802.15.4, packets are carried on a super frame basis[12].

IWSN has more critical requirements than traditional WSN. There are numerous tasks to be considered, such as different means of supporting emergency actions, automated regulatory and supervisory control, safe operation of the plant, real-time open-loop control, close-loop control where a human being is part of the loop, information uploading and/or downloading, and semantic data accessing. At the same time, the complexity of the IWSN node has to be minimized, such that it can be implemented with accordable cost.

To deal with this challenge, the communication network must be designed to meet the real-time requirements of the application system. This involves two tasks:

To tune the communication traffic such that the network will not be overloaded while meeting real-time requirements.

To specify maximum acceptable latency of each transaction and guarantee that the success or failure of that transaction is notified to the application system.

Both tasks are related to the planning of super frame structure. In IWSN, the super frame structure is defined in MAC layer. In particular, the 802.15.4 beacon-enabled protocol uses a slotted channel access mechanism, where the slots of a super frame are divided into two phases: the contention access period (CAP) and the contention free period (CFP). In the CAP phase, a slot is shared by devices (i.e., any node can transmit), but it is not guaranteed that the transmission would succeed, and a random back-off strategy is used to allow retransmission in case of collision. This MAC mechanism is called Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). In the CFP phase, a slot is allotted to one node (i.e., only this node can transmit in this slot), and every node in the topology is assigned a guaranteed time slots (GTS). So the communication can be improved by applying the CFP phase for time–critical transmission[8].

The access latency in the MAC layer is determined by the structure of super frame including the total number of slots of the super frame, the CFP stage and the number of slots in the CAP stage. Therefore, for the IWSN, a good super frame planning is essential to minimize the access latency, optimize the utilization of network throughput, channel resources and, as a result, to improve the real-time performance. However, the existing standards have not specified any methods for this function. The existing research on this problem is far from sufficient. In this paper, the planning of the super frame structure of the slotted MAC is investigated by three means:

A mathematical model of the MAC access latency based on the queue theory.

Performance analysis of cluster tree architecture with inactive part of super frame modeled.

An easy-to-use software tool based on packet-level simulation.

The mathematical model gives an overall estimation of the average MAC access latency of the complete network. The software tool establishes the exact latency of each packet and then can derive the optimal super frame structure of each network. The two means are validated correspondingly. With the methods suggested in this paper, IWSN designers able to minimize the MAC access latency while satisfying the requirements for different parameters, such as number of nodes in the network, packet generation rates, and packet buffer length of each node.

II. SYSTEM DESCRIPTION

The various aspects of the system are described as follows.

A. Cluster Tree Network

The cluster tree network is a special case of a peer-to-peer network. The simplest form of a cluster tree network is a single cluster network, but larger networks are possible by organizing a mesh of multiple neighbouring clusters[4]. Once predetermined application or network requirements are met, the first PAN coordinator instructs a device to become the PAN coordinator of a new cluster adjacent to the first one. Other devices gradually link and form a multi-cluster network structure, such as the one shown in Fig. 1. The lines in Fig. 1 represent the parent-child relationships of the devices and not the communication flow [13]. The advantage of multi-cluster structure is increased coverage area, while the disadvantage is an increase in message latency.

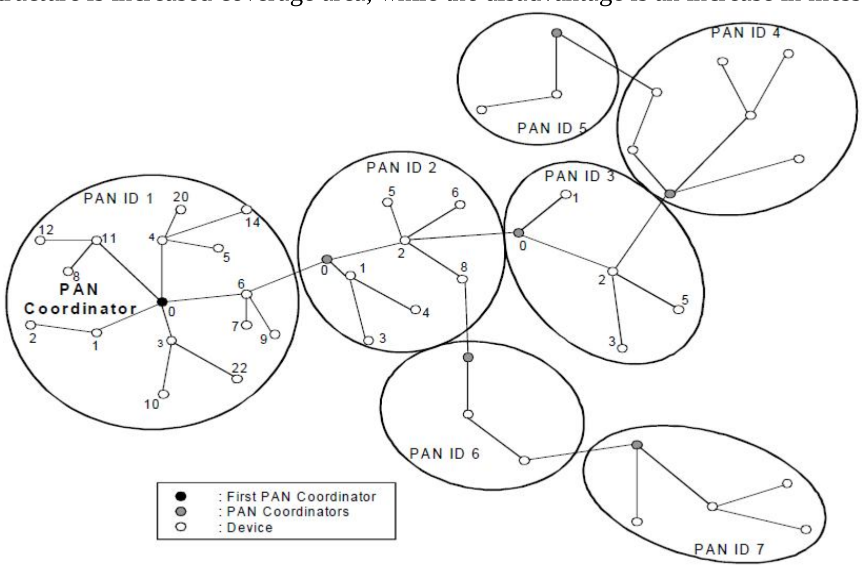

Fig. 1 Cluster Tree Network

B. Overview of IEEE 802.15.4 Protocol

In beacon-enabled mode, beacon frames are periodically sent by the PAN coordinator to identify its PAN and synchronize nodes that are associated with it. The Beacon Interval (BI) defines the time between two consecutive beacon frames, and includes an active period and an inactive period (Fig. 2). The active period, called super frame, is divided into 16 equally-sized time slots, throughout which frame transmissions are allowed. The inactive period, all nodes may move into a sleep mode, thus saving energy. The Beacon Interval and the Super frame Duration (SD) are determined by two parameters such as the Beacon Order (BO) and the Super frame Order (SO), respectively [4]. By default, nodes compete for medium access using slotted CSMA/CA during the Contention Access Period (CAP). A node computes its backoff delay based on performs two CCAs and a random number of back off periods before accessing the medium. The IEEE 802.15.4 protocol can also offers the possibility of defining a Contention-Free Period (CFP) within the super frame (Fig. 2). The CFP, being optional, is activated upon request from a node to the PAN coordinator for allocating guaranteed time slots (GTS) depending on the node's demands. The performance of the GTS mechanism is addressed [15].

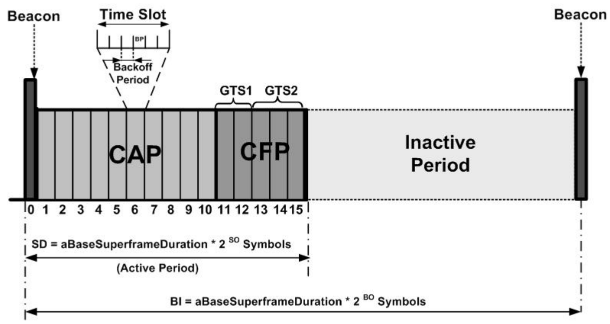

Fig. 2 Superframe structure of IEEE 802.15.4

C. The Slotted CSMA/CA Mechanism

The slotted CSMA/CA algorithm is based on a basic time unit called Back off Period (BP), which is adequate to a Unit Back off Period = 80 bits (0.32 ms) . Every operation of slotted CSMA/CA (channel access, back off count, CCA) can only happen at the boundary of a BP. Additionally, the BP boundaries must be aligned with the super frame time slot boundaries (shown in Fig. 2).

The slotted CSMA/CA back off algorithm mainly depends on three variables:

The Back off Exponent (BE) enables the computation of the back off delay, which is the time before performing the CCAs. The back off delay is a random variable between 0 and (2^BE −1) .

The Contention Window (CW) represents the number of back off periods during which the channel must be sensed idle before accessing the channel. The standard set the default initialization value to CW = 2 (corresponding to two CCAs). In each back off period, channel sensing is done during the 8 first symbols of the BP.

The Number of Back offs (NB) represents the number of times the CSMA/CA algorithm was required to back off while attempting to access the channel. This value is initialized to zero (NB =0) before each new transmission attempt.

D. Delays and MAC access latency

As shown in Fig. 3, Wireless HART, WIA-PA, and ISA100.11a allow the devices to share a slot or dedicatedly occupy a slot. In the Wireless HART, the principle super frame will be composited by GTS, which is CFP-like, the common way used in industrial applications for collecting sensor/actuator's data to guarantee the critical time requirement[9]. At the same time, an additional super frame can use shared slots and dedicated slots. The length of the super frame can be adapted to the needs of the application, and the slot length is fixed to 10 ms. The ISA100.11a-2009 supports configurable timeslot length. There is an extension shim for frequency hopping and slotted hopping. It has slotted hoping and slow hopping mechanisms. The carrier sensing scheme can be disabled to reduce possible delay transmission.

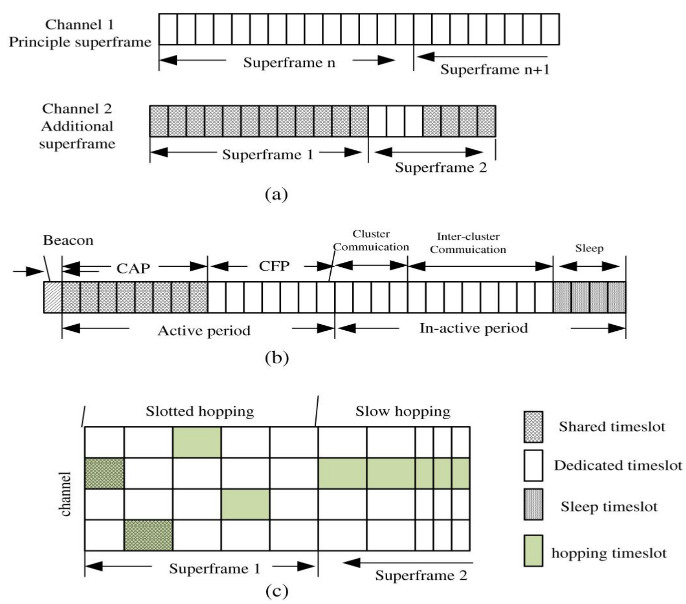

Fig. 3. Superframe structure of the mainstream IWSN standards: (a) Wireless HART (b) WIA-PA (c) ISA100.11a

WIA-PA is a cross-layer design. Its super frame has seven stages: beacon period, cluster communications, application period, request to restore the stage, free, cluster communication, and network detection, respectively. It supports the frequency hopping slots, the TDMA and CSMA hybrid channel access mechanism. Taxonomy of the MAC protocols in WSN, which divides the WSN into asynchronous and synchronous (slotted). The asynchronous latency and its affecting factors are analyzed. It uses processing delay, propagation delay, queue delay, transmission delay, channel access delay, and reception delay to describe the one hop delay. Similarly, sum of multi-hop delays would be used to calculate the end-to-end delay. Packet access latency (T_i) of MAC is the delay caused by the packet in queue and the delay caused by slot completion. Queue delay (T_q) is the time period taken from the time a packet generated to the packet at the head of the queue. Slot competition delay (T_c) is the time period taken from the time the packet at the head of the queue to the time who wins the right to send the packet in its slot. There is CAP and CFP phase. In CAP phase, every slot, all nodes with data sending will contend. If it lost the competition, it will wait a random number (T_c) of slots before it comes back to contend again. Its delay equals to N slots. Thus, $T_i = T_q + T_c$. We consider total end-to-end delay is having components such as queuing delay at each cluster, with usual star topology based structure across each cluster. At the entry point the delay is due to sensor nodes within this origin cluster. Next at the PAN coordinator which forwards the packet to the next PAN coordinator, the packet has to compete with all other packets within this cluster and also with other sensors in this intermediate cluster. With converge cast type of forwarding to base station, this would result in delay growing as the packet moves over downstream clusters towards the sink. We consider the simple Poisson model of sensor data flowing in the origin cluster and traffic from other sensors in new clusters is considered as a background traffic which is also modelled as Poisson traffic. A simple decomposed M/M/1 queue model is constructed with appropriate traffic intensities. This analytical end-to-end delay will be compared with simulation.

III.SIMULATION MODEL OF CLUSTER TREE NETWORK

We use ns-3 simulator in order to analyse the mean end-to-end delay over the cluster tree network. The working of a super frame is composed of Queue simulation, CSMA/CA simulation, and GTS simulation. During a super frame, the sensor nodes in WSNs have executed CSMA/CA simulation N_{CAP} times, before it executes GTS simulation. Similarly, the GTS simulation will execute N_{GTS} times. Using the results of simulation, we can know what the kind of super frame structure can minimize the system packet latency (D_S).The CSMA/CA simulation uses a random number to determine which node in WSNs has the ability to access slot in the super frame. A linked list is applied to simulate the set of sensor in WSNs. The sensor network is simulated using a linked list. As all nodes have equal right to obtain a CAP slot, an equally distributed random number is used to decide which node has the privilege to send its packet. For instance, suppose that there are four devices each having a packet to send in the WSN, i.e. There are four nodes in the linked list.

Simulator generates a random number from one to four. If number two is selected by the random generator, representing that node at position two in the list who is able to send the packet at the head of its queue. Furthermore, the selected queue head packet's wait time is represented by the CAP delay T_C of this packet. Meantime, other packets in all the queues set the increment by 1 to their waiting time (nWaitSlot) accordingly. Since there are N_{CAP} slots in a superframe, the CSMA/CA simulation would be executed N_{CAP} times. For GTS packet, it is not really generated at this superframe period. Any GTS requirement generated at the last superframe period or early. After the GTS requirement has contended in some CAP slot in last superframe and send to the coordinator, the coordinator then allocates scheme and shows in the beacon slot of this superframe. The device will arrange and send according to the allocated slots in this superframe. Therefore, suppose there is g number GTS packet, the total delay for one GTS packet is $T_{s'} = T + T_c + L$. Sending one GTS packet needs at least two CAP slot. One slot sends request and one slot gets the acknowledgement. The number for total valued packet is TotalPacketNumber-2g. Unlike CSMA/CA in which sending a packet is not guaranteed, in GTS period, after having been allocated one of GTS, the device is guaranteed to be able to transmit its head queue packet.

IV.RESULTS

Setting BO and SO is one of the most important tasks of the PAN coordinator. In this part, we examine the impact of BO and SO on the performance of slotted CSMA/CA.

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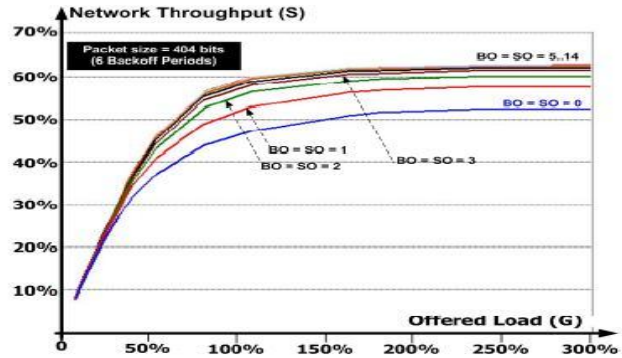

Fig. 4. The network throughput as a function of the Offered load for different (BO, SO) values

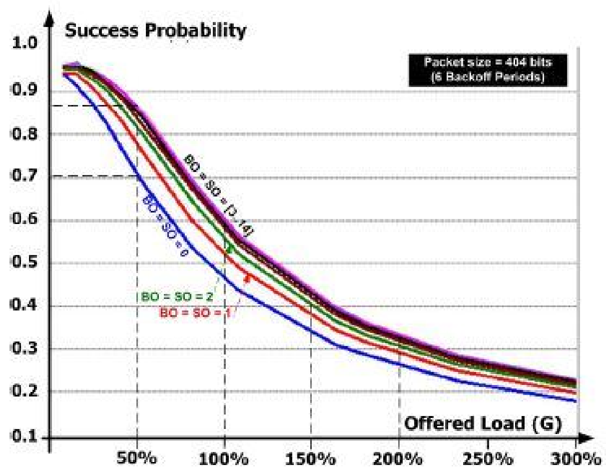

Fig. 5. Success probability as a function of the offered Load for different (BO, SO) values

For the evaluation of end-to-end delay we have selected the following parameters.

TABLE I
SIMULATION PARAMETERS

S. No.	Name	Number
1	Number of Clusters	6
2	Number of Sensors in each cluster	16
3	Queue Length	5
4	Packet Generating Interval	8 slots

TABLE III
THEORETICAL AND SIMULATION VALUES COMPARISON

Slot	Theory	Simulation
22	2183	2190
23	2357	2359
24	2518	2522
25	2874	2834
26	3206	3182

From the results shown in Table II, we can observe that before 25 slots, the average network latency is same. After 25 slots, for the network latency, program value is lower than theory value. The reason is that we calculate the theory value using some supposing. We suppose before the system buffer full condition, there is no lost of the packet. But in our simulation program, some node will always not get the slot. Its buffer will be full before the system buffer is full. The packet will be lost. Then the system packet number is smaller than theory calculation number.

V. CONCLUSIONS

The average end-to-end delay through the analysis agrees well with simulation results. We observe that when number of sensors is greater than packet generating interval, the packet latency is closely related to packet generation interval. When there is longer interval, all CAP slot will incur the lower system packet latency. In addition, we trace the packets sent by GTS slots. The result of blending, in which some slots run in CAP and others in CFP performs worse than pure CAP or pure CFP. We also noted exchanging the CAP model with CFP mechanism may provide a better model.

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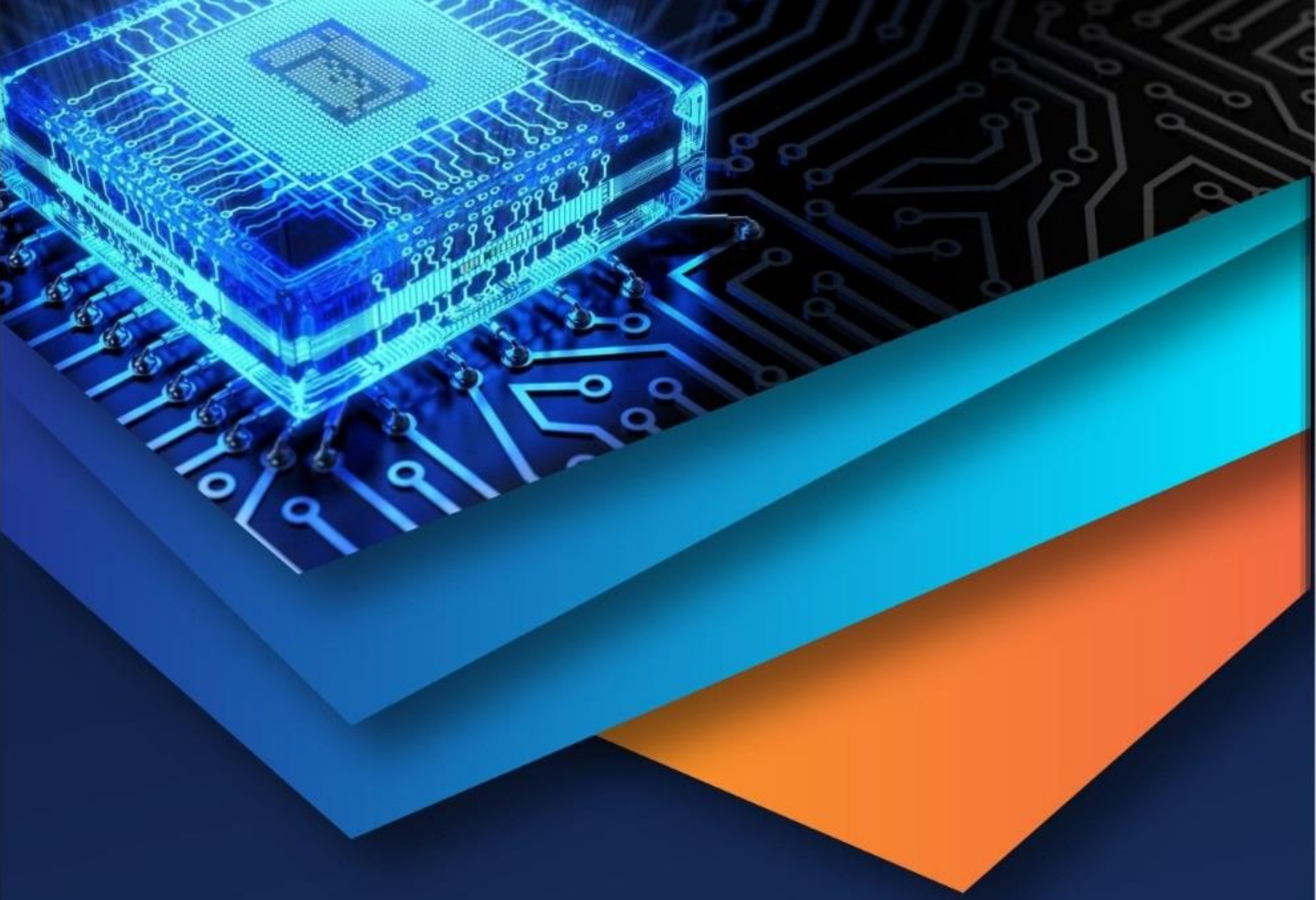

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