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Performance Analysis of Asymmetrical Cascaded Multilevel DC Link Inverter using Unipolar Modulation Techniques

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Abstract: ***This paper presents single-phase thirteen level asymmetrical cascaded multilevel DC-link (ACMLDCL) inverter using unipolar modulation techniques fed R and RL loads. The proposed ACMLDCL inverter consists of two stages. The first stage of the inverter consists of multiple half-bridge inverter cells with two switches and a single DC source. All half-bridge inverter cells are connected in a cascaded mode. The inverter performance can be enhanced by selecting the proper values of the DC sources. The second stage of the inverter circuit consists of full bridge circuit operating at a fundamental frequency. Compared with conventional cascaded H-bridge multilevel inverter the proposed ACMLDCL topology has the advantages of reduced switch count, size, cost, modularity and flexibility to increase the number of stages without changing structure of the first stage. The proposed topology can have the improved performance by implementing modulation techniques. This paper presents two unipolar modulation techniques, namely, sub-harmonic and modified space vector modulating techniques to validate the proposed ACMLDCL inverter. The validity of the proposed ACMLDCL inverter is verified in terms of total harmonic distortion (THD) and fundamental output phase voltage using Matlab/Simulink.***
Keywords: MLI's, ACMLDCL Inverter, USMT, UMSVMT, THD

I. INTRODUCTION

The Multilevel inverters (MLI's) are most promising device in ac power drives when higher power ratings are required with limited harmonic content. The MLI's offers several advantages as compared to the conventional inverters, such as, lower dv/dt, low magnetic interference, high efficiency and operates at high voltage etc. There are three types of the traditional MLI's, namely diode-clamped, flying capacitor and cascaded H-bridge MLI's. Among these three types, cascaded H-bridge MLI widely used for many applications such as electrical drives and renewable energy systems etc. due to its modular structure and requires less number of components as compared to other two topologies [1-2].But the traditional MLI's are required more number of components to increase the number of levels. So, the requirement of heat sinks, protection circuits and driver circuits are increased accordingly, so that it leads to increase in size, cost and complexity [3-4]. In order to overcome these difficulties, a reduced component count topologies are introduced. Generally, design of a new topology follows three categories such as structural modification and the placement of asymmetric DC source instead of symmetric DC source. The terms symmetric and asymmetric are the most well-known words in MLI topology. If the values of all the DC sources of MLI topology have the same magnitude it is called symmetric whereas asymmetric have unequal DC source value. Every topology has its own advantages and disadvantages. In this paper, analysis of the ACMLDCL inverter is addressed [5-6].

This paper presents a single-phase thirteen level ACMLDCL inverter based on an half-bridge and a full bridge inverter circuits. Compared with the traditional MLI's, the proposed ACMLDCL inverter can have the enhanced performance by implementing the modulating techniques [7-8]. This paper presents the unipolar sub harmonic modulating technique (USHMT) and unipolar modified space vector modulating technique (UMSVMT). The proposed ACMLDCL inverter can significantly reduce the switch count as well asthe number of gate drivers as the number of voltage levels increases [9].

II. ASYMMETRIC CASCADED MULTILEVEL DC LINK INVERTER TOPOLOGY

The proposed Thirteen Level ACMLDCL inverter circuit is shown in fig. 1 with an unequal DC voltage source with a ratio of 1:2:3. The corresponding values of dc voltage sources are to be chosen using equation (1).

$$V_{dci} = i*V_{dc}\text{ , where i = 1,2 and 3} \qquad (1)$$

The maximum value of the output voltage is obtained using equation (2).

$$V_{max} = \sum_{i=1}^{S} V_{dci} \qquad (2)$$

The number of output voltage levels can be obtained using the equation (3) and the number of switches for the proposed ACMLDCL inverter can be obtained by using equation (4). Therefore, the proposed thirteen level ACMLDCL inverter consists of three voltage sources, one full bridge inverter and ten switches [10].

$$N_{Levels} = (2^{n+1} - 3)^{F} \qquad (3)$$

$$N_S = 2\,(n_1+n_2+\ldots\ldots n_n) + 4F \qquad (4)$$

Where 'n' is the number of voltage sources and 'F' is the number of full bridge circuits.

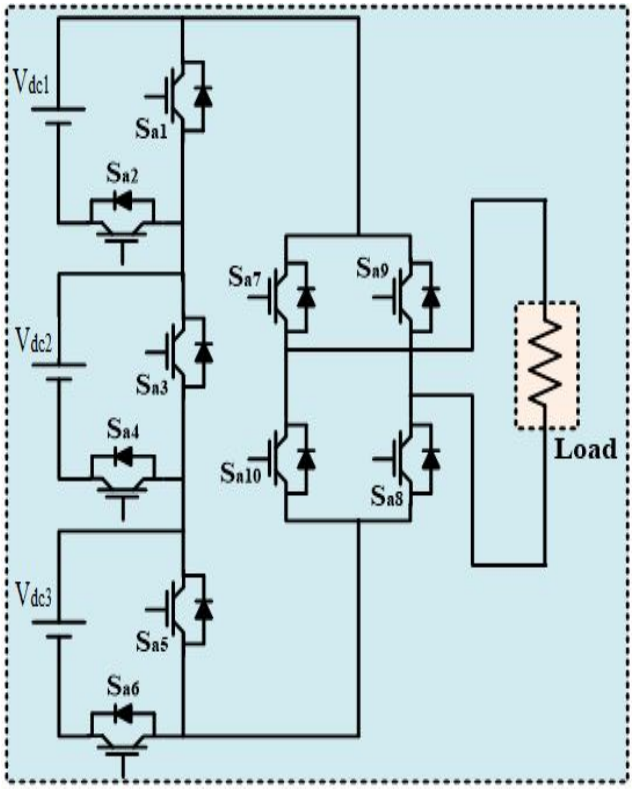

Fig.1. Proposed ACMLDCL inverter (13-level)

The operation of the proposed thirteen level ACMLDCL inverter explained in different modes of operation as follows and the corresponding output voltage is shown in figure 2.

Mode 1: Conduct the switches S_2, S_4, S_6, S_7 and S_8 to generate + 6 V_{dc}
Mode 2: Conduct the switches S_1, S_4, S_6, S_7 and S_8 to generate + 5 V_{dc}
Mode 3: Conduct the switches S_2, S_3, S_6, S_7 and S_8 to generate + 4 V_{dc}
Mode 4: Conduct the switches S_1, S_3, S_6, S_7 and S_8 to generate + 3 V_{dc}
Mode 5: Conduct the switches S_1, S_4, S_5, S_7 and S_8 to generate + 2 V_{dc}
Mode 6: Conduct the switches S_2, S_3, S_5, S_7 and S_8 to generate + V_{dc}
Mode 7: Conduct the switches S_2, S_3, S_5, S_9 and S_{10} to generate – V_{dc}
Mode 8: Conduct the switches S_1, S_4, S_5, S_9 and S_{10} to generate – 2 V_{dc}
Mode 9: Conduct the switches S_1, S_3, S_6, S_9 and S_{10} to generate – 3 V_{dc}
Mode 10: Conduct the switches S_2, S_3, S_6, S_9 and S_{10} to generate – 4 V_{dc}
Mode 11: Conduct the switches S_1, S_4, S_6, S_9 and S_{10} to generate – 5 V_{dc}
Mode 12: Conduct the switches S_2, S_4, S_6, S_9 and S_{10} to generate – 6 V_{dc}

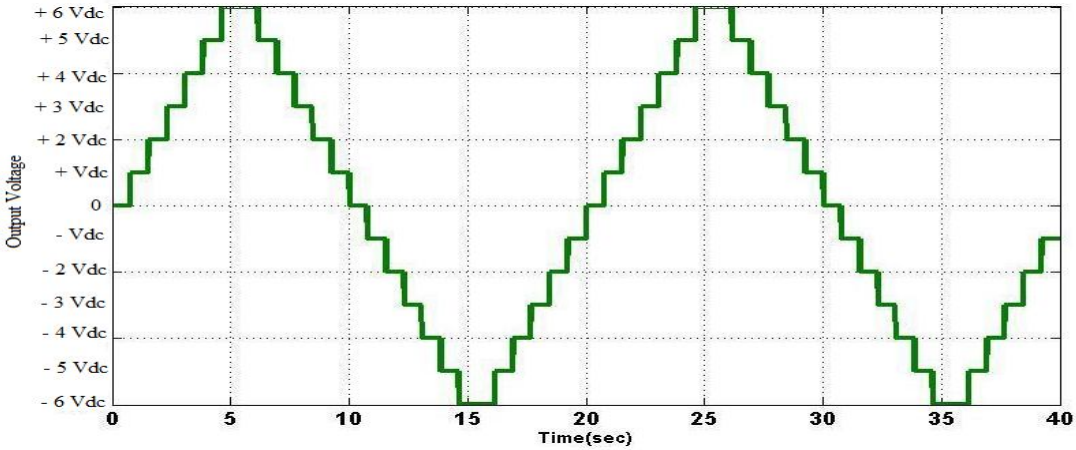

Fig.2. Output voltage of the proposed thirteen level ACMLDCL inverter using constant pulses

III.MODULATION TECHNIQUES

Modulation techniques are mainly classified into three types, namely fundamental switching frequency, space vector vector and carrier based modulation techniques. Among all the pulse width modulation methods for MLI's, carrier based modulation techniques and space vector control are often used but when the number of output level is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based modulation techniques are preferred under this condition in MLI's. This paper focuses on unipolar carrier based sub-harmonic and modified space vector modulation techniques which have been extended for use in MLI topologies by using multiple carriers [11].

Unipolar carrier type modulation techniques are employed to trigger the switches of first stage of the proposed ACMLDCL inverter and the fundamental switching frequency is used to generate the pulses for the full bridge inverter circuit. For an m-level of ACMLDCL inverter the proposed modulation requires (m-1)/2 carriers with the same amplitude and frequency, therefore for the thirteen level ACMLDCL inverter, six carriers are used to generate the firing pulses and all the carrier signals will have same amplitude and frequency but the carrier signals are shifted in levels. All the carrier signals will be in-phase [12].

A. Unipolar Sub-harmonic Modulation Technique (USMT):

The pattern of in-phase triangular carrier based level shifted technique is used to generate firing pulses to power switches of thirteen level ACMLDCL inverter using USMT is shown in Figure 3.

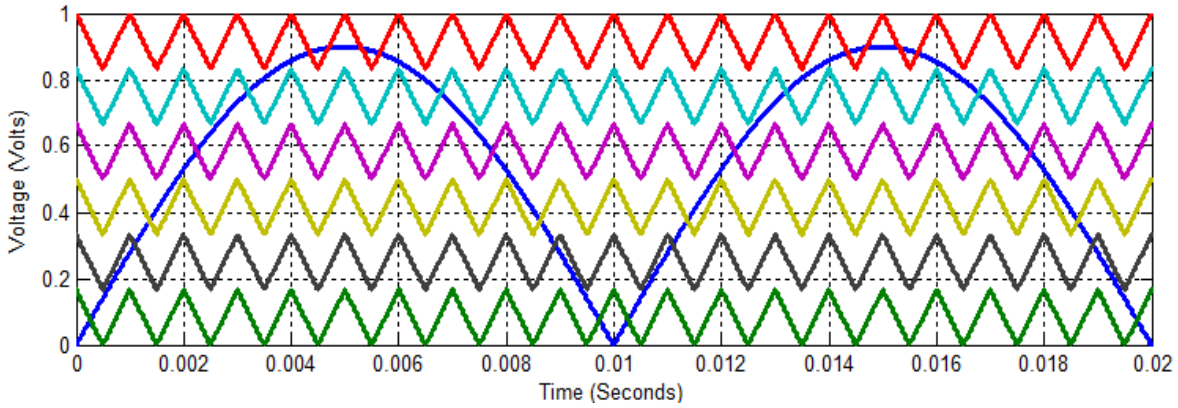

Fig.3. Pulse generation of the proposed ACMDCL inverter using USMT

B. Unipolar modified space vector modulation technique (umsvmt)

To obtain the maximum possible peak amplitude of the fundamental phase voltage, a offset voltage, Voffset1, is added to the reference phase voltages to generate the USVMT waveform, where the magnitude of Voffset1 is given by equation (5). The pattern of in-phase triangular carrier based level shifted technique is used to generate firing pulses to power switches of thirteen level ACMLDCL inverter using UMSVMT is shown in Figure 4.

$$V_{offset1} = \frac{-(V_{max} + V_{min})}{2} \quad \text{-- (5)}$$

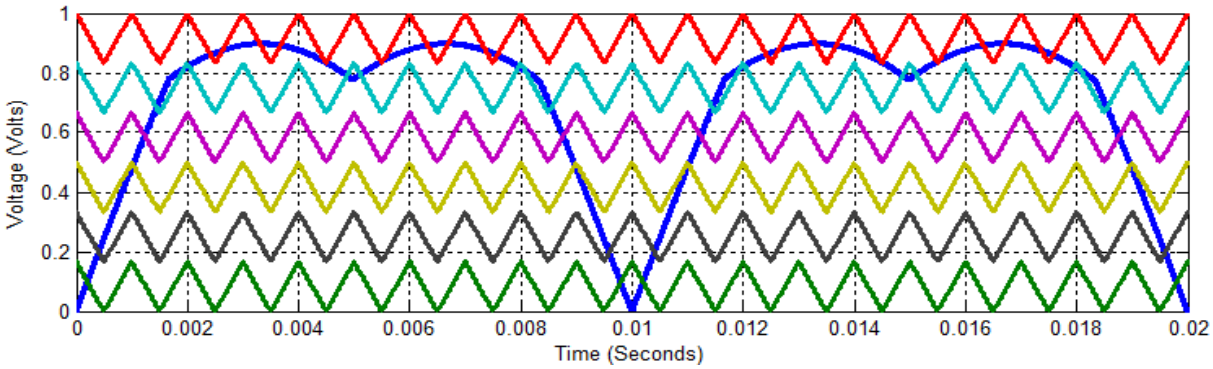

Fig.4. Pulse generation of the proposed ACMDCL inverter using UMSVMT

IV. SIMULATION RESULTS

The Simulation was conducted to verify the operation of the proposed single phase thirteen level ACMLDCL inverter using USPM and MSVPM Techniques fed R and RL-loads. The parameters used to simulate the proposed models are depicted in table 1.

TABLE I. SYSTEM PARAMETERS

Parameter	Value
Resistance Load	50 Ohms
Inductance Load	100 mH
Voltage ratios (V_{dc1}, V_{dc2}, V_{dc3})	50 V, 100 V and 150 V
Switching frequency	5 kHz
Modulation index	0.866

A. Unipolar Sub-harmonic Modulation Technique (USMT):

Fig. 5 and 7 shows the single-phase thirteen level output phase voltage and current of proposed ACMLDCL inverter using USMT fed R-load with a modulation index of 0.866 and Fig.6 and 8 shows the corresponding THD analysis, from the Fig's 6 and 8 it is noticed that the harmonic distortion of 11.88 % is present in phase voltage and phase current of proposed ACMLDCL inverter.

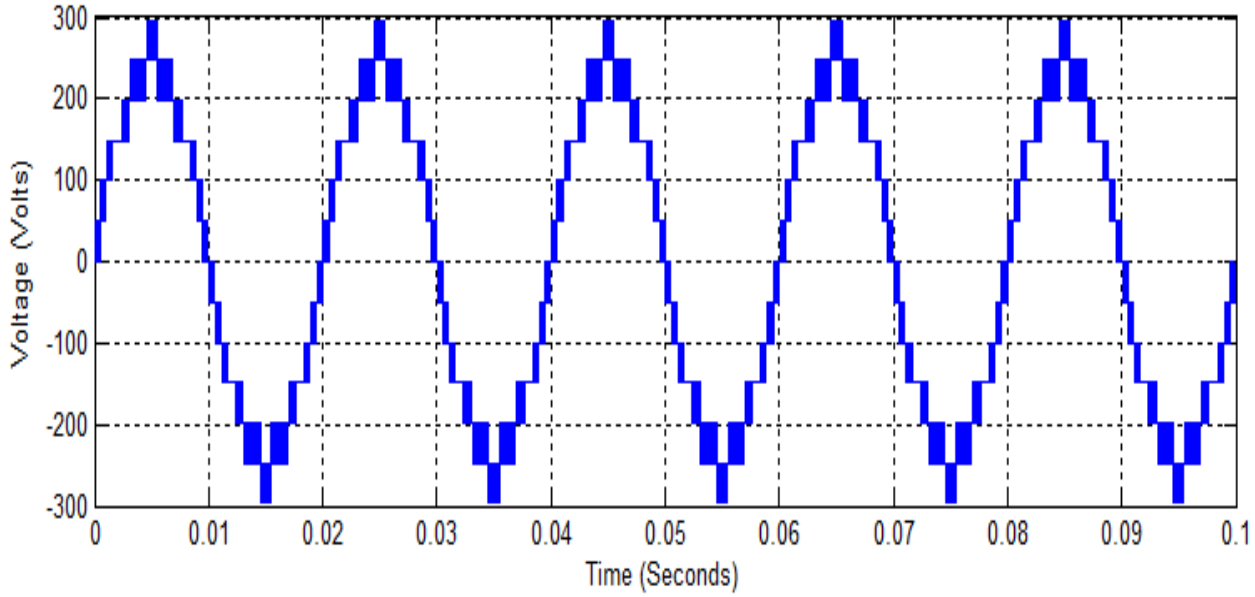

Fig. 5 Output phase voltage of single phase thirteen level ACMLDCL using USMT with R-Load

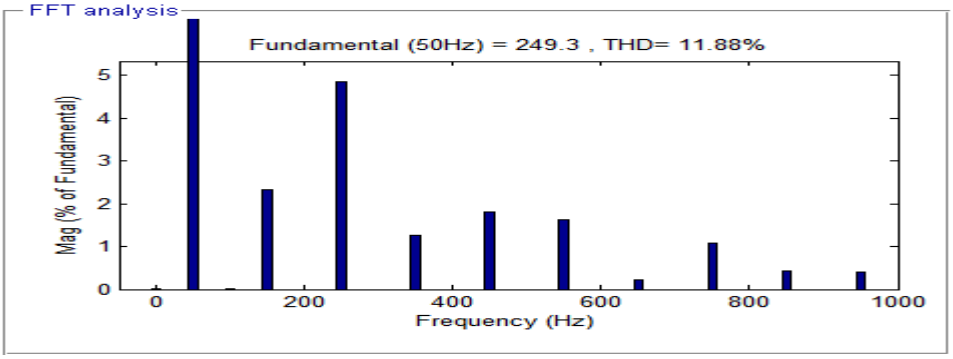

Fig. 6 Phase voltage THD of single phase thirteen level ACMLDCL using UMSVMT with R-Load

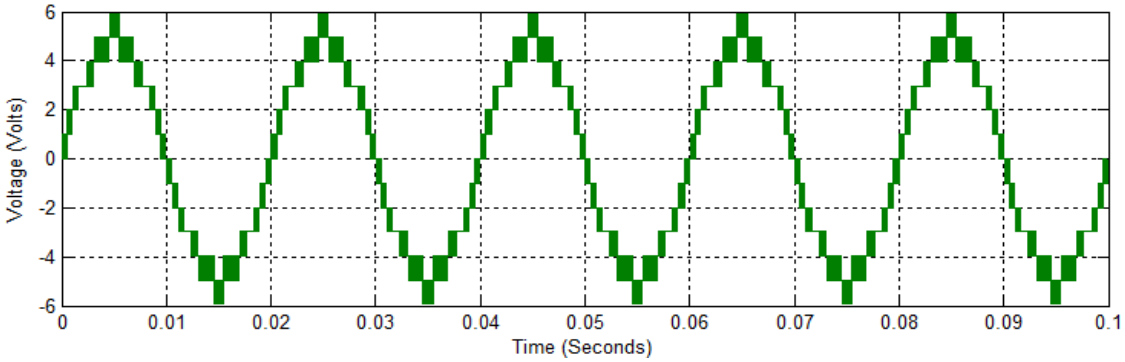

Fig. 7 Output phase current of single phase thirteen level ACMLDCL using USMT with R-Load

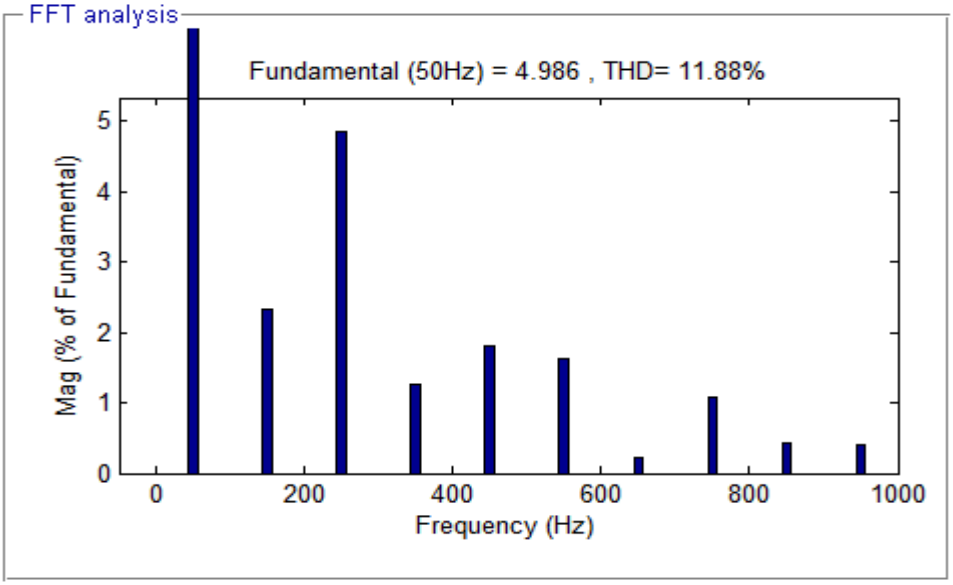

Fig. 8 Phase current THD of single phase thirteen level ACMLDCL using USMT with R-Load

Fig. 9 and 11 shows the single-phase thirteen level output phase voltage and current of proposed ACMLDCL inverter using USMT fed RL-load with a modulation index of 0.866 and Fig.10 and 12 shows the corresponding THD analysis, from the Fig's 10 and 12 it is noticed that the harmonic distortion of 11.93 % is present in phase voltage and 2.24 % in phase current of proposed ACMLDCL inverter.

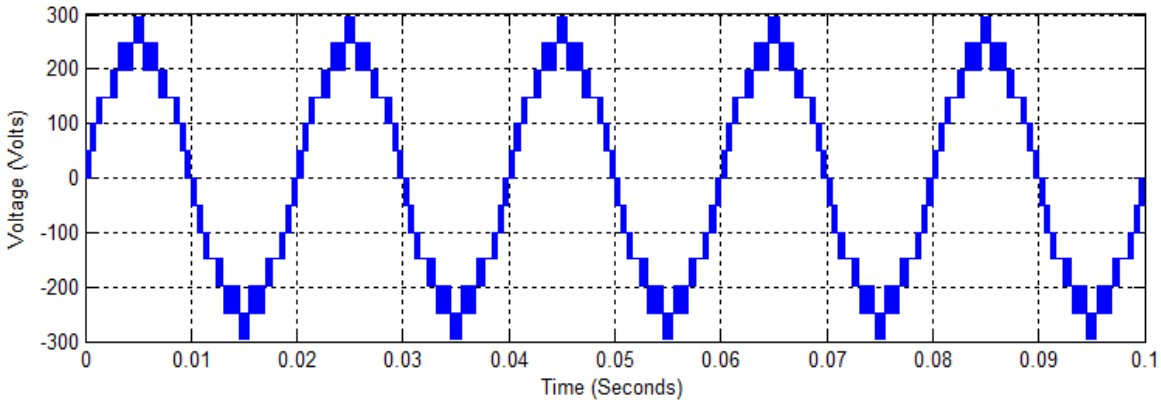

Fig. 9 Output phase voltage of single phase thirteen level ACMLDCL using USMT with RL-Load

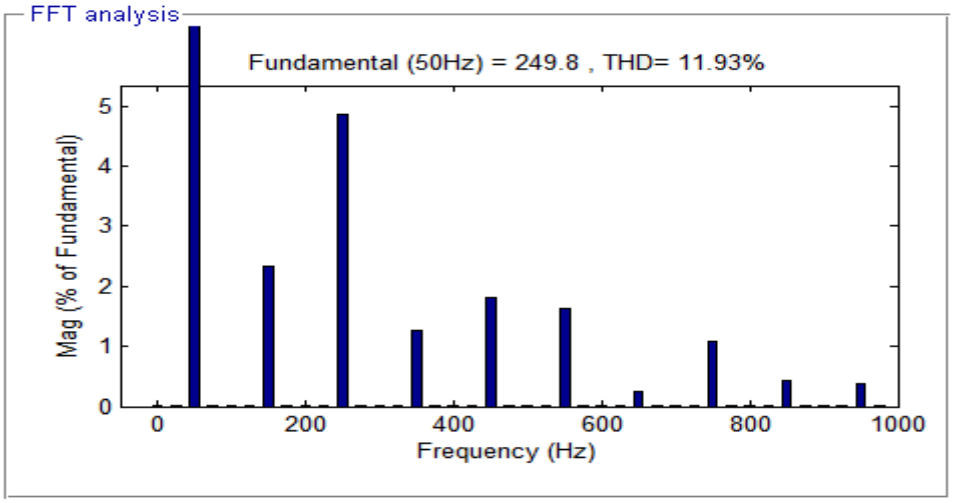

Fig. 10 Phase voltage THD of single phase thirteen level ACMLDCL using UMSVMT with RL-Load

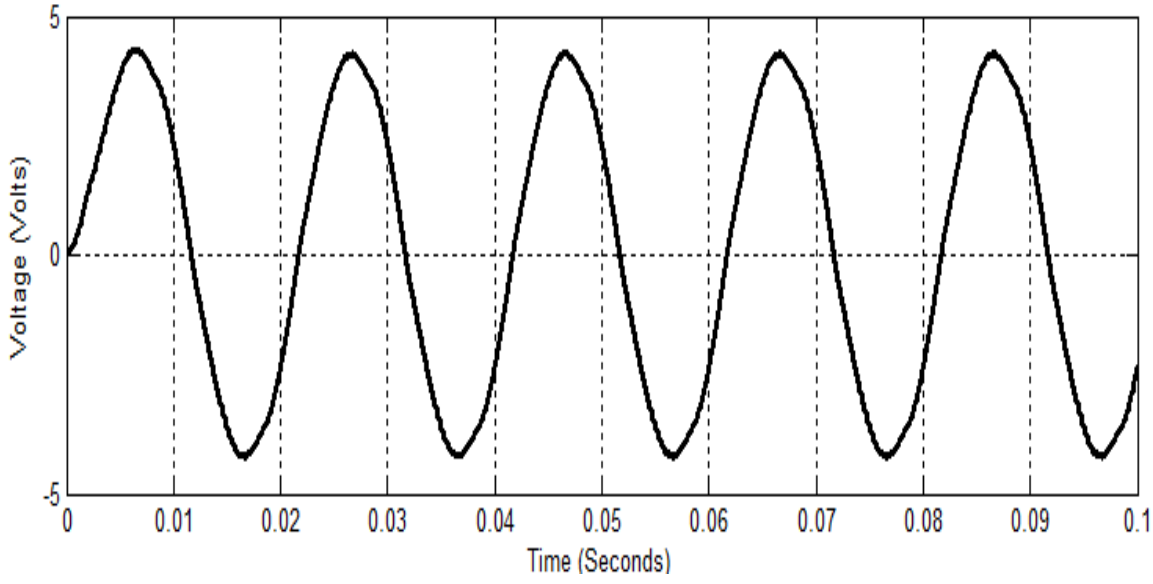

Fig. 11 Output phase current of single phase thirteen level ACMLDCL using USMT with RL-Load

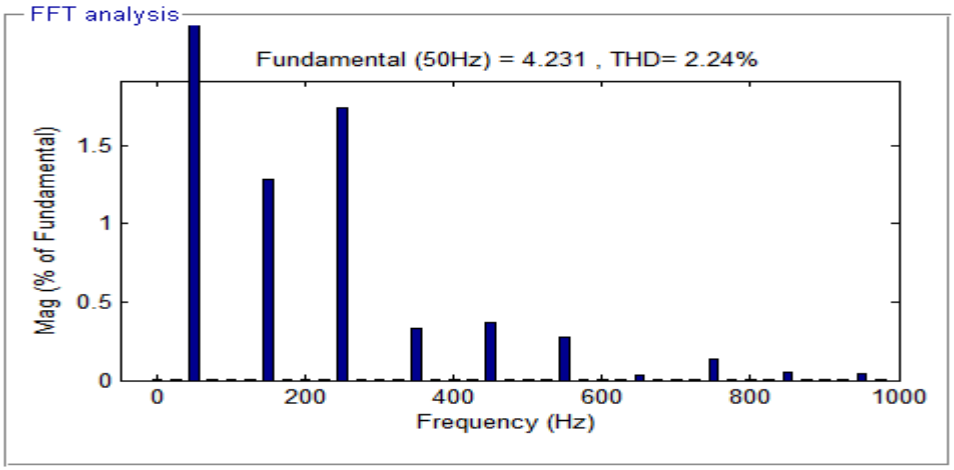

Fig. 12 Phase current THD of single phase thirteen level ACMLDCL using USMT with RL-Load

B. Unipolar Modified Space Vector Modulation Technique (UMSVMT):

Fig. 13 and 15 shows the single-phase thirteen level output phase voltage and current of proposed ACMLDCL inverter using UMSVMT fed R-load with a modulation index of 0.866 and Fig.14 and 16 shows the corresponding THD analysis, from the Fig's 14 and 16 it is noticed that the harmonic distortion of 10.30 % is present in phase voltage and phase current of proposed ACMLDCL inverter.

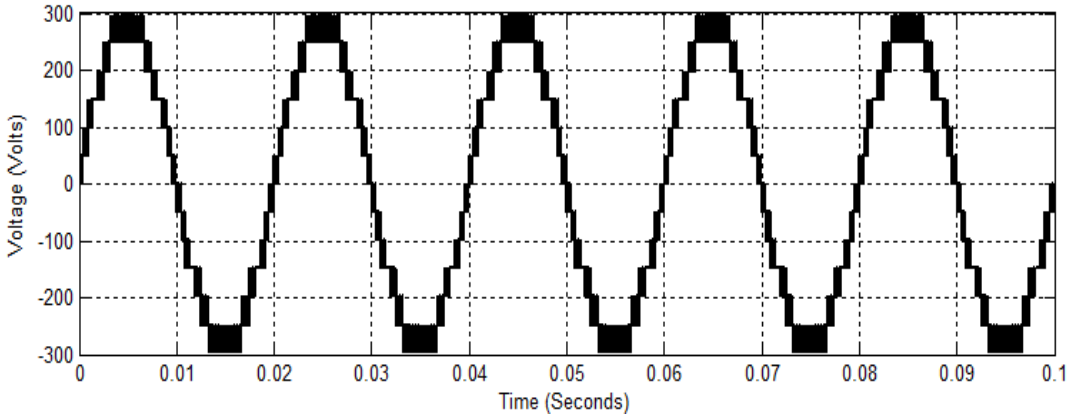

Fig. 13 Output phase voltage of single phase thirteen level ACMLDCL using UMSVMT with R-Load

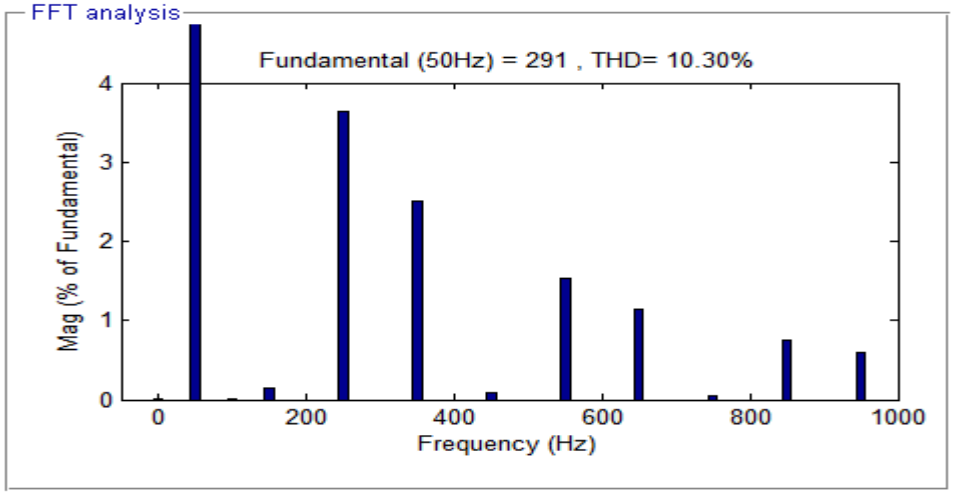

Fig. 14 Phase voltage THD of single phase thirteen level ACMLDCL using UMSVMT with R-Load

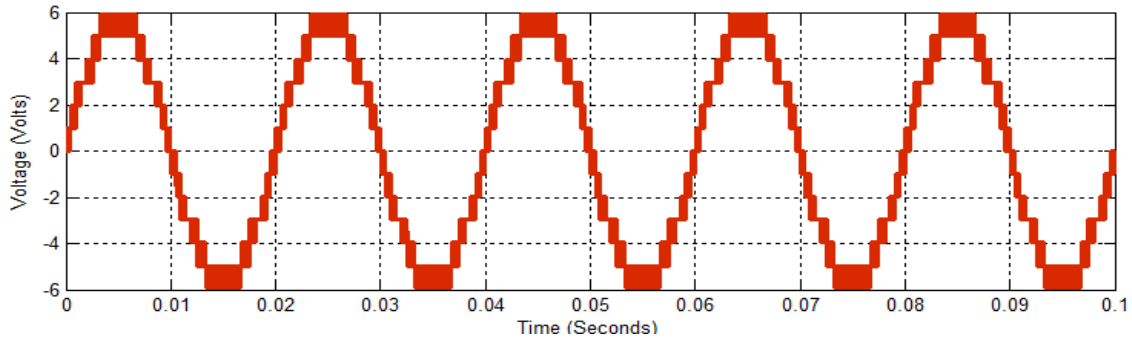

Fig. 15 Output phase current of single phase thirteen level ACMLDCL using UMSVMT with R-Load

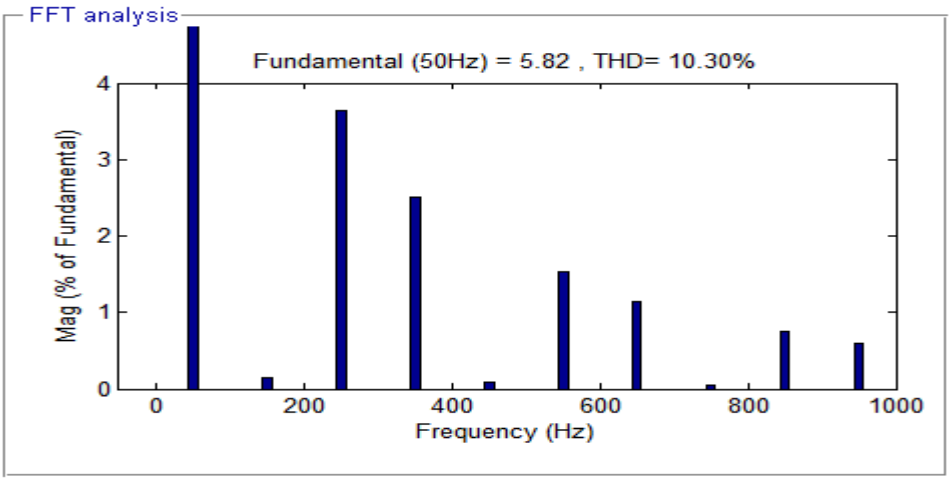

Fig. 16 Phase current THD of single phase thirteen level ACMLDCL using UMSVMT with R-Load

Fig. 17 and 19 shows the single-phase thirteen level output phase voltage and current of proposed ACMLDCL inverter using UMSVMT fed RL-load with a modulation index of 0.866 and Fig.18 and 20 shows the corresponding THD analysis, from the Fig's 18 and 20 it is noticed that the harmonic distortion of 10.35 % is present in phase voltage and 1.51 % in phase current of proposed ACMLDCL inverter.

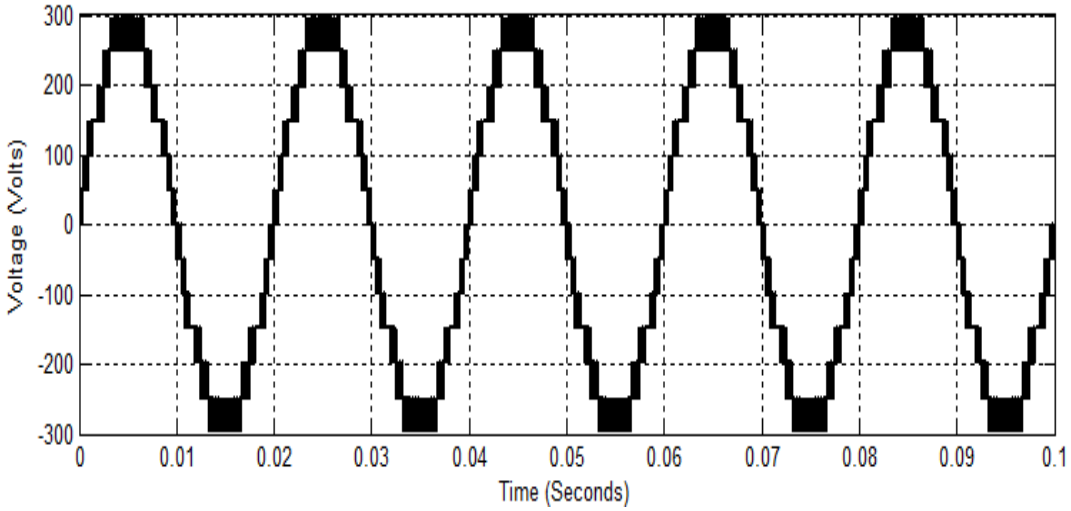

Fig. 17 Output phase voltage of single phase thirteen level ACMLDCL using UMSVMT with RL-Load

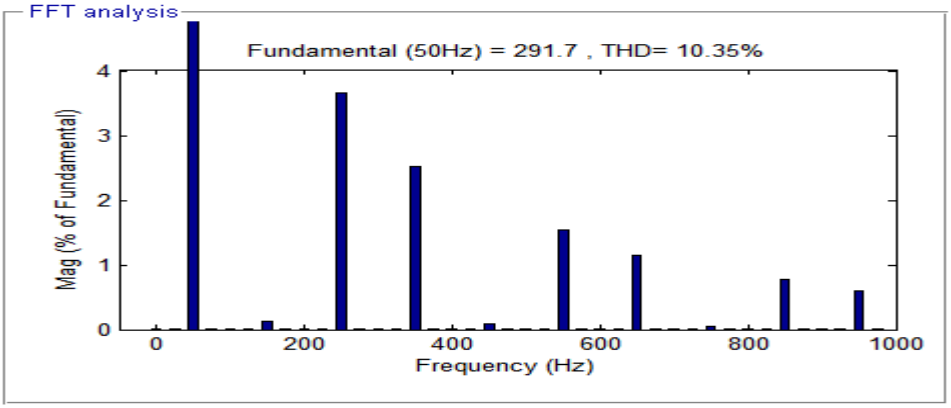

Fig. 18 Phase voltage THD of single phase thirteen level ACMLDCL using UMSVMT with RL-Load

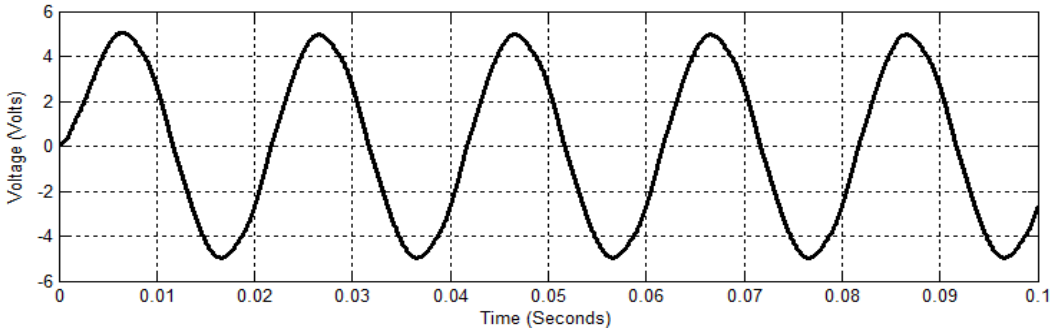

Fig. 19 Output phase current of single phase thirteen level ACMLDCL using UMSVMT with RL-Load

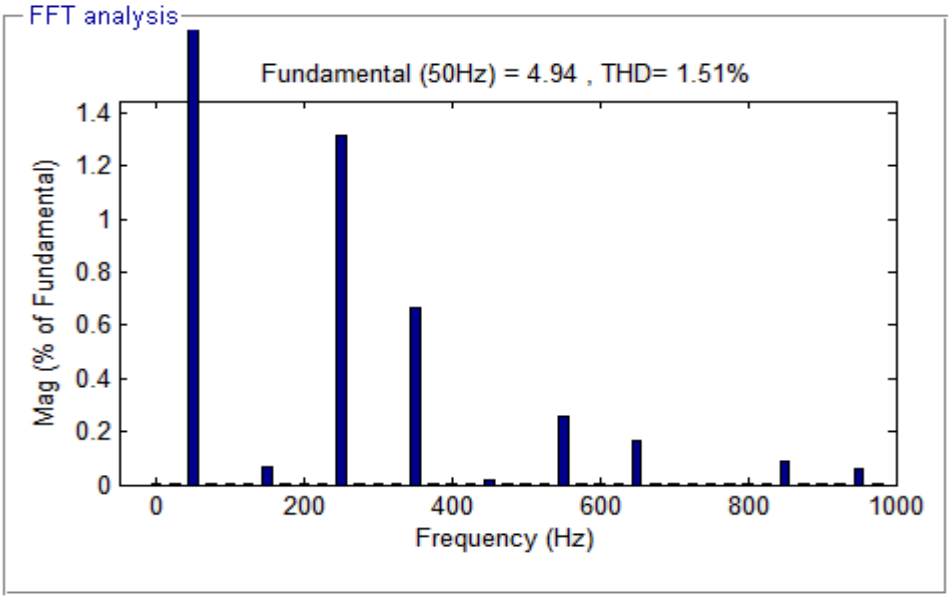

Fig. 20 Phase current THD of single phase thirteen level ACMLDCL using UMSVMT with RL-Load

V. COMPARISON OF RESULTS

A summary of THD and fundamental output voltage of proposed single phase thirteen level ACMLDCL inverter with their modulating techniques are presented in table 2 using USMT and modified UMSVMT with unipolar triangular carriers and it is concluded that proposed ACMLDCL inverter using UMSVMT has given good fundamental output voltage with less THD fed R and RL-loads when compared to USM technique.

Table ii. Comparison of results

Modulating Techniques	ACMLDCL inverter fed R-Load				ACMLDCL inverter fed RL-Load			
	Output Voltage (V)	Voltage THD (%)	Output Current (A)	Current THD (%)	Output Voltage (V)	Voltage THD (%)	Output Current (A)	Current THD (%)
USMT	249.3	11.88	4.98	11.88	249.8	11.93	4.23	2.24
UMSVMT	291	10.30	5.82	10.30	291.7	10.35	4.94	1.51

VI. CONCLUSION

The presented thirteen level ACMLDCL inverter can significantly eliminates half the number of switches, gate drivers compared with the traditional MLI counterparts. Despite a higher total VA rating of the switches, the proposed ACMLDC inverter is cost less due to the savings from the eliminated gate drivers and from fewer assembly steps because of the substantially reduced number of components, which also leads to a smaller size and volume. The operational principles of the proposed thirteen level ACMLDCL inverter are explained in detail and also the modulation techniques are employed successfully.

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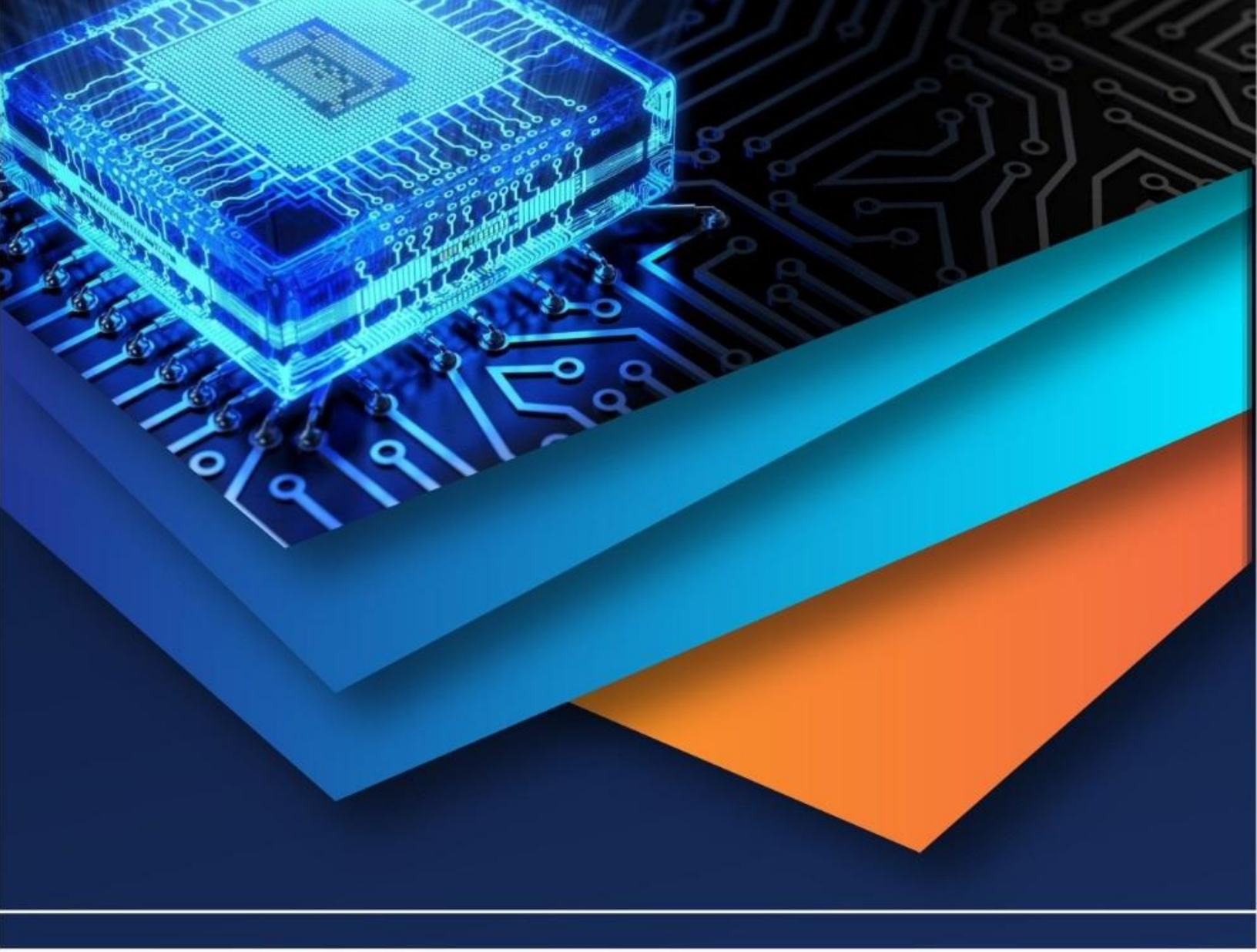

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