iJRASET
International Journal For Research in Applied Science and Engineering Technology

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

**Volume:** 6 **Issue:** II **Month of publication:** February 2018

**DOI:** http://doi.org/10.22214/ijraset.2018.2135

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
*ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887*
*Volume 6 Issue II, February 2018- Available at www.ijraset.com*

# Analysis of Self-Resetting GDI Primitives and Implementation in Adder Design

S.A.Sivakumar[1], M. Haritha[2], R. Gowtham Krishna[3], A. Karthega[4]
[1]*Assistant Professor,* [2, 3, 4]*UG Scholar, Info Institute of Engineering, Coimbatore, Tamilnadu.*

***Abstract:*** ***The CMOS dynamic logic has some drawbacks such as charge leakage, high power consumption, loss of noise immunity etc. due to which there was a need of introduction of Self-Resetting Logic (SRL).Our proposed idea is to design SRGDI primitives suitable for combinational designs and implement them in 8-bit ALU. ALU is to be designed using Adders, Multiplier, Comparator and Logic Gates (AND, NAND, OR, XOR). Self-Resetting Logic reduces the switching activity and power consumption. SRLGDI primitives will be simulated using Tanner EDA with IBM 130nm CMOS technology.***
***Keywords: SRGDI, ALU, Primitives, Power, Logic gates***

## I. INTRODUCTION

Various electronic devices such as mobile phones, DSPs, ALU etc., are designed by using VLSI (Very Large Scale Integration) technology. This technology reduces the power consumption, delay, number of transistors by implementing low power techniques. Static complementary metal oxide semiconductor (CMOS) technology has been widely used by the designers due to its robustness against voltage scaling and transistor sizing [1]. The main drawbacks of static CMOS are high power dissipation and large propagation delay. This is due to the fact that the larger number of PMOS transistors end up with high input loads.

The high operating frequency also increases the power dissipation of these circuits. To overcome the drawbacks of static CMOS, there is a need of dynamic CMOS logic circuit arises for high speed applications. It offers faster switching speed and requires less no. of transistors and power consumption. It has also drawbacks like noise immunity, charge leakage. This can be resolved by Asynchronous Dynamic Circuit named Self Resetting Logic (SRL). In this paper we have explained the primitives and adder design using SRGDI logic. It reduces the switching activity and power consumption.

This paper is structured as follows: Section I provides the introduction to SRLGDI. Survey of various Types of GDI is explained in section II. Section III explains the analysis of primitives and adder design using SRGDI logic. Section IV explains the implementation of logic Gates and adders in Tanner EDA. Results and performance for newly proposed designs are compared in terms of average power and delay. Paper ends with the conclusion in section V.

## II. LITERATURE SURVEY

In this paper we survey the various types of GDI (Gate Diffusion Input) techniques and understand various pros and cons to design area efficient adder design using SRLGDI logic.

### *A. Gate Diffusion Input*

Gate diffusion input (GDI) - a new technique of low-power digital combinational circuit design. It is a structure that act as an inverter and perform various operations like AND, OR, etc. A variety of logic gates and adder design have been implemented in 130 nm technology to compare the GDI technique with CMOS and PTL [2]. The schematic of GDI is shown in fig.1.

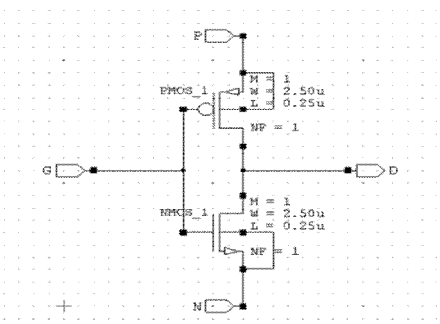



Fig.1 Structure of basic GDI cell

*B. Modified Gate Diffusion Input*

Modified Gate Diffusion Input (MGDI)-This technique is adopted from GDI technique. MGDI also consists of three input terminals G(input of both PMOS and NMOS) P(input to drain/source of PMOS) and N(input to drain /source of NMOS). In this work a modified primitive GDI logic gates have been implemented in 130nm technology and it is compared with existing GDI and CMOS logic. Its main advantage over GDI is it reduce transistor count and also area of digital circuits [3]. Like GDI this MGDI also have its drawbacks like Full Swing output voltage is not obtained in this method. The schematic of MGDI is shown in fig.2.

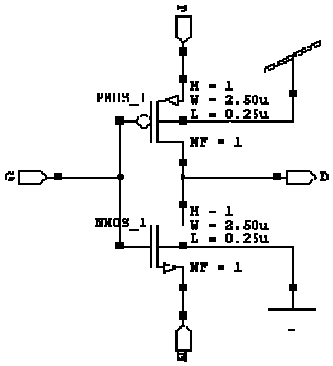



Fig.2 Structure of basic MGDI cell

*C. Full swing Gate Diffusion Input*

Full Swing Gate Diffusion Input(FSGDI)-The name full swing denotes the high speed of operation. This method is suitable for design of fast, low power circuits using a reduced number of transistors. This FSGDI have advantage over MGDI like Reduced propagation delay [4]. The Full swing output voltage is obtained in this method. Its drawbacks are Signal restoring transistor. The schematic of FSGDI is shown in fig.3 and fig.4.

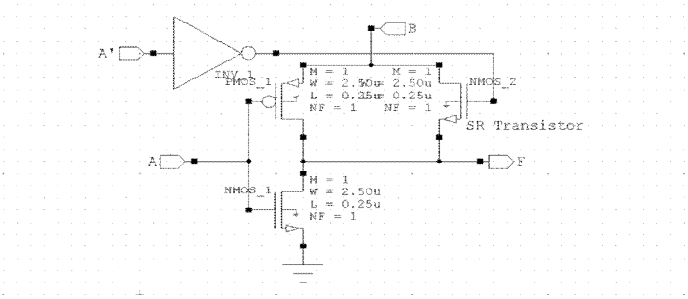



Fig.3 Structure of actual FS F1 Cell

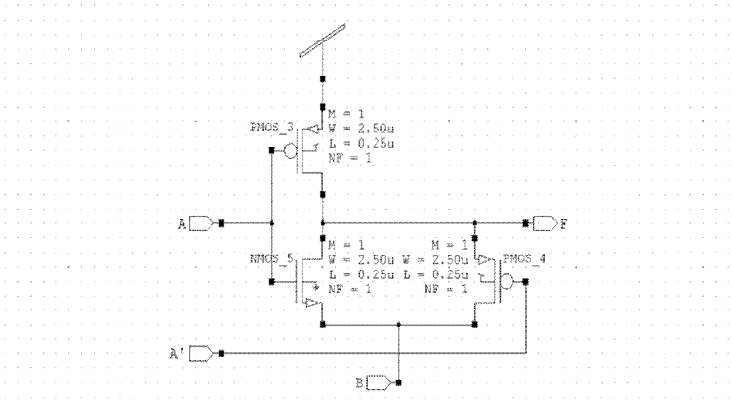



Fig.4 Structure of actual FS F2 Cell

### *D. Self Resetting Gate Diffusion Logic*

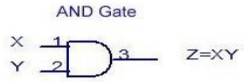
Self Resetting Gate Diffusion Input (SRGDI)-is the advanced technique used by VLSI researchers in sequential circuits. In this logic, it automatically resets the input with an given interval of clock pluses. It is a asynchronous dynamic circuit. Its advantage over other GDI techniques are it reduces switching activity and also reduces power consumption [5-8]. SRL represents signals as short-duration pulses rather than as voltage levels. The analysis of SRLGDI is done exhaustively in the following section.

## III.ANALYSIS OF SELF RESETTING GDI PRIMITIVES

The proposed SRGDI technique is focused on reduction in power consumption and switching activity over the existing technique.

### *A. And Gate*

An AND gate is an electrical circuit that combines two signals so that the output is on if both signals are present. The AND gate is a basic digital logic gate that implements logical conjunction it behaves according to the truth table. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If none or not all inputs to the AND gate are HIGH, a LOW output results. The function can be extended to any number of inputs. The truth table and primitive cell diagram of SRGDI AND gate is shown in fig.5 and fig.6 respectively.




TRUTH TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Fig.5 Truth table of AND gate

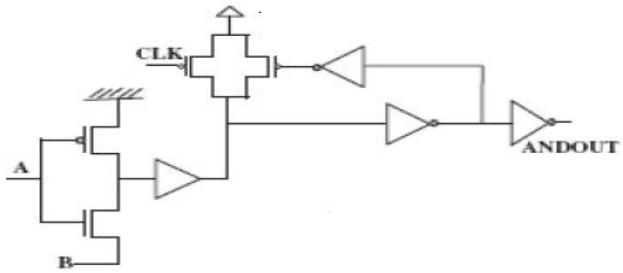



Fig.6 Primitive cell of SRGDI AND gate

The simulation of SRGDI AND primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI AND primitive cell is shown in fig.7 and fig.8 respectively.

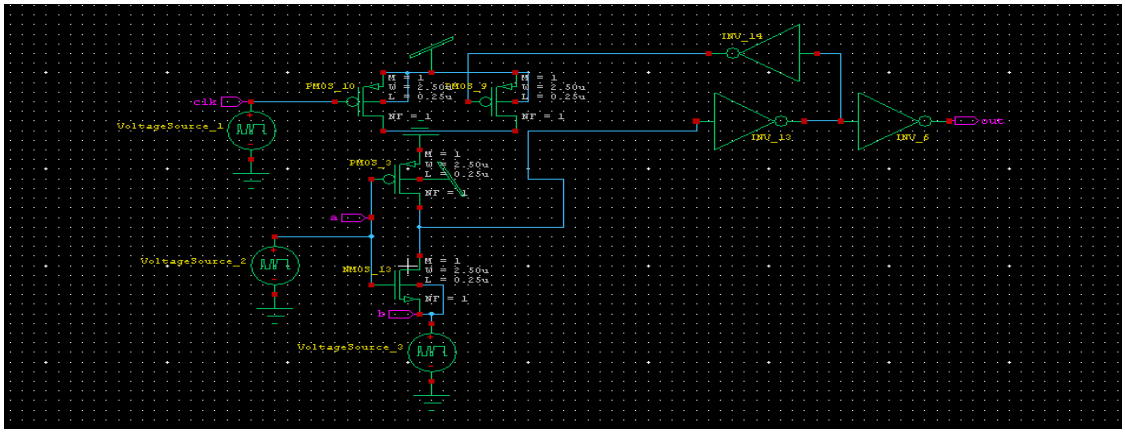



Fig.7 S-edit schematic cell of SRGDI AND gate

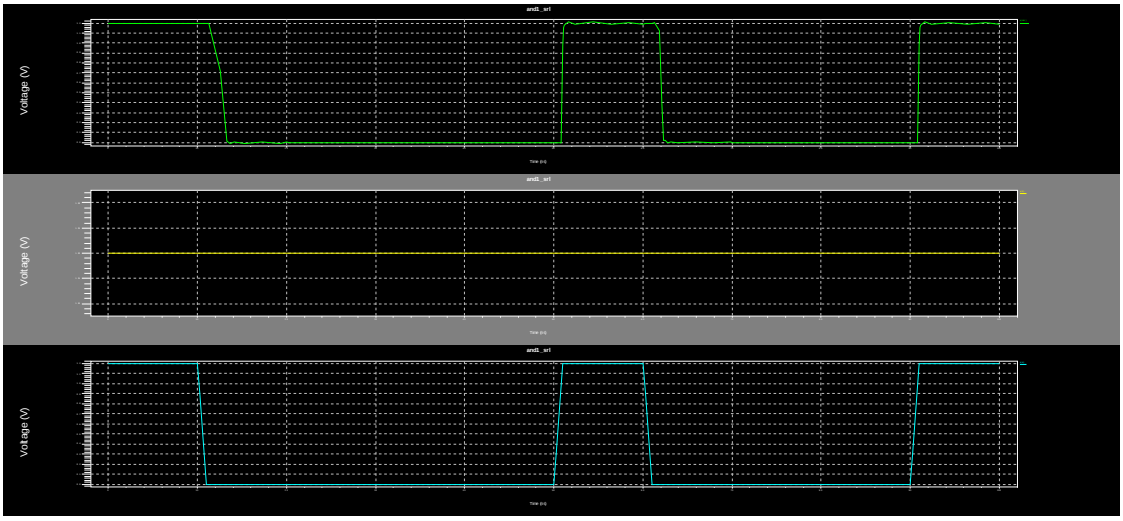
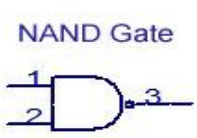



Fig.8 W-edit output waveform of SRGDI AND gate

*B. Nand Gate*

A NAND Gate is a logical gate which is the opposite of an AND logic gate. It is a combination of AND and NOT gates and is a commonly used logic gate. It is considered as a "universal" gate in Boolean algebra . It produces an output which is false only if all its inputs are true; thus its output is complement to that of the AND gate. A LOW (0) output results only if both the inputs to the gate are HIGH (1), if one or both inputs are LOW (0), a HIGH (1) output results [9]. The truth table and primitive cell diagram of SRGDI NAND gate is shown in fig.9 and fig.10 respectively.




TRUTH TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Fig.9Truth table of NAND gate

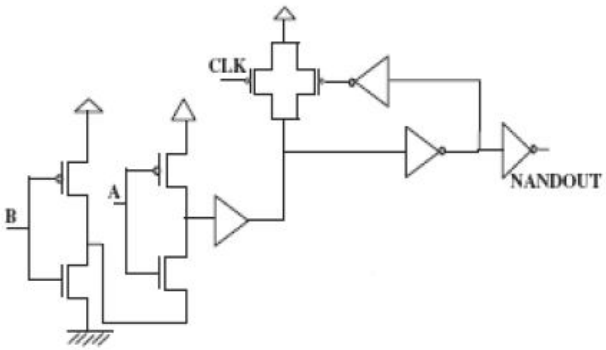



Fig.10 Primitive cell of SRGDI NAND gate

The simulation of SRGDI NAND primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI NAND primitive cell is shown in fig.11and fig.12 respectively.

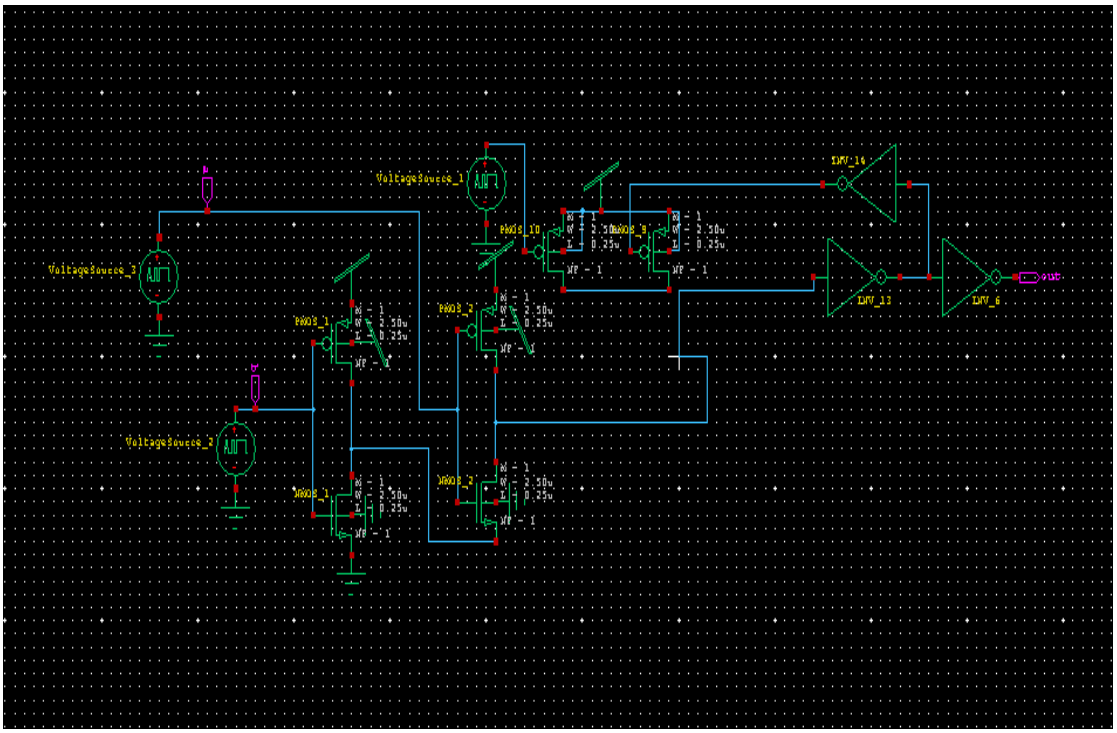


Fig.11S-edit schematic cell of SRGDI NAND gate

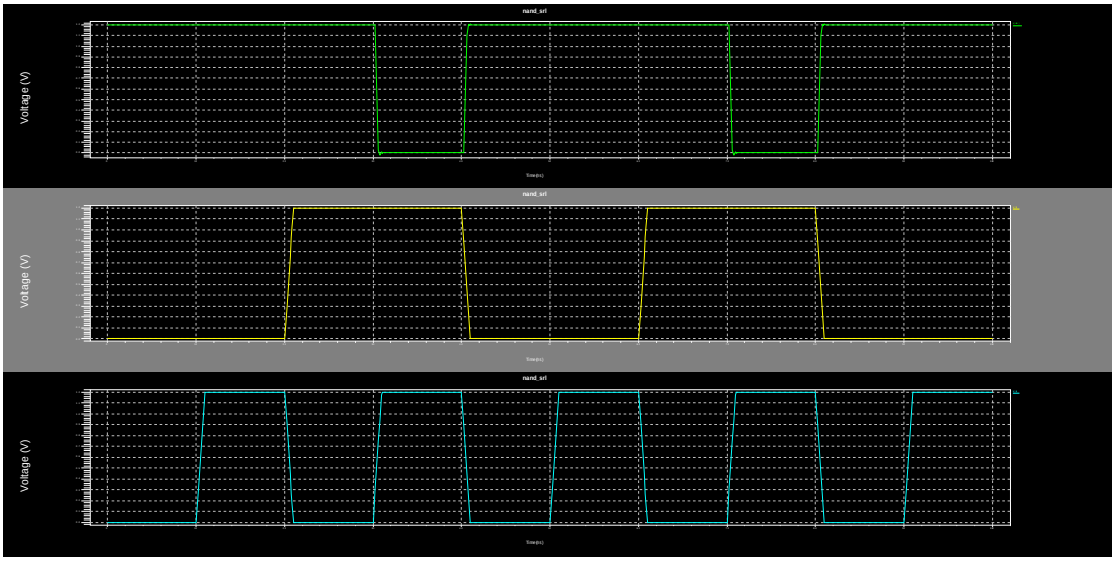
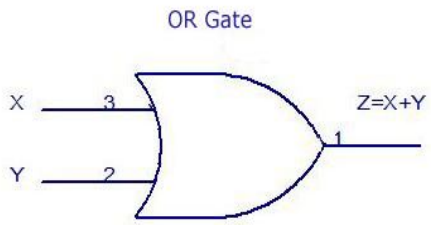



Fig.12W-edit output waveform of SRGDI NAND gate

*C. Or Gate*

An OR gate performs like two switches in parallel supplying a light, so that when either of the switches is closed the light is on. An OR gate is a digital logic gate that gives an output of 1 when any of its inputs are 1, otherwise 0. It implements logical disjunction and also it behaves according to the truth table [10]. A HIGH output (1) results if one or both the inputs to the gate are HIGH (1). If neither input is high, a LOW output (0) results. The truth table and primitive cell diagram of SRGDI OR gate is shown in fig.13 and fig.14 respectively.




TRUTH TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Fig.13Truth table of OR gate

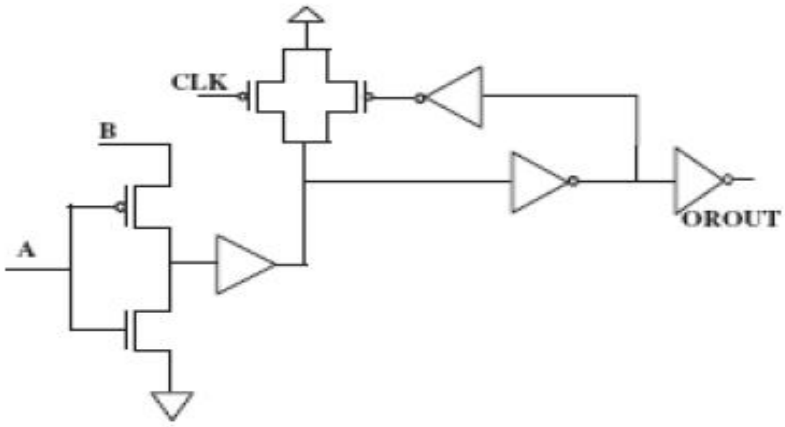



Fig.14Primitive cell of SRGDI OR gate

The simulation of SRGDI OR primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI OR primitive cell is shown in fig.15 and fig.16 respectively.

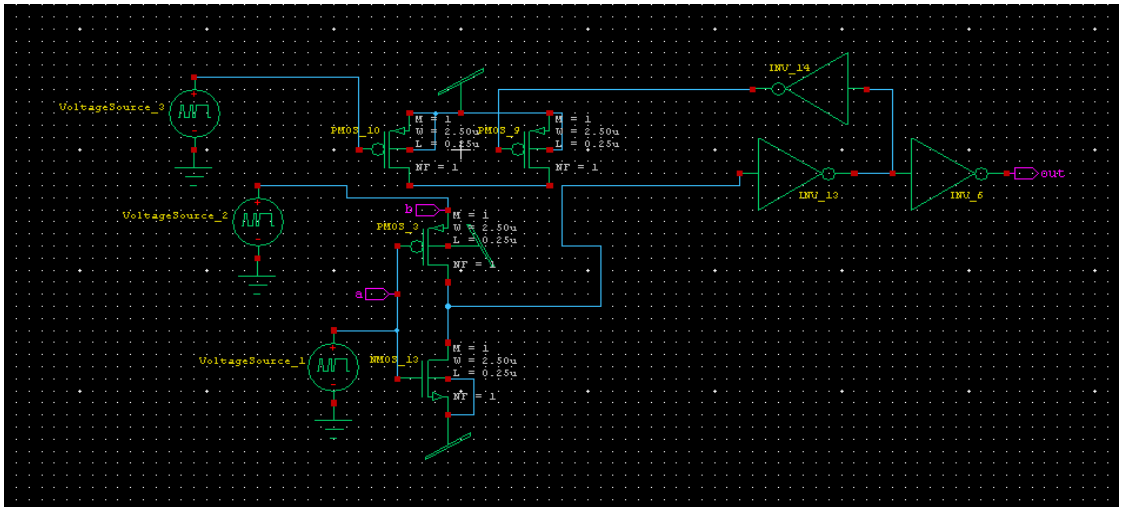



Fig.15S-edit schematic cell of SRGDI OR gate

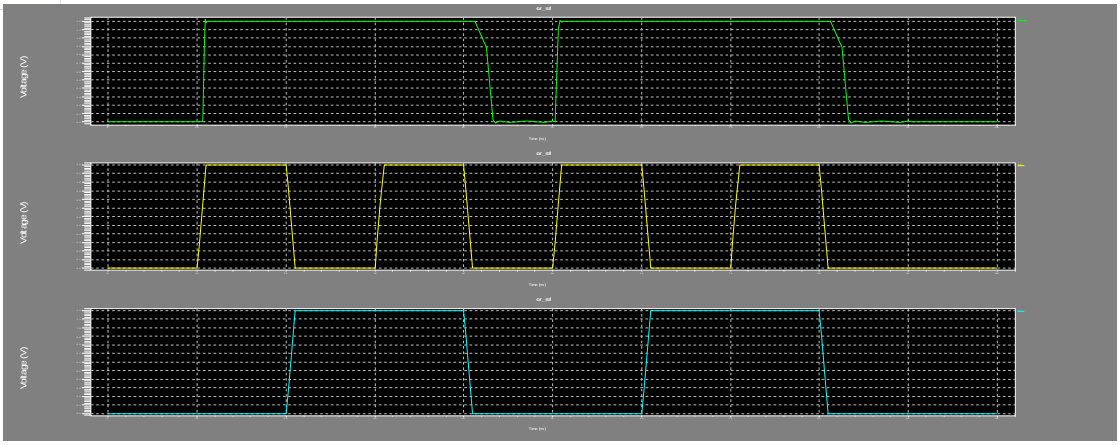


Fig.16 W-edit output waveform of SRGDI OR gate

*D. Nor Gate*

A NOR gate is a type of logic gate that works on the principle of "neither this nor that." This type of digital logic gate produces a high output only if two binary results are satisfied by a zero or low input. The NOR gate is a digital Logic gate that implements Logical NOR- it behaves according to the truth table . A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator. The truth table and primitive cell diagram of SRGDI NOR gate is shown in fig.17 and fig.18 respectively.


| A | B | Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Fig.17Truth table of NOR gate

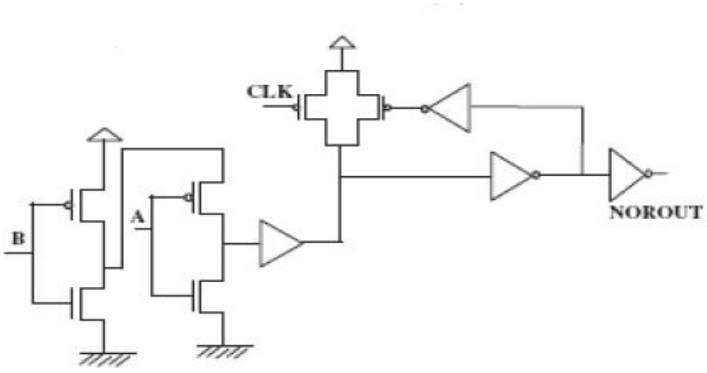



Fig.18Primitive cell of SRGDI NOR gate

The simulation of SRGDI NOR primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI NOR primitive cell is shown in fig.19 and fig.20 respectively.

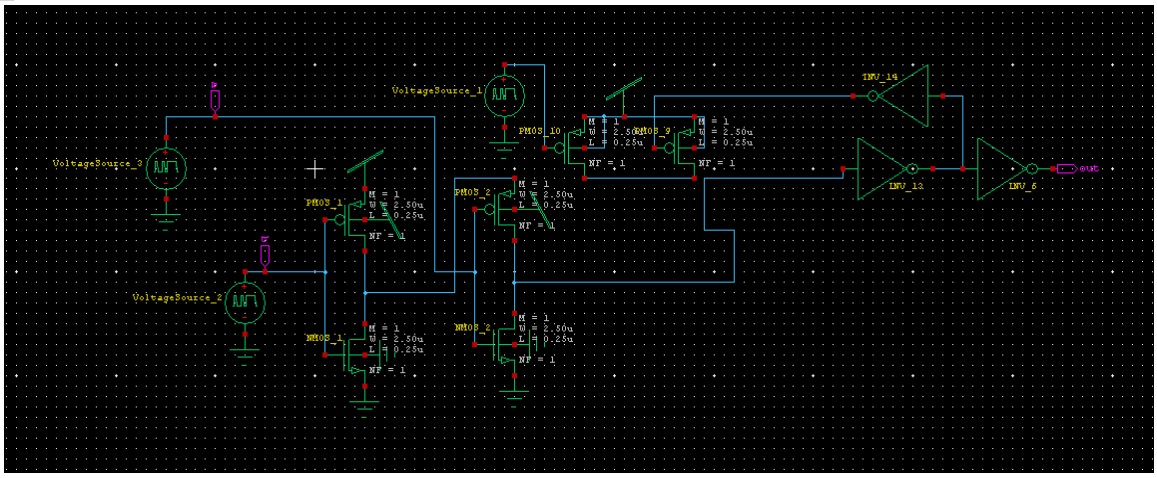



Fig.19 S-edit schematic cell of SRGDI NOR gate

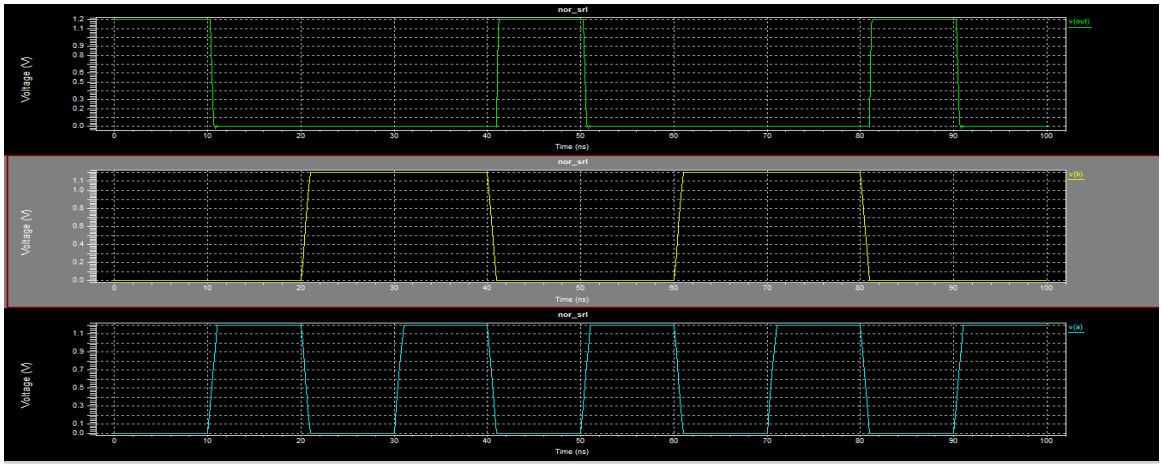



Fig.20 W-edit output waveform of SRGDI NOR gate

## IV. IMPLEMENTATION OF SRGDI PRIMITIVES IN ADDER CIRCUITS

*A. Half Adder*

A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value. It has two inputs, called A and B, and two outputs S (sum) and C (carry). The common representation uses a XOR logic gate and an AND logic gate. The truth table and primitive cell diagram of SRGDI Half Adder is shown in fig.21 and fig.22 respectively.

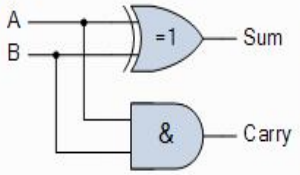
| Symbol | Truth Table | | | |
|---|---|---|---|---|
|  | B | A | SUM | CARRY |
| | 0 | 0 | 0 | 0 |
| | 0 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 |
| | 1 | 1 | 0 | 1 |



Fig.21Truth table of Half Adder

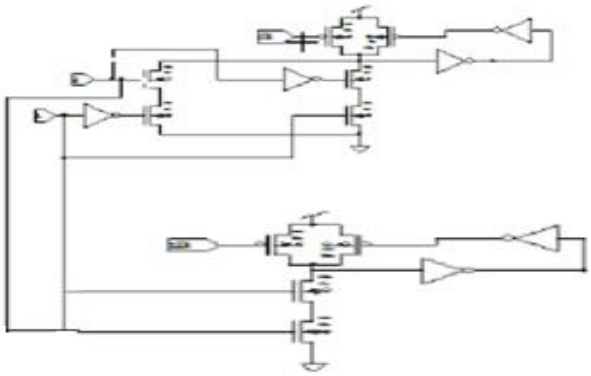


Fig.22Primitive cell of SRGDI Half Adder

The simulation of SRGDI Half Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI Half Adder cell is shown in fig.23 and fig.24 respectively.

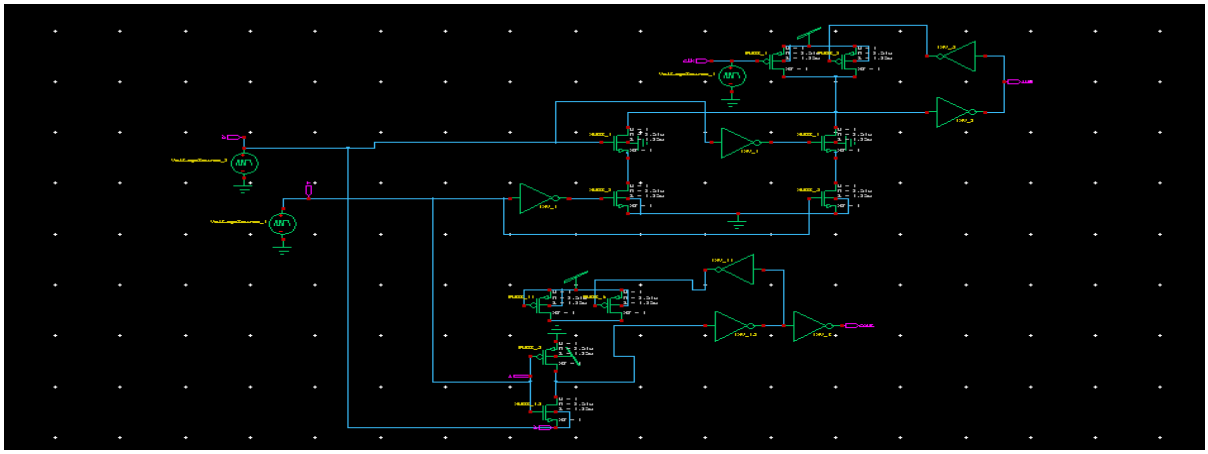


Fig.23 S-edit schematic cell of SRGDI Half Adder

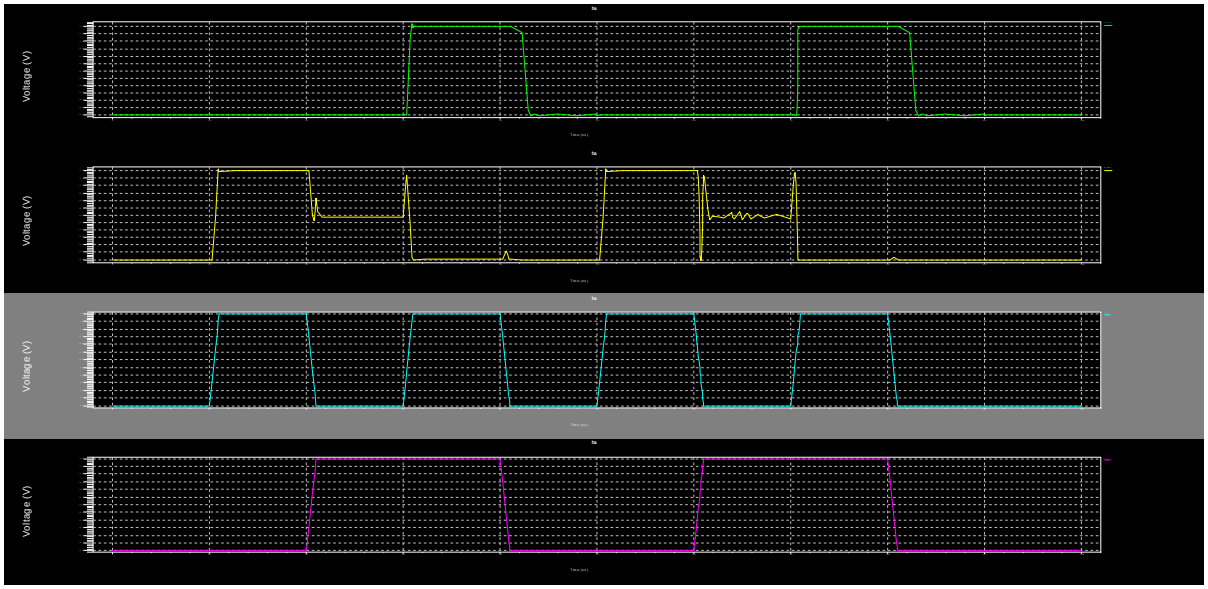
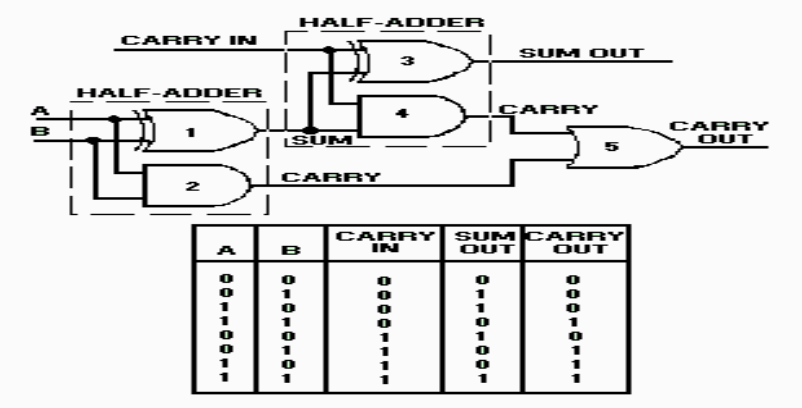



Fig.24 W-edit output waveform of SRGDI Half Adder

*B. Full Adder*

A full adder is a digital circuit that performs addition. Full adders are implemented with logic gates in hardware. A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, which adds two binary digits. The full adder is usually a component in a cascade of adders, which add 8, 16, 32 etc. binary numbers. The truth table and primitive cell diagram of SRGDI Full Adder is shown in fig.25 and fig.26 respectively.




| A | B | CARRY IN | SUM OUT | CARRY OUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Fig.25Truth table of Full Adder

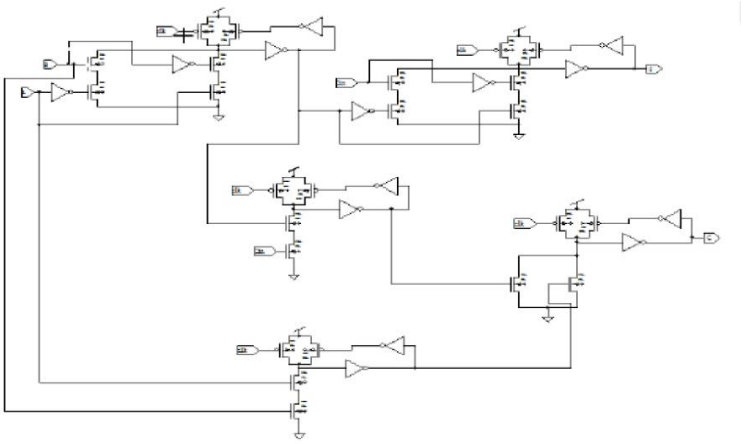


Fig.26Primitive cell of SRGDI Full Adder

The simulation of SRGDI Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI Full Adder cell is shown in fig.27 and fig.28 respectively.

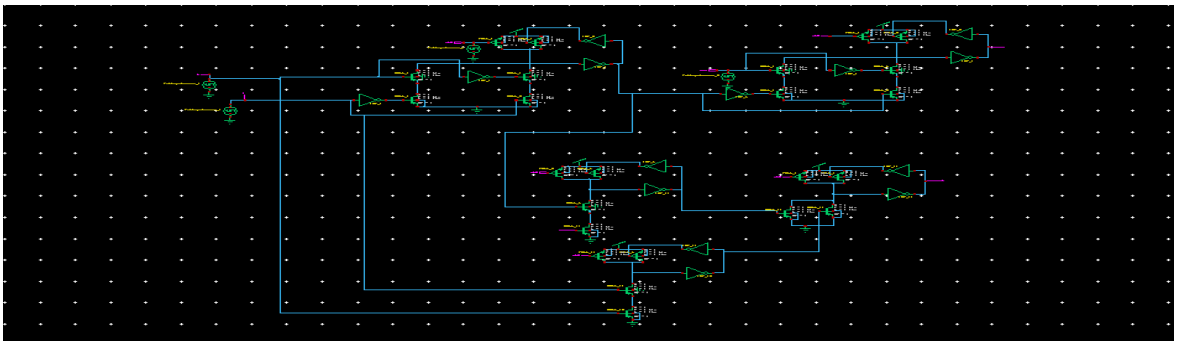


Fig.27 S-edit schematic cell of SRGDI Full Adder

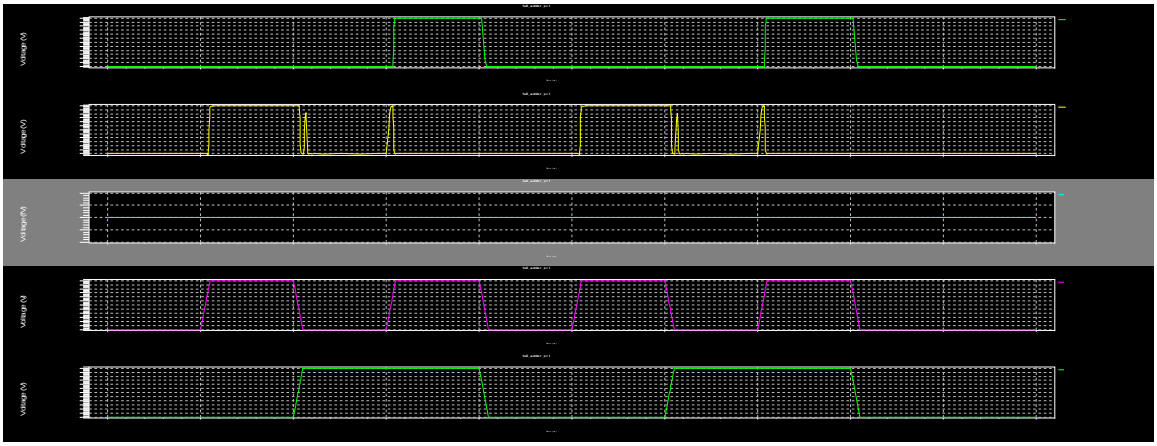


Fig.28 W-edit output waveform of SRGDI Full Adder

## V. SIMULATION RESULTS AND COMPARISON

Simulations are performed using Tanner EDA using 130nm technology nodes. The analysis shows reduced power, delay and PDP for proposed SRGDI logic compared to GDI, MGDI and FSGDI approaches. The simulation results are tabulated in table 1.

TABLE I
SIMULATION RESULT COMPARISON SHOWING VARIOUS GDI STYLES

| Parameters | GDI | MGDI | FSGDI | SRGDI |
|---|---|---|---|---|
| Power (µw) | 8.89 | 7.05 | 5.23 | 4.60 |
| Delay (ns) | 2.50 | 1.79 | 0.97 | 0.35 |
| Power Delay product (ns) | 22.22 | 12.62 | 5.07 | 1.36 |

From above table it is clear that the proposed SRGDI design shows considerable improvement in power and delay performance. The comparison chart showing the variations of proposed SRGDI approach with other existing approaches like GDI, MGDI and FSGDI is shown in fig.29.

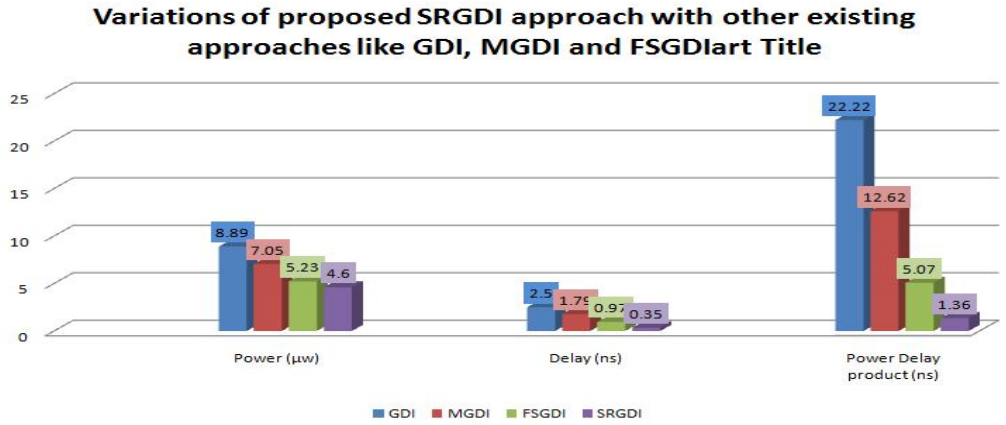



Fig.29 Variations of proposed SRGDI approach with other existing approaches like GDI, MGDI and FSGDI

## VI. CONCLUSIONS

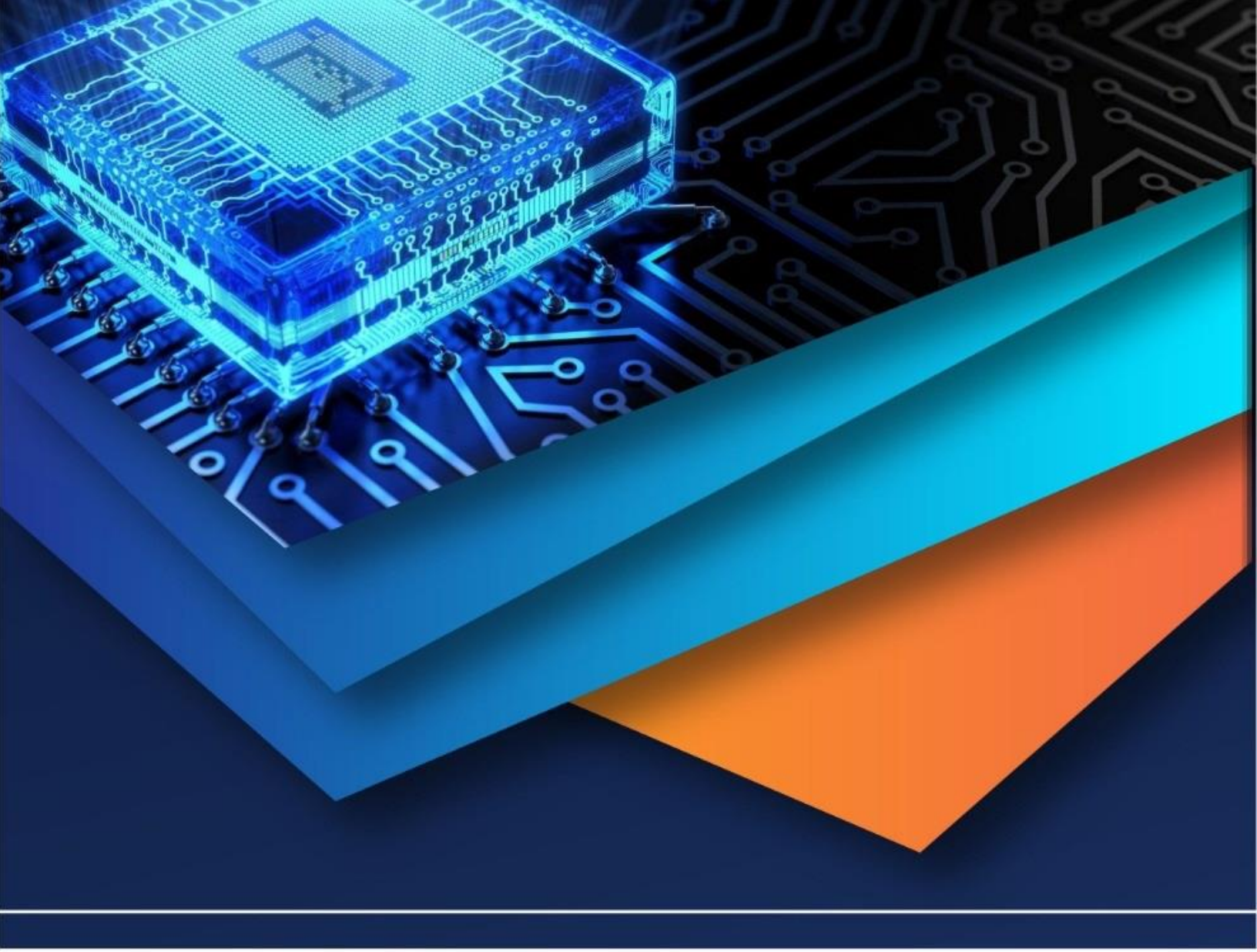
The A new technique based on GDI SRL was proposed with advantage of low power consumption to existing technique. The proposed technique shows two-fold improvement in power consumption and considerable improvement in delay of the sum and carry outputs. The proposed design can be used in low power logic circuits due to its low power and low device count. The proposed SRLGDI primitives and adders logic performs better than different logic and it's existing counterparts. While comparing the other techniques of GDI our proposed method (SRLGDI) represents low power, less delay and low PDP . On the whole about 54% of power and 36% of PDP have been achieved using this proposed SRLGDI logic when compared with the best of the existing logics.

## VII. ACKNOWLEDGMENT

Our Sincere thanks to Dr. R. Naveen HOD/ECE for supporting throughout the course of the work. We also extend our thanks to the management of Info Institute of Engineering, Coimbatore for providing the research lab for the work.

## REFERENCES

[1] Uma, R., Dhavachelvan, P., 2012a, New Low power delay element in self resetting logic with modified gated diffusion input technique. In: IEEE International Conference on Semiconductor Electronics,
[2] Saravanan Savadipalayam Venkatachalam, Sivakumar Sabapathy Arumugam, Sasipriya Sivasubramaniyam, "Design of Low Power Flip Flop Based on Modified GDI Primitive Cells and Its Implementation in Sequential Circuits", International Journal of Advances in Computer and Electronics Engineering, Volume 2, Issue 5, May 2017, pp. 22 - 32.
[3] Agrawal, Adarsh Kumar, Wairya, S., Nagaria, R.K., Tiwari, S., 2009. A new mixed gate diffusion input full adder topology for high speed low power digital circuits.World Appl. Sci. J. 7, 138–144.
[4] Aguirrre-Hernandez, M., Linares-Aranda, M., 2011. CMOS full-adders for energy-efficient arithmetic applications.IEEETrans.Very Large Scale Integr. VLSI Syst.19 (4), 718–721.
[5] Balsara, P.T., Steiss, D., 1996. Performance of CMOS differential circuits. IEEE J. Solid-State Circuits 31, 841–846.
[6] Bisdounis, L.,Gouvetas,D.,Koufopavlou,O.,1998.Acomparativestudy of CMOS circuit design styles for low-power high-speed VLSI circuits. Int. J. Electron. 84, 599–613.
[7] Chatzigeorgiou, A., Nikolaidis, S., 2001. Modelling the operation of pass transistor and CPL gates. Int. J. Electron. 88, 977–1000.
[8] Ghadiry, M.H., Nadisenejani, M., Miryahyaei, M., 2010. A new full swing full adder based on a new logic approach. World Appl. Sci. 11 (7), 808–812.
[9] Kim, W.J., Kim, Y.B., 2001. A localized self-resetting gate design methodology for low power. In: Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems, August 14–17,2001, Dayton, OH, pp: 305–308.
[10] Litvin, M.E., Mourad, S., 2005. Self-reset logic for fast arithmetic applications.IEEETrans.Very Large Scale Integr.Syst.13,462–475.
[11] Mirzaee, R.F., Moaiyeri, M.H., Navi, K., 2010. High speed NPCMOS and multi-output dynamic full adder cells. World Acad. Sci. Eng. Technol. 39, 698–704.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY